The 2025 Symposium on VLSI Technology & Circuits, The VLSI field thrives on continuous growth with the Theme: "Cultivating the VLSI Garden : From Seeds of Innovation to Thriving Growth"

Tokyo, Japan (APRIL 18, 2025) – For the 45th consecutive year delivering a unique convergence of microelectronics technology and circuits in one venue, Symposium on VLSI Technology & Circuits will offer as an in-person event in Kyoto, Japan on June 8–12, 2025. The five-day event will take place at the Rihga Royal Hotel Kyoto to showcase the theme of "Cultivating the VLSI Garden : From Seeds of Innovation to Thriving Growth". The Symposium will feature advanced VLSI technology developments, innovative circuit designs, and the applications they enable, such as artificial intelligence(AI), machine learning, IoT, wearable/implantable biomedical devices, big data, cloud/edge computing, and augmented/virtual reality (AR/VR).

The weeklong Symposium is the premier global venue that promotes synergies between technologists and designers on today's applications and future breakthroughs. In addition to the technical presentations, the Symposium program will feature a demonstration session, joint focus sessions, evening panels, short courses, and workshops.

Plenary Sessions:

• "Driving Innovation in DRAM Technology : Towards a Sustainable Future" by Seon-Young Cha, CTO, Head of R&D, SK hynix

Since the introduction of the $6F^2$ Buried Gate Scheme in the early 2010s, DRAM technology has evolved based on platforms that can be continuously scaled down to 10nm technology. Beyond 10nm, however, the evolution of DRAM technology has reached an inflection point where it is difficult to build scalable platforms using existing cell schemes and meet the high-performance demands of the AI era. In response to the inflection point, this presentation will review how cell schemes will change to ensure a scalable platform and describe how DRAM technology can innovate in a way that delivers new values in the era of AI.

• "Innovate VLSI for AI Growth" by John Chen, Corporate Vice President of Technology and Foundry Management, NVIDIA

AI is built on VLSI by the amazing Moore's law which has ended, but we need VLSI more than ever in the AI era. So, what's next? It's innovation, innovate from materials, devices, modules to systems. This speech presents the progress of VLSI from the past decade and highlights the most complicated VLSI chip today. Innovation is easier said than done. What are the criteria and barriers for success and what leadership is needed to cultivate innovation? The speaker's career has lived through the relationship between VLSI and AI, their similarity, synergism and reinforcement that accelerates their thriving growth. With AI taking away routine and complicated tasks, it raises the question of what young people should be doing? While AI is becoming such a powerful tool, the leaders and engineers must help to grow ethics and morality for mankind.

• "Enabling Generative AI : Innovations and Challenges in Semiconductor Design Technologies" by Kou-Hung Lawrence Loh, Corporate Senior Vice President, MediaTek Inc, President, MediaTek USA Inc.
In recent years, Generative AI has profoundly transformed a wave of revolution across all fields, from our daily life to advanced science exploration. This transformation has triggered an unparalleled increase in the demand for computing, connectivity/communication, and memory/data storage across data centers, infrastructures, and edge devices. The uptick has catalyzed booming industrial investments spanning a spectrum of "hard tech" based on advanced materials, packaging and semiconductor process technologies, such as hardware accelerators, wired and wireless connectivity/communication, and heterogeneous integrations from chip to discrete levels, all supported by substantial research and development investments to embrace the AI era.
In this presentation, we will explore the frontier of cutting-edge technologies and tackle the challenges associated with developing high-performance computing and high-speed connectivity solutions under considerations to accomplish demanding energy efficiencies. Additionally, we will address the mounting demands posed by power distribution and other engineering complexities. Our focus will highlight the pivotal role of innovation and investments to ensure the long-term sustainability in the forthcoming decades.

• "The evolution of edge AI : contextual awareness and generative Intelligence" by Alessandro Cremonesi, Executive Vice President, Chief Innovation Officer, General Manager of System Research and Applications, STMicroelectronics
We are witnessing a rapid transition from traditional AI to generative AI in the cloud. This is driving increased demands in the high-performance computing domain. However, to support this shift sustainably, edge AI technologies are advancing, including hardware accelerators (NPU) in microcontrollers and disruptive technologies like in-memory and neuromorphic computing. These developments, along with optimized large language models, enable more efficient AI and generative AI solutions for edge products. This keynote will explore the transformative potential of contextual awareness in AI for edge devices. Advanced sensing technologies and generative AI will revolutionize interactions with the world, allowing AI to adapt based on localized experiences and migrate seamlessly across devices. These innovations will drive the future of technology, making it more cognitive, generative, and interactive, ultimately leading to smarter, more connected and more sustainable solutions.

Focus Sessions:

The Symposium program integrates technology & circuit topics through three Joint Focus sessions: 1) Design-Technology Co-Optimization (DTCO) and Design Enablement, 2) AL and ML Hardware, 3)3D Integration and Photonics. In addition, there are two Technology focus sessions on: 1) Memories for AI Applications, and 2) Advanced 3D Stacked Transistors.

Short Courses on Key VLSI Topics:

Two full-day short courses will be featured:

- Short Course 1: "*Key VLSI technologies in the AI era*" highlights key technologies for advanced logic, memory and heterogeneous integration. The course will cover advanced CMOS technologies, novel materials, advanced process technologies, heterogeneous / 3D integration, DRAM, emerging memories, DTCO / STCO, and 3D integrated image sensors.

- Short Course 2: "*Circuits and Systems for AI and Computing*" highlights the latest advances in circuits and systems driving the evolution of AI and computing. The course will cover the latest trends in AI and computing, scalable computing, efficient AI architectures, and the technologies behind them such as EDA, chip-to-chip communications, silicon photonics, high-speed memory, storage and power supply circuits.

Evening Panel Discussions:

- *"What can semiconductor industry do for greener society?*

  This panel discussion explores the crucial role of the semiconductor industry in building a sustainable future. As the world grapples with climate change and environmental challenges, semiconductors are at the forefront

of technological advancements driving positive change. Key discussion topics include energy-efficient technologies enabled by advanced VLSI and sustainable manufacturing. The panel, featuring six experts in this field, will be moderated by Bala Haran from AMAT.

- *"Practical Circuits & Technology Training : Academia vs. Industry – Where Do We Learn the Most ?"*

  Traditional education may not fully prepare IC designers for real-world challenges. However, obtaining a sound theoretical basis and strong understanding of basic principles of electrical engineering and systems design is learned at an academic institution that also imparts critical thinking skills. So, is learning best done on the job or is there something that on-the-job training just doesn't teach you? Audience participation is encouraged. A scorecard will track academia vs. industry, with final scores revealed at the event's end.

Demo Session:
Introduced in 2017, the popular in-person demonstration session will again be part of the Symposium program, providing participants an opportunity for in-depth interaction with authors of selected papers from both Technology and Circuits sessions. Approximately 15–20 tabletop presentations will demonstrate device characterization, chip operational results, and potential applications for circuit-level innovations. The best demo will be selected by Symposium attendees.

Workshops:
To support the conference theme: "Cultivating the VLSI Garden: From Seeds of Innovation to Thriving Growth." The workshop sessions are designed to merge cutting-edge research in areas not covered in detail in the Symposium technical program, and could serve as topics for future Symposium sessions. The workshop sessions will be held in person. This year, we have 1 Special Workshop and 12 Regular Workshops. The topics are as follows.

Special Workshop: Centennial Anniversary of FET Invention: Past, Present, and Future (FET 100)

Regular Workshops:
- Required circuits and systems for LLM inference,
- Manufacturing with AI,
- Heterogeneous System integration including HBM, Packaging and EDA tools.
- Compute-in-Memory, biosensors, and GaN.

Special Events at the Symposium include mentoring events sponsored by the Women in Engineering and Young Professionals groups of the IEEE Solid-State Circuits Society.

Best Student Paper Awards for each track of the Symposium are chosen based on the quality of the papers and presentations. The candidates whose papers were praised in our review will receive a BSPA finalist certificate at each session. The BSPA recipients will receive a monetary award, travel cost support, and a BSPA certificate. For a paper to be reviewed for this award, the lead author and presenter of the paper must be enrolled as a full-time student at the time of submission and must indicate on the web submission form that the paper is a student paper.

Further information about the Symposium is available at: http://www.vlsisymposium.org.

Sponsoring Organizations:
The VLSI Symposium on Technology & Circuits is sponsored by the Japan Society of Applied Physics, the IEEE Electron Devices Society, the IEEE Solid State Circuits Society, and in cooperation with the Institute of Electronics, Information and Communication Engineers.

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