Technical Highlights from the 2026 Symposium on VLSI Technology and Circuits

The 2026 IEEE/JSAP Symposium on VLSI Technology and Circuits is a premier international conference scheduled for June 14 - 18, 2026 that showcases breakthroughs, advances, and evolution of micro/nanoelectronics. The joint technology and circuits symposium will be held in person at the Hilton Hawaiian Village in Honolulu, Hawaii to enable networking opportunities, with access to OnDemand content following the Symposium.

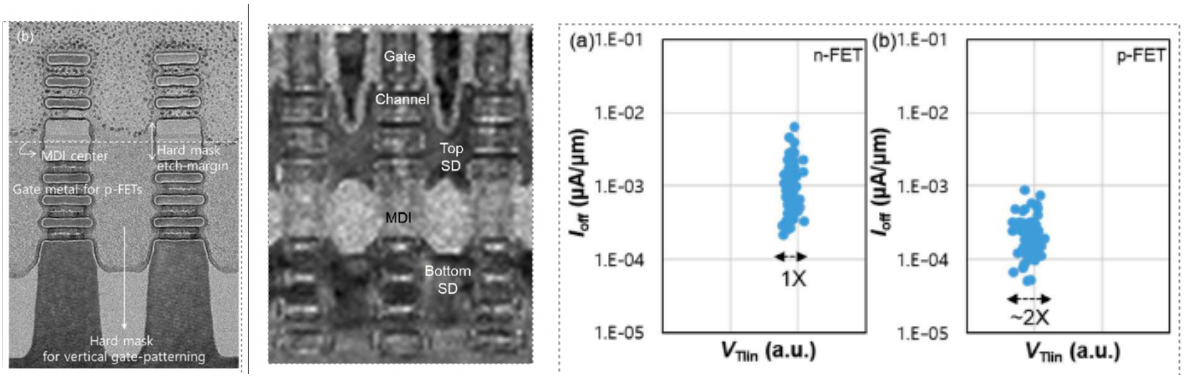
The Symposium's overall theme, ***"Advancing the AI Frontier through VLSI Innovation,"*** integrates advanced technology developments, innovative circuit design, and the applications that they enable, as part of a worldwide transition to a new era of intelligent connected devices, energy efficient infrastructure, and AI enabled hardware systems that change the way humans interact with each other.

The following are some of the highlighted papers that address this theme:

Technology Highlights

Advanced CMOS Technology

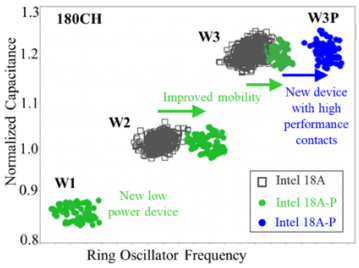
Samsung 3D Stacked FETs (3DSFETs) with Triple Nanosheet Channels: Samsung will present, for the first time, a 3D stacked FET with triple-stacked nanosheet channels for both n- and p-FETs on the same wafer. This is the largest number of nanosheets ever presented for a 3D stacked FET – or CFET. In addition, with the smallest gate pitch of 42nm, this work has shown the most aggressive CFET scaling which could be industrialized. ***(Paper T1.1, "First Demonstration of 3D Stacked FETs at Gate Pitch of 42nm Featuring Triple Stacked Nanosheet Channels for Advanced Logic Applications," Donghoon Hwang et al, Samsung Electronics)***

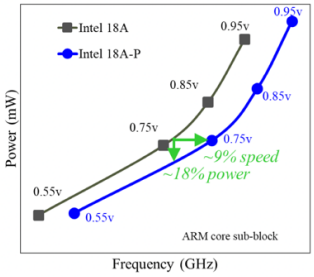


Figures: **(Left)** TEM image after formation of suitable gate metals for n- and p-FETs. **(Middle)** TEM image of the final fabricated 3DSFETs at gate pitch of 42nm and triple-stacked nanosheet channels **(Right)** Electrical characteristics of 3DSFETs with I_{off} vs. I_{Dsat} for n-FETs and p-FETs.

Intel 18A-P Advanced RibbonFET (GAA) Technology: Intel will present the first performance enhancement in their 18A technology family. By introducing additional logic VT pairs, skew corner tightening, new low power and new high-performance devices, lower thermal resistance, this 18A-P achieved 9% iso-power performance gain, or over 18% energy efficiency at iso-performance, with matched SRAM V_{min} and improved logic negative-bias temperature instability (NBTI). 18A-P was introduced as design-compatible with 18A. ***(Paper T1.2, "Intel 18A-P CMOS Technology Enhancement Featuring Advanced RibbonFET (GAA) Transistors and PowerVia for High-Performance Computing," A. Bowonder, et al, Intel Foundry)***

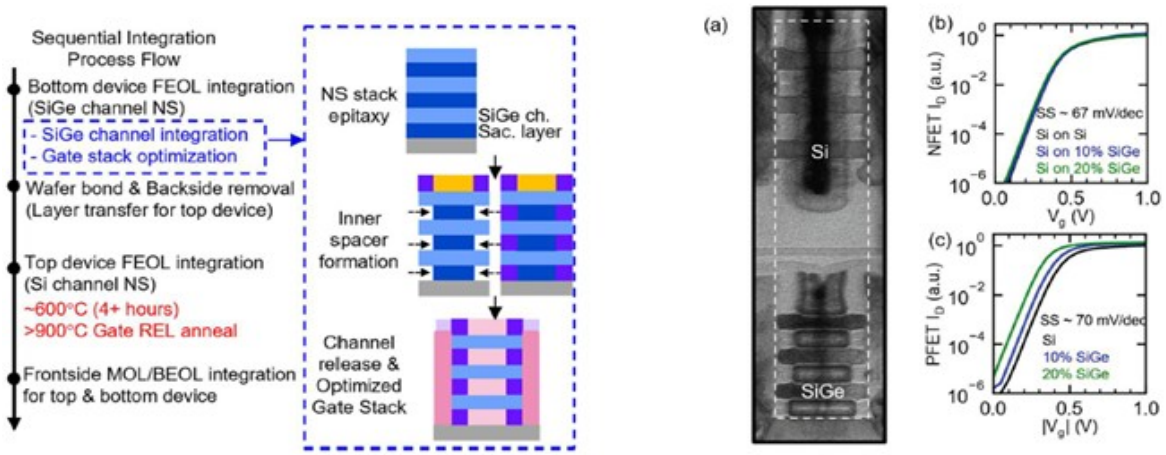
	18A Feature List		18A-P feature list	
Performance @Iso-Power	1x		9% Iso-Power Performance Gain	
Contacted Poly pitch (nm)	50		50	
Library Height (nm)	180	160	180	160
Transistor	W2, W3	W1, W2, W3	W2, W3	W1, W2, W3
			W1 (Low Power)	W1.5 (Low Power)
			W3P (HP contact)	W3P (HP contact)
VT	4 pairs of Logic VTs		5+ pairs of logic VTs (New Logic VT between ULVT and LVT)	
			10mV lower ULVT	
Skew corners	Intel 18A Base Process		33% tightening in skew corners	
Interconnect RC			V0-V2 R reduction; M2-M4 jogs	
Thermals			Improved thermal conductivity by 50%	





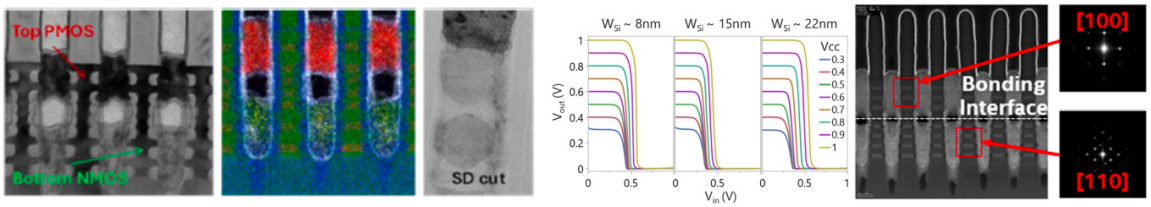
Figures: (**Left**) Intel 18A-P new technology features compared to Intel 18A (**Middle**) Performance of new devices (low power and high performance) in 18A-P (**Right**) Intel 18A-P demonstrates ~9% iso-power performance gain (at 0.75V) over Intel 18A on an industry standard ARM core sub-block.

IBM High-Temperature SiGe Nanosheet PFET: IBM will demonstrate SiGe nanosheet (NS) replacement-metal-gate (RMG) PFETs with high temperature stability exceeding 900°C, validated through sequential integration of a top Si NFET over a bottom SiGe PFET. The fabricated PFET devices were confirmed to exhibit excellent I_d-V_g characteristics with subthreshold slopes of 70mV/dec. These results pave the way for multi-tiered sequential integration. ***(Paper T5.4, "High-Temperature Resilient SiGe Nanosheet PFET RMG Towards Multi-Tiered Sequential Integration," N. Shanker et al, IBM Research)***



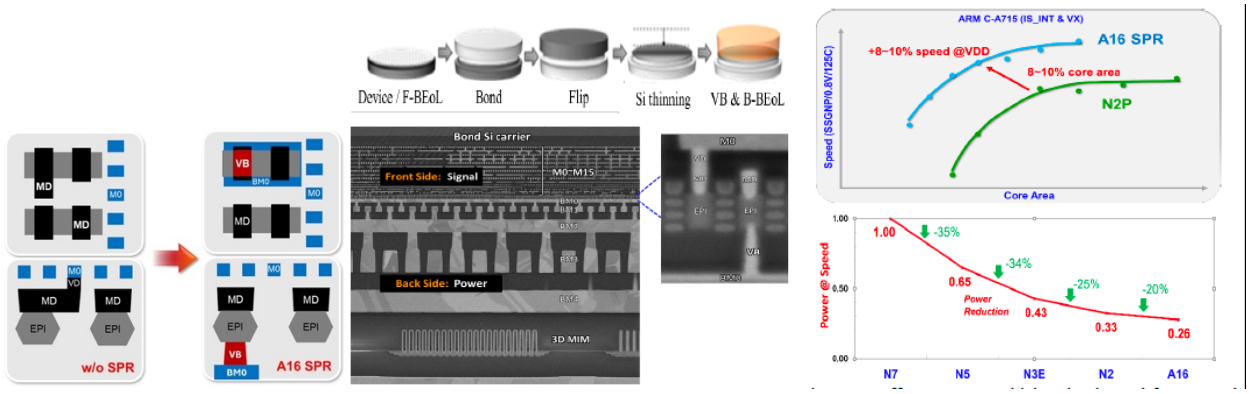
Figures: (**Left**) High-level integration process flow for stack FET with SiGe GAA NS channel (Bottom) and Si GAA NS channel (Top). (**Right**) Cross-section TEM of stacked Si NFET on thermally stable SiGe PFET showing excellent overlay. I_d-V_g curves for Si, 10% SiGe, and 20% SiGe devices after full sequential integration. All PFET devices show subthreshold slopes of ~70 mV/dec, suggesting no additional degradation due to interface traps in the SiGe channel devices.

Intel CFET Inverters with 2x2 RibbonFETs: Intel will demonstrate several new features of their CFET technology to provide the best PPA improvement with minimal process risk, which include 45nm Gate pitch, PowerVia, Direct Backside Contacts, Epi-to-Epi Via for Intra-connect (connecting the top and the bottom device), and uniquely PMOS on top of NMOS. In addition, a hybrid PMOS Si (110) on NMOS Si (100) stack with middle dielectric isolation (MDI) less than 10nm to enhance PMOS performance will be presented. ***(Paper T5.2, "Demonstration of CFET Inverters on Si (110) with 2X2 RibbonFETs at 45nm Gate Pitch with PowerVia and Direct Backside Contacts," J. A. Wiedemer et al, Intel Corporation)***



Figures: (**Left**) TEM micrograph of 2 ribbon CFET device at contacted poly pitch CPP=45nm post vertical dual epi on Si (110) substrate – the first CFET technology with PMOS on top **(Middle)** Voltage transfer characteristics (VTC) of CFET inverters at CPP=45nm on Si (110) wafers with VCC ranging from 0.3V to 1V, representing the furthest advances in CFET technology to date **(Right)** EM micrograph of bonded wafers processed using the same monolithic CFET process, showing channel orientation of Si (110) and Si (100).

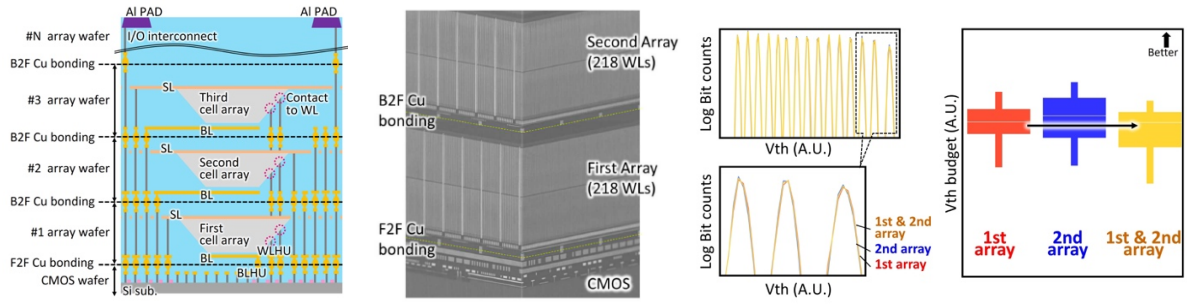
Late News Paper – TSMC A16 Angstrom-class CMOS Technology: TSMC will present their A16 platform technology – their latest GAA technology with backside power delivery solution incorporating a novel backside direct contact – named Super Power Rail (SPR). Compared with N2P (performance-enhanced N2), A16 provides a further 8%-10% faster speed at the same power, or 15%-20% power improvement and additional 8%-10% chip density gain. Mass production for this A16 is slated for Q4'26. ***(Paper T1.5, "A16 Angstrom-class CMOS Technology featuring Enhanced Nanosheet Transistors with SuperPower Rail (backside direct contact power delivery) for AI and HPC Applications", G. Yeap et al, TSMC)***



Figures: (**Left**) Schematic of A16-SPR with backside direct contact (VB) power delivery (**Middle**) SPR process flow schematics and A16 SPR TEMs showing enhanced nanosheet transistors with backside direct contacts power, front/back-side metals and 3D MiM (**Right**) A16 offers up to 10% higher density and faster speed than N2P benchmarked on an ARM core.

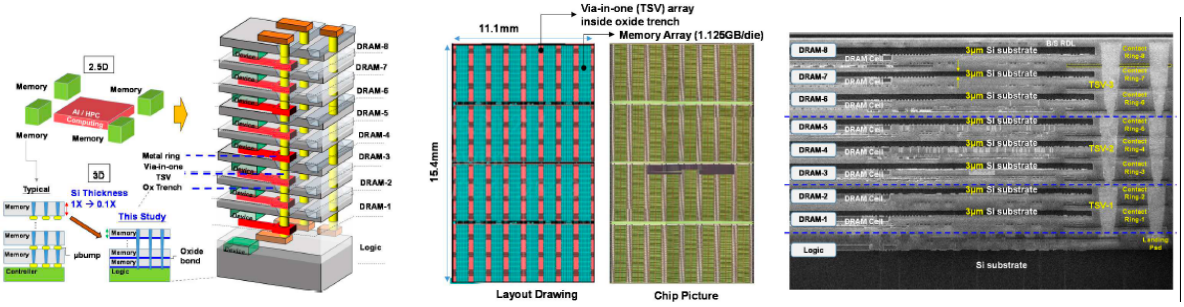
Memory Technology

Kioxia/Sandisk First QuadLevel Cell in Multi-Stacked Cell Array: Kioxia and Sandisk will jointly present the world's first successful QuadLevel Cell (QLC) operation of a multi-stacked cell array CMOS directly bonded to array (MSA-CBA). This breakthrough overcomes key challenges in high stacking of 3D flash memory: cell current degradation, wafer warpage, and large block (BLK) size. These results mark a milestone toward ultra-high-density 3D flash memory with over 1,000 stacked layers. ***(Paper T1.4, "A Multi-Stacked Cell Array Architecture with Wafer-to-Wafer Cu Direct Bonding for Ultra-High-Density 3D Flash Memory beyond 1,000 Word Lines," M. Noda et al, Kioxia Corporation)***



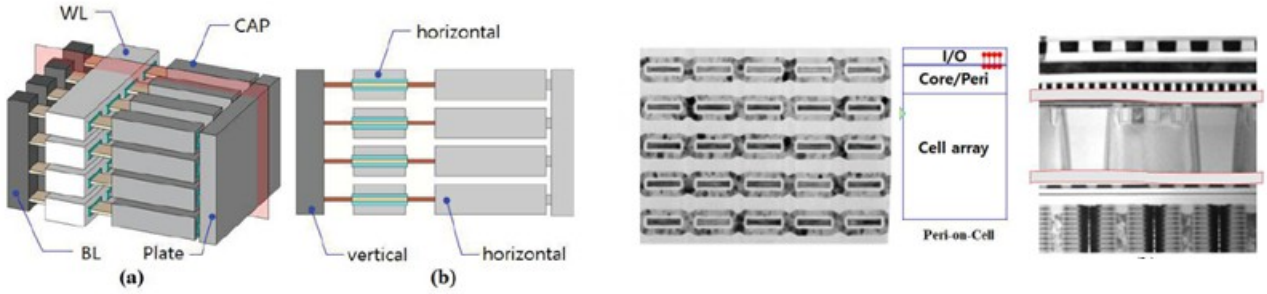
Figures: (**Left**) Conceptual illustration of the MSA-CBA device structure, showing sequential stacking and bonding **(Middle)** FIB-SEM image of a multi-stacked cell array, showing successful bonding of two array wafers, each with 218 WLs, demonstrating the effectiveness for large-scale stacking **(Right)** Comparison of individual first and second cell arrays with the overall MSA-CBA structure demonstrates stable V_{th} characteristics and reliable QLC operation in the BL selection type MSA-CBA.

SAIMEMORY Team 3D HB DRAM: Researchers from SAIMEMORY, Intel, PSMC and AP will demonstrate a multiple-wafer via-in-one TSV architecture implemented in a 3D high bandwidth DRAM. Every metal routing layer in the 8-stacked cube directly links to the TSV bus for providing better signal and power integrity. This architecture offers exceptional memory bandwidth (~0.25Tb/s/mm^2) at low data transfer power. ***(Paper T17.5, "Multiple-Wafer (9-layer), Extreme thin (3µm-Si per stack) and Innovative Fusion-bonded Via-in-one Architecture for High Bandwidth 3D Memory," C.- L. Lu et al, SAIMEMORY Corporation)***



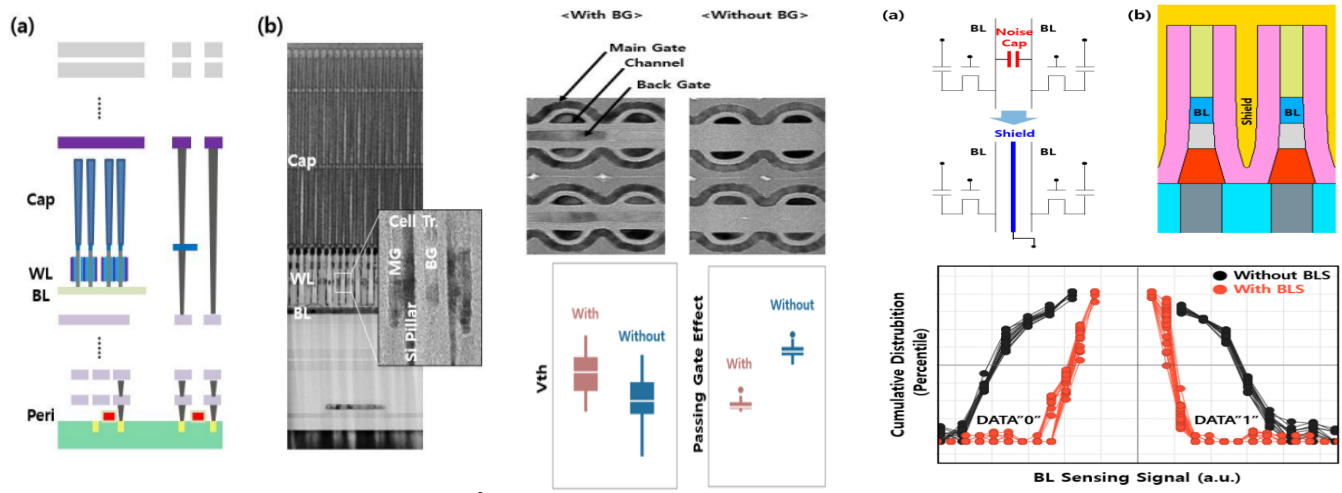
Figures: **(Left)** Comparison of the typical memory with micro bump in 2.5D packaging vs. fusion-bonded 3D Memory with via-in-one TSV **(Middle)** Top view of the 3D Memory layout drawing and chip micrograph - the memory array of 1.125GB consists 13.7K via-in-one TSV array per die **(Right)** Cross-sectional images of the 1+8-stacked Logic/DRAM architecture – extreme thin Si substrate (~3µm) in each DRAM was formed. Via-in-one contacts 2 to 3 metal rings in each set.

Samsung 16-tier VS-DRAM: To address DRAM scalability challenges beyond the 10nm node, Samsung will demonstrate a 16-tier Vertically Stacked DRAM (VS-DRAM) employing Gate-All-Around (GAA) cell transistors (CTR) and horizontal storage capacitors (CAP). In addition, they will demonstrate the viability of Peri-on-Cell (PoC) architecture by fabricating core/peri device on separate wafers and bonding on the cell wafer, highlighting it as a promising candidate for future memory technology. ***(Paper T5.1, "Vertically Stacked DRAM Technology for Scaling Evolution," S.U. Han, Samsung Semiconductor)***



Figures: (**Left**) (a) Bird eye's and (b) cross-sectional views of schematic illustration of VS-DRAM with horizontal write line (WL), vertical bit line (BL), and horizontal capacitor. (**Right**) Cross-sectional TEM image of fabricated gate-all around devices and TEM image of Peri-on-Cell (PoC) emphasizing that the PoC approach is better in terms of I/O efficiency.

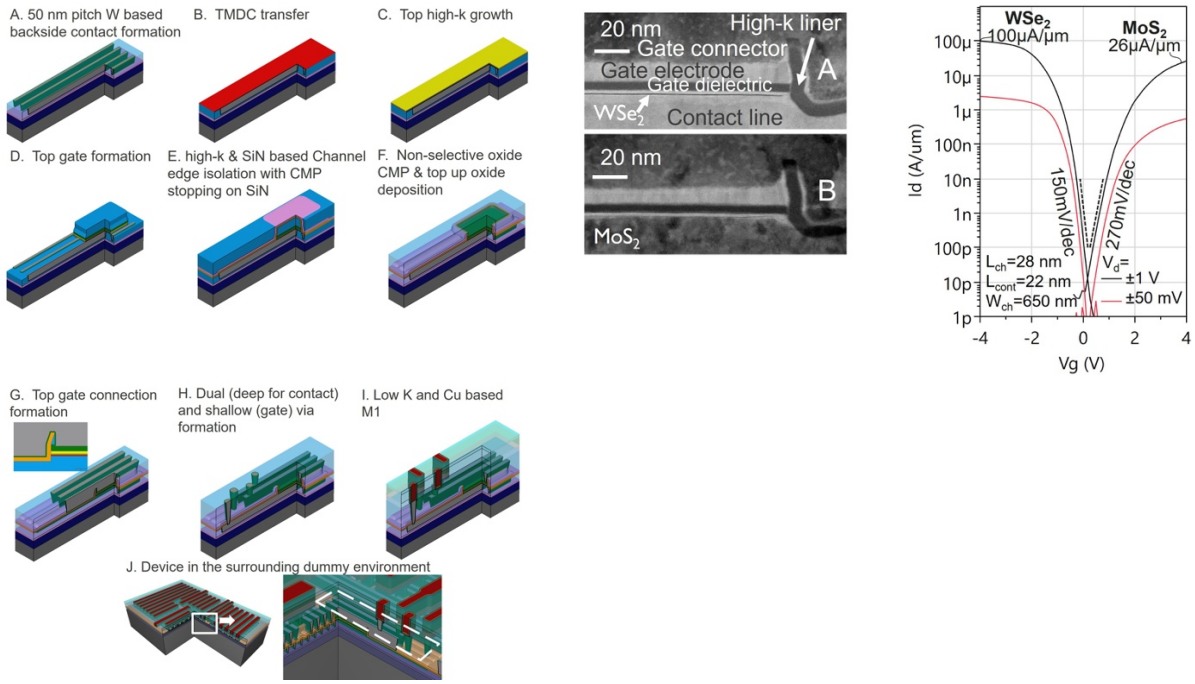
Late News Paper – SK Hynix 4F^2 Vertical Gate (VG) DRAM: SK Hynix will present the electrical characteristics of their 4F^2 Vertical Gate DRAM which incorporates key technology features including bit-line shielding (BLS) to suppress coupling noise and shared back gate (BG) to enhance threshold voltage (V_{th}) control and passing gate effect. Die thinning is also introduced to support reliable circuit operation in wafer-bonded structures. Robust performance of cell transistor and read-write operation of 4F^2 VG DRAM is achieved. ***(Paper T8.5, "Electrical Characteristics of the 4F2 Vertical Gate (VG) DRAM integrated with BitLine Shielding (BLS) and Back Gate (BG) Transistor," S. W. Chu et al, SK Hynix)***



Figures: (Left) (a) Schematic diagram of 4F^2 VG DRAM cell transistor integrated with peripheral devices through fusion wafer bonding and **(b)** Cross-sectional TEM image of 4F^2 VG DRAM **(Middle)** TEM plane views of VG DRAM array and the effect of Back-gate on the functionality of VG cell transistor. (**Right**) Conceptual design and schematic diagram of BLS structure - BLS improves significantly the BL sensing failure

Processes and Materials for CMOS Scaling and New Devices

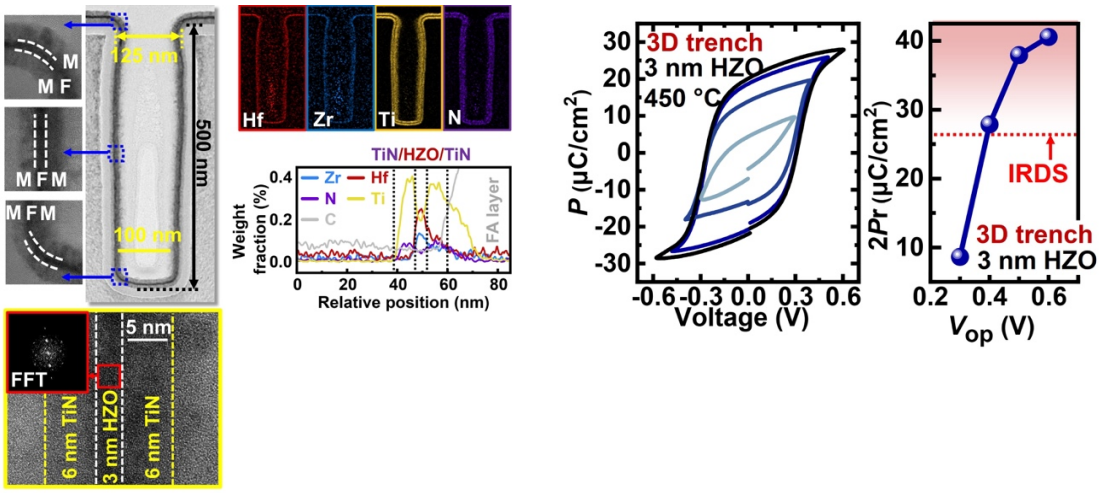
EUV Lithography for 2D Materials: imec will demonstrate a novel integration flow for transistors with 2D materials channel, utilizing EUV lithography and 300mm fab processes. This approach enabled the fabrication of scaled transistors featuring contact pitches down to 50nm, active widths down to 75nm, and an equivalent oxide thickness (EOT) of approximately 2nm. Furthermore, quasi-CMOS integration was achieved by using different channel materials, MoS_2 for NMOS and WSe_2 for PMOS, side by side on the same wafer by die or small wafer transfer method. ***(Paper T1.3, "First EUV-enabled Integration Route for 50nm Pitch N and PMOS Transistors with 2D Materials Channel from a 300mm Fab," T. Schram, imec)***



Figures: (**Left**) Proposed process flow (**Middle**) Cross-sectional STEM images of fabricated transition metal dichalcogenide (TMD) materials (WSe_2 for NMOS and MoS_2 for PMOS). (**Right**) I_d-V_g characteristics of the fabricated NMOS and PMOS devices.

Device Physics, Characterization, Modeling and Reliability

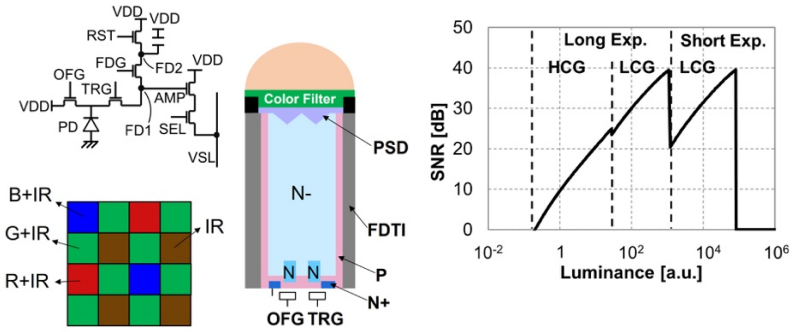
Universities Collaborate to Investigate 3D MFM Capacitors: National University of Singapore, Shandong University, and A*STAR Institute of Microelectronics will report on the investigation of 3D MFM (Metal-Ferroelectric-Metal) capacitors featuring 3nm ultra-thin HZO with orientation-controlled ALD-TiN electrodes. ALD-deposited TiN/HZO/TiN stack exhibited $2P_r$ at ultra-low operation voltage, with $2P_r$ >38μC/cm^2 at 0.5V and $2P_r$ >28μC/cm^2 at 0.4V. Even at a reduced operation voltage of 0.4V, the results showed that it remains on track to satisfy the International Roadmap for Devices and Systems (IRDS) $2P_r$ target (≥26.5μC/cm^2). ***(Paper T5.3, "Record $2P_r$ (>38μC/cm^2 at 0.5 V, >28μC/cm^2 at 0.4V) of 3D MFM Capacitors Enabled by 3nm HZO and ALD-TiN Orientation Engineering, Y. Feng et al, Shandong University")***



Figures: (**Left**) TEM images together with FFT and EDX analyses of a fabricated 3D trench MFM capacitor (depth: 500nm; opening diameter: 125nm). (**Right**) Measured P_r-V characteristics loops of a 3nm HZO-based 3D trench FE capacitor annealed at 450°C with optimized TiN orientation.

Sensors, Imagers, IoT, MEMS, Display Circuits

Sony RGB-IR Image Sensor: Sony proposes a 2.1-µm RGB-IR CMOS image sensor with sequential operation combining rolling shutter (RS) and global-shutter (GS) modes for in-cabin applications. As an RGB sensor, they achieved a dynamic range (DR) of 112dB at T_j=85°C, enabling high-quality visible imaging. For the IR sensor, state-of-the-art characteristics with 65% modulation transfer function (MTF) and 35% infrared quantum efficiency (IR-QE), facilitating gaze detection under IR illumination. Furthermore, the IR sensor achieved superior performance, featuring an MTF of 65% and an IR-QE of 35%. ***(Paper T5.5, "A 2.1-µm Pixel-Pitch CMOS Image Sensor with 65% MTF/35% QE IR Global Shutter and RGB Rolling Shutter Sequential Operation for In-cabin Applications," M. Hiroki, Sony Semiconductor)***

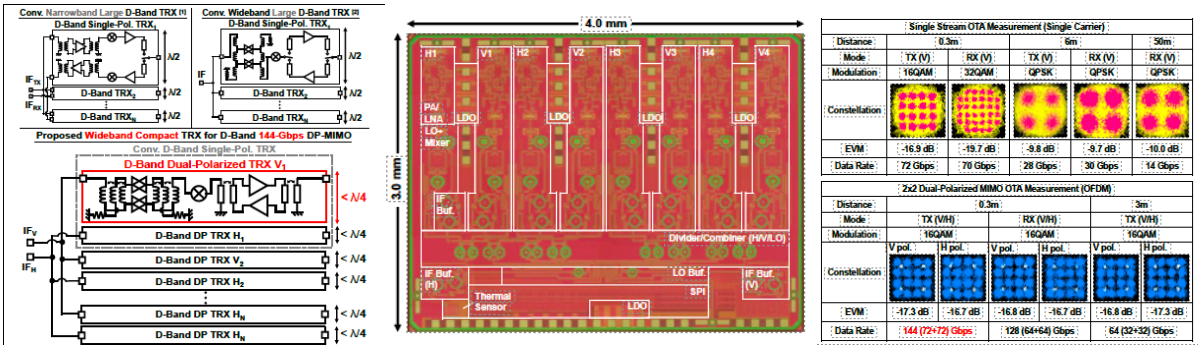


Item		Data
Common	Supply Voltage	3.3V/1.8V/1.1V
	Pixel Pitch	2.1 µm
	Pixel Array	2593×1945
	Conversion Gain (HCG, LCG)	177 µV/e⁻, 34.5 µV/e⁻
RGB	FWC at T_j=85 °C	13 ke⁻
	Sensitivity (3200K with IR cut filter)	15,800 e⁻/lx/s
	Random Noise at T_j=85 °C	0.96 e⁻rms
	Dynamic Range at T_j=85 °C	112 dB
IR	FWC(GS) at T_j=85 °C	5 ke⁻
	QE	35%
	MTF at Nyquist/2	65%

Figures: (**Left**) The proposed sensor's pixel schematic and structures. RGB filters also have IR sensitivity. (**Middle**) The SNR curves of RGB frame at T_j=85 °C, achieving a DR of 112dB. (**Right**) Good pixel performance was achieved in both RGB and IR.

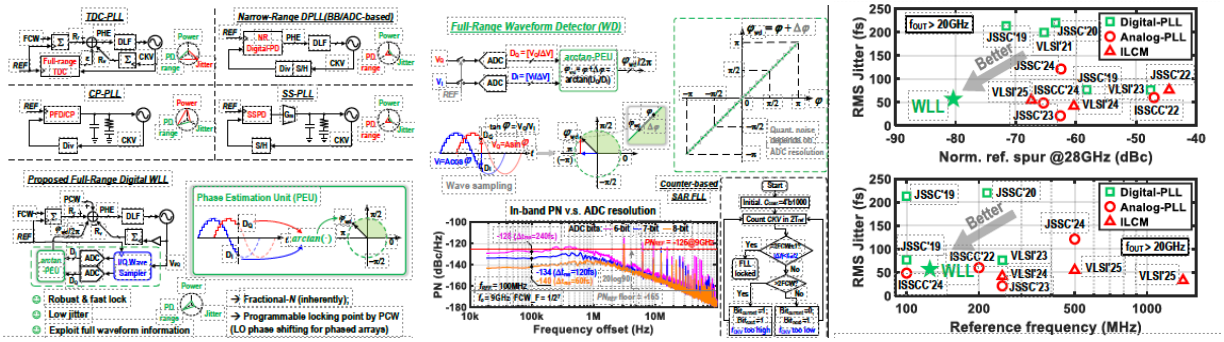
Circuits Highlights

D-Band Dual-Polarized MIMO Phased-Array Transceiver for 6G UE: Institute of Science Tokyo will present the world's first D-band dual-polarized (DP) MIMO phased-array transceiver for 6G user equipment in 65nm CMOS. Each IC integrates four vertical- and four horizontal-polarized TRX elements in a compact 3mm × 4mm die, while an antenna-in-package module with two ICs enables 8V+8H-element operation. The transceiver achieves a maximum data rate of 144Gbps in DP-MIMO operation at 0.3m, 64Gbps at 3m, and long-distance single-stream communication up to 50m, demonstrating a highly integrated and power-efficient sub-THz solution for future 6G mobile devices. ***(Paper C1.5, "A 144Gbps D-Band Dual-Polarized MIMO High-Density Phased-Array Transceiver in 65nm CMOS for 6G UE," 22Yudai Yamazaki et al, Institute of Science Tokyo)***



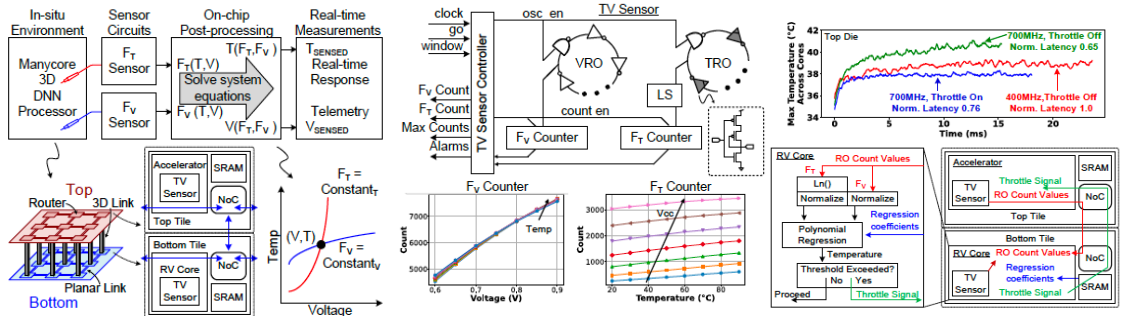
Figures: (Left) Proposed D-band DP-MIMO phased-array architecture highlighting compact λ/4 TRX integration for vertical and horizontal polarizations. **(Middle)** Die micrograph of the 65nm CMOS transceiver integrating 4V+4H TRX elements in a 3mm × 4mm chip. **(Right)** Measured OTA performance demonstrating up to 144Gbps DP-MIMO data rate and long-range communication capability.

28GHz Digital Wave-Locked Loop with Integrated LO Phase Shifting: University College Dublin will present a 28GHz quadrature digital wave-locked loop that achieves ultra-low jitter, low reference spur, and fast locking while directly supporting LO phase shifting for mm-wave phased arrays. The waveform-based detector uses I/Q sampling and arctangent-based phase estimation to provide full-2π monotonic detection with high resolution, enabling 57.2fs$_{rms}$ jitter at 27.375GHz and −80.6dBc reference spur. In addition, the prototype demonstrates a full 360° LO phase-shifting range with 2.8125° resolution and ±1.5GHz frequency hopping with lock times below 0.59µs, pointing to an attractive synthesizer architecture for highly integrated mm-wave MIMO systems. ***(Paper C4.4, "A 28-GHz Quadrature LO-Phase-Shifting Digital Wave-Locked Loop (WLL) Achieving 57.2-fs$_{rms}$ Jitter, −80.6-dBc Spur$_{ref}$, and 0.59µs Near-Integer Lock Time," Feifan Hong et al, University College Dublin)***



Figures: (Left) Conceptual comparison of conventional PLL architectures and the proposed waveform-based digital WLL. **(Middle)** Arctangent-based waveform detector enabling full-2π phase detection with high resolution. **(Right)** Comparison of jitter performance vs normalized ref. spur at 28GHz, and vs. ref. frequency for SoTA PLLs.

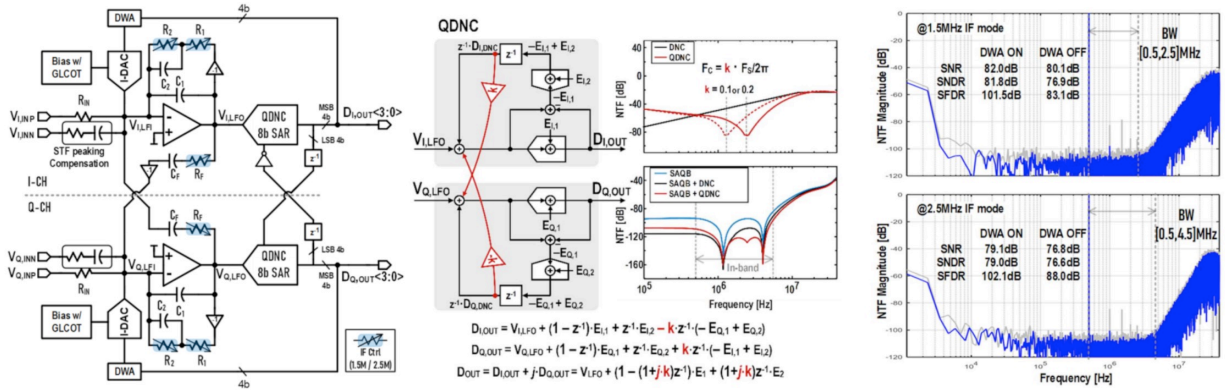
Unified Digital Thermal-Voltage Sensor for Advanced 3DICs: Intel will present a unified digital thermal-voltage sensor for thermal management in Intel 18A and Intel 3, implemented in a hybrid-bonded 3DIC DNN processor with sensor spacing below 216µm. Using two digitally implemented ring oscillators with different voltage and temperature sensitivities, the sensor achieves inaccuracies of 3.1°C/2.1mV in Intel 18A and 1.9°C/1.3mV in Intel 3 through a high-volume-manufacturing calibration flow based on principal component analysis. Intel also demonstrated an aging compensation scheme that restores end-of-life accuracy close to the fresh condition, as well as real-time thermal telemetry and per-core throttling that reduced DNN workload latency by 24%, highlighting a practical monitoring and control solution for dense 3D AI processors. ***(Paper C10.5, "Unified Digital Thermal-Voltage Sensor for Thermal Management in Intel 18A/Intel 3," Shanshan Xie et al, Intel Corporation)***



Figures: (Left) Placement of distributed thermal-voltage sensors in a hybrid-bonded 3DIC DNN processor. **(Middle)** Unified digital TV sensor architecture based on dual ring oscillators and on-chip processing. **(Right)** Measured system-level impact showing real-time thermal monitoring and dynamic throttling for improved performance and thermal control.

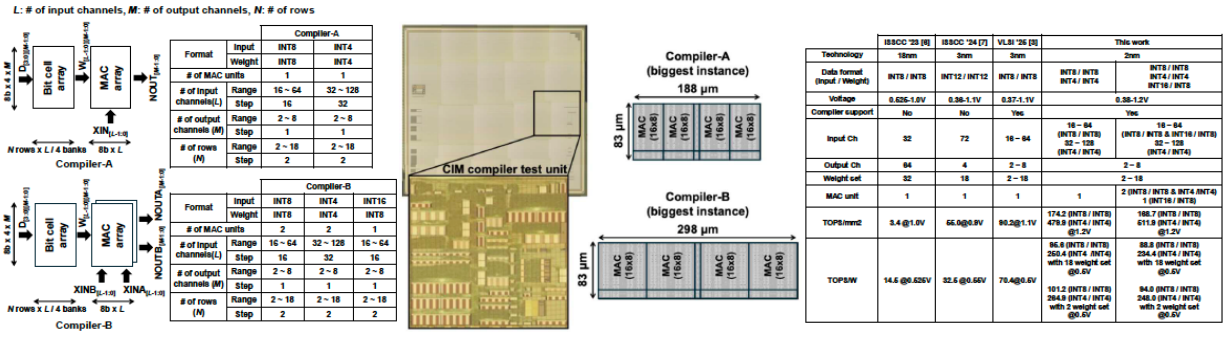
Robust Low-IF Quadrature CT ΔΣ Modulator in 14nm FinFET: Samsung Electronics will presenta configurable low-IF quadrature continuous-time delta-sigma modulator in 14nm FinFET for 1.5MHz and 2.5MHz IF operation, targeting 2MHz and 4MHz bandwidth modes. The design combines a single-

amplifier quadrature biquad with a proposed quadrature digital noise coupling technique to realize sixth-order noise shaping with improved robustness against process variation. Fabricated in 14nm FinFET, the prototype achieves peak FoMs of 175.2dB and 175.4dB for the two operating modes, while measurements from 50 chips show performance variation confined within ±3dB, demonstrating a highly robust and compact ADC solution for advanced Bluetooth low-IF receivers. ***(Paper C28.5, "Robust Configurable 1.5MHz / 2.5MHz IF Quadrature CT ΔΣ Modulator Using SAQB and QDNC for 175.4dB FoMs in 14nm FinFET," Seong-Eun Cho et al, Samsung Electronics)***



Figures: (Left) Proposed quadrature CT ΔΣ modulator architecture using SAQB and digital noise coupling. **(Middle)** Quadrature digital noise coupling (QDNC) mechanism enabling flexible IF operation and robust high-order noise shaping. **(Right)** Measured output spectra showing high SNDR and effective in-band noise suppression for both IF modes.

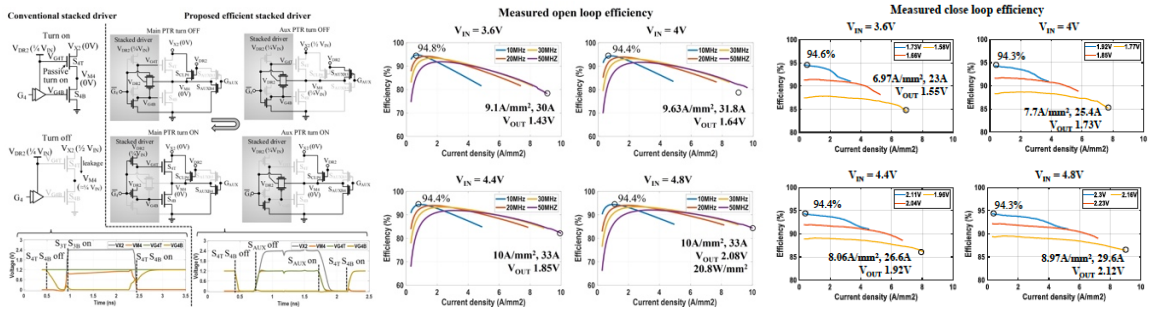
2nm Digital Compute-in-Memory Compiler with Flexible Data Formats: TSMC will present a 2nm digital compute-in-memory compiler supporting multiple MAC units per weight and multiple data formats, including INT8/INT8, INT4/INT4, and INT16/INT8 operation. Implemented in nanosheet technology, the test chip demonstrated V_{MIN} below 0.38V, energy efficiency up to 234.4TOPS/W at 0.5V, and compute density up to 511.9TOPS/mm² at 1.2V. By enabling flexible data-format support together with compiler-level configurability and improved hardware utilization, this work highlights a highly scalable path for efficient AI edge computing in advanced logic nodes. ***(Paper C8.1, "A 2nm 234.4TOPS/W and 511.9TOPS/mm² Digital Computing-in-Memory Compiler with Multiple MAC Units per Weight and Multiple Data Format Support," Hidehiro Fujiwara et al, TSMC)***



Figures: (Left) Overview of the 2nm CIM compiler supporting multiple data formats and multiple MAC units per weight. **(Middle)** 2nm test chip including the CIM complier test unit. **(Right)** Performance comparison demonstrating state-of-the-art energy efficiency and compute density up to 234.4 TOPS/W and 511.9 TOPS/mm².

Power Management Devices and Circuits

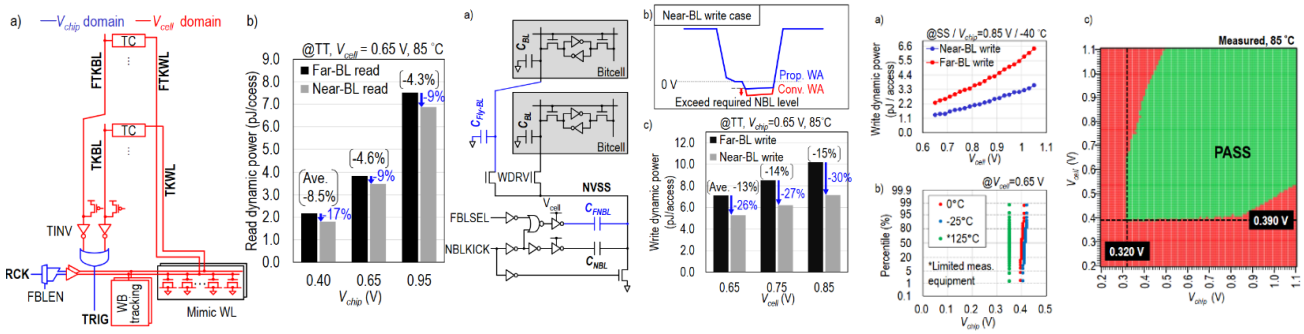
Intel Switched-Capacitor Voltage Regulator: Intel will present a monolithic first stage 2-1 switched-capacitor voltage regulator (SCVR) pushing SoC package V_{IN} to 4.8V. It features stacked devices with synchronized auxiliary power converters, realizing self-generated drive voltages, efficient gate driving and safe startup, achieving 20W/mm2 power density and 94.8% peak efficiency. ***(Paper C2.1, "A Monolithic 20W/mm² 4.8V Input 94.8% Peak Efficiency 2-1 Switched Capacitor Voltage Regulator as First-Stage Current Multiplier for Vertical Power Delivery," M. Gong et al, Intel)***



Figures: (**Left**) Comparison between conventional and proposed stacked-devices gate driving scheme. (**Middle**) Measured open-loop efficiency. (**Right**) Measured closed-loop efficiency.

Memory Technologies, Devices, Circuits, and Architectures

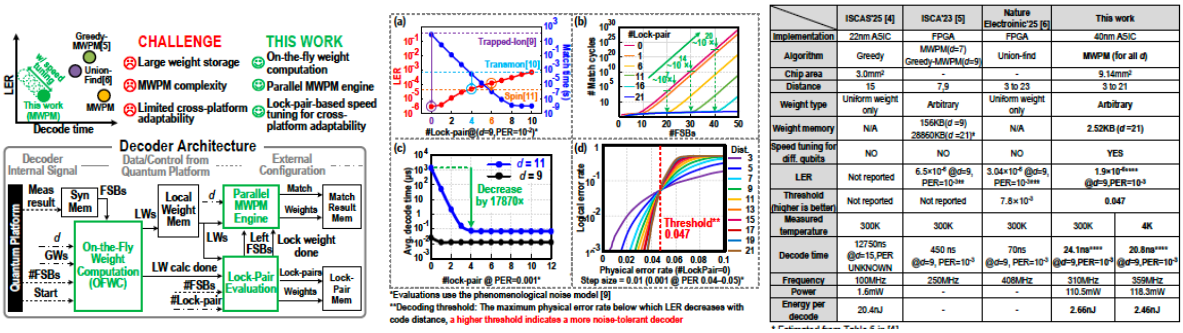
TSMC 2nm Dual-Rail SRAM: TSMC will demonstrate an energy-efficient high-density (HD) 6T single-port SRAM employing row-access aware read tracking and write assist (WA) circuits. In the read operation, the dynamic power is reduced by up to 8.7%, and 8.5% on average, thanks to the row-access aware read tracking and its optimal wordline (WL) deactivating timing. In the write operation, up to 15% dynamic power on average is reduced. 539kbit dual-rail multi-array SRAM macros are demonstrated in 2nm nanosheet technology, achieving a bit-density of 37.42Mbit/mm², a 0.35 − 1.10V low voltage operation at 125°C, and an energy-efficient read/write operation with 2.28pJ/access. ***(Paper C29.1, "A 2nm 37.4 Mbit/mm² Dual-Rail SRAM with Row-Access Aware Read Tracking and Write Assist Circuits Enabling 2.28pJ/Access Energy Efficient Operation," R. Takamatsu et al, TSMC)***



Figures: (**Left**) Proposed row-access aware read tracking, a) schematic, b) read dynamic power comparison between near- and far-BL read. (**Middle**) Proposed row-access aware WA circuit and its impact on write dynamic power, a) schematic, b) NBL waveforms, c) write power comparison for near- and far-BL. (**Right**) Measured silicon data, a) measured write dynamic power, b) V_{min} distribution, c) V_{chip} vs. V_{cell} shmoo plot.

Devices and Accelerators For ML/DL and New Compute

Universities Collaborate to Investigate Cryo-CMOS Surface Code Decoder: Southern University of Science and Technology and Kochi University of Technology will report on the investigation of a cryo-CMOS surface code decoder supporting full-MWPM (minimum-weight perfect matching) up to distance 21. The design employs on-the-fly weight computation to reduce the weight memory area by 989×, a parallel matching engine for full MWPM, and lock-pair-based speed tuning for cross-platform speed adaptability. The 40nm test chip achieves a logical error rate of 1.9×10 -6 with a 20.8ns decode time at 4K, providing a 3.3× to 612× speedup over prior art while consuming 2.46nJ per decode. ***(Paper C7.3, "A Full-MWPM Surface Code Decoder with On-the-Fly Weight Computation and Cross-Platform Adaptability Achieving 1.9×10^{-6} LER and 20.8-ns Decode Time at 4K," H. Lyu and Y. Chen et al, Southern University of Science and Technology)***



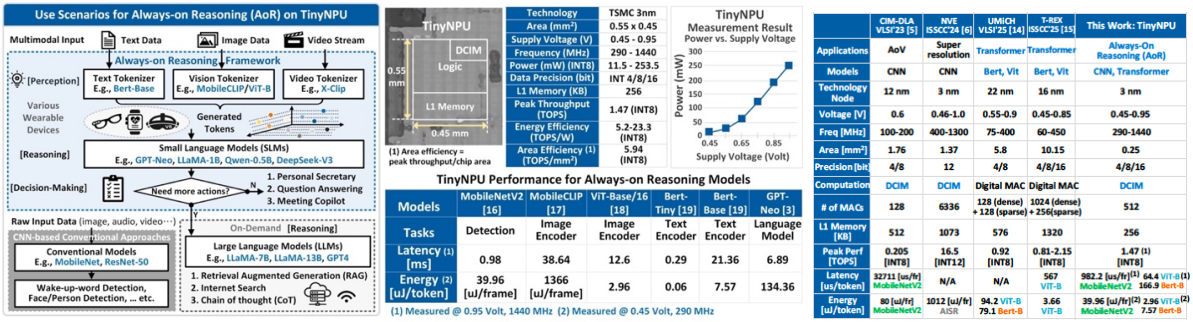
	ISCAS'25 [4]	ISCA'23 [5]	Nature Electronic'25 [6]	This work	
Implementation	22nm ASIC	FPGA	FPGA	40nm ASIC	
Algorithm	Greedy	MWPM(d=7) Greedy-MWPM(d=9)	Union-find	MWPM (for all d)	
Chip area	3.0mm²	-	-	9.14mm²	
Distance	15	7,9	3 to 23	3 to 21	
Weight type	Uniform weight only	Arbitrary	Uniform weight only	Arbitrary	
Weight memory	N/A	156KB(d =9) 28860KB(d =21)*	N/A	2.52KB (d =21)	
Speed tuning for diff. qubits	NO	NO	NO	YES	
LER	Not reported	6.5×10^{-6} @d=9, PER=10^{-3}**	3.04×10^{-6} @d=9, PER=10^{-3}**	1.9×10^{-6}*** @d=9,PER=10^{-3}	
Threshold (higher is better)	Not reported	Not reported	7.8×10^{-3}	0.047	
Measured temperature	300K	300K	300K	300K	4K
Decode time	12750ns @d=15,PER UNKNOWN	450 ns @d=9, PER=10^{-3}	70ns @d=9, PER=10^{-3}	24.1ns**** @d=9,PER=10^{-3}	20.8ns**** @d=9,PER=10^{-3}
Frequency	100MHz	250MHz	408MHz	310MHz	359MHz
Power	1.6mW	-	-	110.5mW	118.3mW
Energy per decode	20.4nJ	-	-	2.66nJ	2.46nJ

Figures: (**Left**) Key advantages and overall architecture of the proposed decoder. (**Middle**) Measured lock-pair-based speed tuning (a); match cycles versus number of FSBs (b); decoding time (c); decoding threshold (d). (**Right**) Performance summary and comparison with state-of-the-arts.

Processors and SoCs

MediaTek Inc. Tiny NPU: MediaTek will present the first commercial 3nm digital computing-in-memory (DCIM) NPU for ultra-low-power always-on reasoning (AoR) in wearables. It delivers

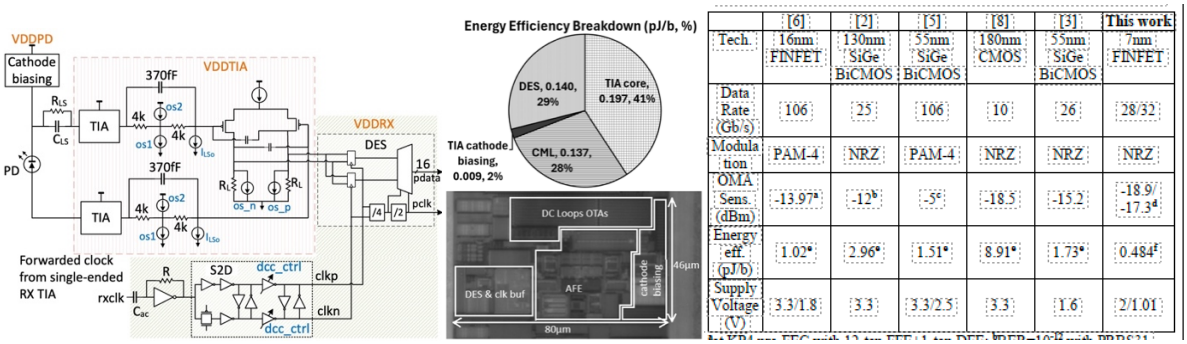
1.47TOPS with 512 8-bit MACs and 256KB on-chip memory. Measurement results show up to 10 days of battery life on smart glasses and 31.8× less energy on transformer models vs state-of-the-art works, enabling efficient next-generation AoR. ***(Paper C21.1, "TinyNPU: A 3nm 0.06-134.36 µJ/token DCIM-Based Ultra Low Power NPU for Always-On Reasoning on Wearables," Y. Hsieh, E. Chang, C. Teng et al, MediaTek)***



Figures: (**Left**) TinyNPU use scenarios. (**Middle**) Chip micrograph and measured TinyNPU performance. (**Right**) Performance summary and comparison with state-of-the-arts.

Wireline and Optical Transceivers, Optical Interconnects and Processors

NVIDIA Optical Receiver: NVIDIA will present a 32Gb/s optical receiver that utilizes a differential transimpedance amplifier (TIA) from a single supply in a 3D-stacked silicon photonics (SiPh) platform. The receiver sensitivity (in terms of Optical Modulation Amplitude or OMA) at the photodiode (PD) is -17.3dBm and -18.9dBm at 32Gb/s and 28Gb/s, respectively. The energy efficiency at 32Gb/s is 0.484pJ/b. The receiver consists of a 7nm FinFET CMOS electronic IC (EIC) stacked on top of a 65nm silicon photonics IC (PIC) via Cu-Cu hybrid bonding. ***(Paper C20.2, "A 32Gb/s Optical Receiver utilizing a Differential TIA with -17.3dBm Sensitivity in a3D-stacked Silicon Photonics Platform," G. Kalogerakis et al, NVIDIA)***



	[6]	[2]	[5]	[8]	[3]	This work
Tech.	16nm FINFET	130nm SiGe BiCMOS	55nm SiGe BiCMOS	180nm CMOS	55nm SiGe BiCMOS	7nm FINFET
Data Rate (Gb/s)	106	25	106	10	26	28/32
Modulation	PAM-4	NRZ	PAM-4	NRZ	NRZ	NRZ
OMA Sens. (dBm)	-13.97[a]	-12[b]	-5[c]	-18.5	-15.2	-18.9/ -17.3[d]
Energy eff. (pJ/b)	1.02[e]	2.96[e]	1.51[e]	8.91[e]	1.73[e]	0.484[f]
Supply Voltage (V)	3.3/1.8	3.3	3.3/2.5	3.3	1.6	2/1.01

Figures: (**Left**) Proposed receiver circuit diagram with the differential TIA. (**Middle**) Chip micrograph and energy efficiency breakdown. (**Right**) Performance summary and comparison with state-of-the-arts.

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