This is a list of accepted papers with their session numbers. The titles have not had the html edited out. This will be taken care of before the full program is posted.

ID#: 3 Session #: C17.2
A uW Output Power, >100V, Single-Capacitor Switched DC-DC Up/Down Converter, Rohit Rothe, University of Michigan, Ann Arbor

ID#: 9 Session #: C20.4
A &[Delta]-Based Spike Sorting SoC with End-to-End Implementation of Event-Driven Binary Autoencoder Neural Network in Analog CIM Achieving 94.54% Accuracy and 3.11&[mu]W/Ch, Edward Choi*, Korea Advanced Institute of Science and Technology

ID#: 12 Session #: T10.1
A Novel Phase Change Material RF Switch with 16nm Technology to Achieve Low Voltage and Low Ron*Coff for mmWave, Hung-Ju Li, TSMC, Taiwan

ID#: 22 Session #: C18.3
Synthesizable 10-bit Stochastic TDC Using Common-Mode Time Dithering and Passive Approximate Adder With 0.012mm² Active Area in 12nm FinFET, Qiaochu Zhang, University of Southern California

ID#: 25 Session #: C7.3
A Stochastic Analog SAT Solver in 65nm CMOS Achieving 6.6&[mu]s Average Solution Time with 100% Solvability for Hard 3-SAT Problems, Qiaochu Zhang, University of Southern California

ID#: 28 Session #: T4.5
a-IGZO FETs with High Current and Remarkable Stability for Vertical Channel Transistor(VCT) DRAM Applications, Younjin Jang, Samsung Advanced Institute of Technology

ID#: 29 Session #: C24.2
A 16GS/s 10b Time-domain ADC using Pipelined-SAR TDC with Delay Variability Compensation and Background Calibration Achieving 153.8dB FoM in 4nm CMOS, Juzheng Liu, University of Southern California

ID#: 34 Session #: C22.3
A 20Gb/s/pin Single-Ended PAM-4 Transceiver with Pre/Post-Channel Switching Jitter Compensation and DQS-Driven Biasing for Low-Power Memory Interfaces, Kyunghwan Min, Samsung Electronics

ID#: 43 Session #: T2.1
HZO-based Nonvolatile SRAM Array with 100% Bit Recall Yield and Sufficient Retention Time at 85 ^{&[deg]}C, Yusuke Shuto, Sony Semiconductor Solutions Corp.

ID#: 48 Session #: T7.1
A New Industry Standard Compact Model Integrating TCAD into SPICE, Sanghoon Myung, Samsung Electronics

ID#: 50 Session #: C23.1
SPIRIT: A Seizure Prediction SoC with a 17.2nJ/cls Unsupervised Online-Learning Classifier and Zoom Analog Frontends, Adelson Chua, University of California, Berkeley

ID#: 52 Session #: C21.4
730-790mA/mm² 48V-to-1V Integrated Hybrid DC-DC Converters based on a Star-Delta Switching Network with 5x/8x Duty Expansion, Chen Kong Teh, Toshiba Electronic Devices & Storage Corporation

ID#: 100 Session #: C2.2

A Monolithic GaN-based Gate Driver for LLC-SRC with Three-Phase Startup Clamping Achieving 23.2&[mu]A I_Q and 98.6% Peak Efficiency, Chi-Yu Chen, EE, National Yang Ming Chiao Tung University

ID#: 103 Session #: C5.1
A 15.4ppm/&[deg]C GaN-based Voltage Reference with Process-Variation-Immunity and High PSR for EV Power Systems, Po-Jui Chiu, EE, National Yang Ming Chiao Tung University

ID#: 106 Session #: C6.1
3D-Stacked 1Megapixel Time-Gated SPAD Image Sensor with 2D Interactive Gating Network for Image Alignment-Free Sensor Fusion, Kazuhiro Morimoto, Canon Inc.

ID#: 114 Session #: T4.4
Highly Enhanced Memory Window of 17.8V in Ferroelectric FET with IGZO Channel via Introduction of Intermediate Oxygen-deficient Channel and Gate Interlayer, Sijung Yoo, Samsung Advanced Institute of Technology

ID#: 121 Session #: T6.5
A Metal Dual Work-function Gate (MDWG) for the continuous scaling of DRAM Cell Transistors, Junsoo Kim, Samsung Electronics

ID#: 126 Session #: C25.1
A 5.6&[mu]W 10-Keyword End-to-End Keyword Spotting System Using Passive-Averaging SAR ADC and Sign-Exponent-Only Layer Fusion with 92.7% Accuracy, Sungjin Park, Seoul National University

ID#: 129 Session #: C3.5
A 278-514M Event/s ADC-Less Stochastic Compute-In-Memory Convolution Accelerator for Event Camera, Jiyue Yang, University of California, Los Angeles

ID#: 131 Session #: C19.1
An On-Chip Current-Sink-Free Adaptive-Timing Power Impedance Measurement (PIM) Unit for 3D-IC in 5nm FinFET Technology, Tsung-Che Lu, TSMC

ID#: 133 Session #: C11.1
A 0.9V Rail-to-Rail Ultra-Low-Power Fully Integrated Clock Generator Achieving 23fJ/Cycle in 28nm CMOS, Sander Derksen, NXP Semiconductors

ID#: 136 Session #: C1.3
A 56-Gb/s 17-mW NRZ Receiver in 0.018 mm², Kshitiz Tyagi, University of California Los Angeles

ID#: 139 Session #: C2.1
A Monolithic Low-I_{LEAK} Cross-Coupled GaN Driver with &[Delta]&[Phi]-Reduced EMI-Rejecter for 21.51dB&[mu]V-EMI-Reduction and 1/10x filter-capacitor, Shi-Jun Zeng, EE, National Yang Ming Chiao Tung University

ID#: 146 Session #: C2.4
A &[plusmn]100A Auto-Calibration Current Sensor with 80V Pulse-Width Modulation Attenuation and 0.15% Gain Error, Yu-Teng Liang, EE, National Yang Ming Chiao Tung University

ID#: 150 Session #: C7.1
Onyx: A 12nm 756 GOPS/W Coarse-Grained Reconfigurable Array for Accelerating Dense and Sparse Applications, Kalhan Koul, Stanford University

ID#: 160 Session #: JFS6.4

A 41.7TOPS/W@INT8 Computing-in-Memory Processor with Zig-Zag Backbone-Systolic CIM and Block/Self-Gating CAM for NN/Recommendation Applications, Zhuoyu Dai, Institute of Microelectronics of the Chinese Academy of Sciences

ID#: 164 Session #: T3.2
EOT scaling via 300mm MX₂ dry transfer - Steps toward a manufacturable process development and device integration., Souvik Ghosh, IMEC

ID#: 169 Session #: C7.4
Occamy: A 432-Core 28.1 DP-GFLOP/s/W 83% FPU Utilization Dual-Chiplet, Dual-HBM2E RISC-V-based Accelerator for Stencil and Sparse Linear Algebra Computations with 8-to-64-bit Floating-Point Support in 12nm FinFET, Gianna Paulin, ETH Zurich, Switzerland

ID#: 173 Session #: C10.2
A 28nm 4.35TOPS/mm2 Transformer Accelerator with Basis-vector Based Ultra Storage Compression, Decomposed Computation and Unified LUT-assisted Cores, Chen Tang, Tsinghua University

ID#: 183 Session #: C29.4
A 5GHz Fractional-N PLL with 97fs_{rms} Jitter and -255.3dB FoM, Zhiqiang Huang, The Hong Kong University of Science and Technology (Guangzhou)

ID#: 185 Session #: C1.1
A 246-fJ/b 13.3-Tb/s/mm Single-Ended Current-Mode Transceiver with Crosstalk Cancellation for Shield-Less Short-Reach Interconnect, Jaeho Lee, POSTECH

ID#: 195 Session #: C11.2
A 94fs_{rms}-Jitter and &[minus]249.3dB FoM 4.0GHz Ring-Oscillator-based MDLL with Background Calibration of Phase Offset and Injection Slope Mismatch, Dongjun Park, POSTECH

ID#: 199 Session #: JFS1.2
A 140-Gbps 1-to-21GHz Ultra-Wideband LNA Achieving 1.95-to-3dB NF Using Gm-Assisted-Feedback Noise Suppression Technique in 40nm Bulk CMOS, Sicheng Han, Fudan University

ID#: 215 Session #: C5.2
A 97.3dB SNR Bioimpedance AFE with -84dB THD Segmented-&[Delta]&[Sigma]M Sinusoidal Current Generator and Passing-Through Instrumentation Amplifier, Qinjing Pan, Fudan University, Shanghai, China

ID#: 218 Session #: C1.5
A 0.88pJ/bit 112Gb/s PAM4 Transmitter with 1V_{ppd} Output Swing and 5-Tap Analog FFE in 7nm FinFET CMOS, Zeynep Toprak Deniz, IBM Reserach

ID#: 219 Session #: JFS6.1
State-Independent Low Resistance Drift SiSbTe Phase Change Memory for Analog In-Memory Computing Applications, HUAI-YU CHENG, Macronix International Co., Ltd.

ID#: 238 Session #: C16.2
A 3nm Fin-FET 19.87-Mbit/mm² 2RW Pseudo Dual-port 6T SRAM with High-R Wire Tracking and Sequential Access Aware Dynamic Power Reduction, Tomotaka Tanaka, TSMC Design Technology Japan

ID#: 239 Session #: C25.2
An Area-Efficient True Single-Phase Clocked and Conditional Capture Flip-Flop for Ultra-Low-Power Operations in 7nm Fin-FET Process, Hyunchul Hwang, Samsung Electronics

ID#: 245 Session #: T9.3
Backside Power Delivery with relaxed overlay for backside patterning using extreme wafer thinning and Molybdenum-filled slit nano Through Silicon Vias, Peng Zhao, imec

ID#: 250 Session #: C26.1
A Scalable mK Cryo-CMOS Demultiplexer Chip for Voltage Biasing and High-Speed Control of Silicon Qubit Gates, Sushil Subramanian, Intel Corporation

ID#: 251 Session #: T12.5
Bit-cost-scalable 3D DRAM Architecture and Unit Cell First Demonstrated with Integrated Gate-around and Channel-around IGZO FETs, Feng-Min Lee, Macronix International Co., Ltd.

ID#: 254 Session #: C3.3
ETCIM: An Error-Tolerant Digital-CIM Processor with Redundancy-Free Repair and Run-Time MAC and Cell Error Correction, Yiqi Wang, Tsinghua University

ID#: 255 Session #: C7.2
A 52.01TFLOPS/W Diffusion Model Processor with Inter-Time-Step Convolution-Attention-Redundancy Elimination and Bipolar Floating-Point Multiplication, Yubin Qin, Tsinghua University

ID#: 268 Session #: C20.3
A 22nm Nonvolatile AI-Edge Processor with 21.4TFLOPS/W using 47.25Mb Lossless-Compressed-Computing STT-MRAM Near-Memory-Compute Macro, De-Qi You, National Tsing Hua University

ID#: 269 Session #: T3.4
Achieving 1-nm-Scale Equivalent Oxide Thickness Top Gate Dielectric on Monolayer Transition Metal Dichalcogenide Transistors with CMOS-Friendly Approaches, Jung-Soo Ko, Stanford University

ID#: 278 Session #: C24.1
A 12-bit 16GS/s Single-channel RF-DAC with Hybrid Segmentation for Digital Back-off and Code-dependent Free Switch Driver achieving -85dBc IMD3 in 5nm FinFET, Byeongwoo Koo, Samsung Electronics

ID#: 279 Session #: C24.4
A 12-bit 10GS/s Time-Interleaved SAR ADC with Even/Odd Channel-Correlated Absolute Error-Based Over-Nyquist Timing-Skew Calibration in 5nm FinFET, Junsang Park, Samsung Electronics

ID#: 298 Session #: C18.5
A Single-Channel, 1-GS/s, 10.91-ENOB, 81-dB SFDR, 9.2-fJ/conv.-step, Ringamp-Based Pipelined ADC with Background Calibration in 16nm CMOS, Jorge Lagos, imec

ID#: 299 Session #: TFS2.3
Backside power distribution for nanosheet technologies beyond 2nm, Ruilong Xie, IBM

ID#: 301 Session #: C8.3
A Beyond-the-rail Audio CTDSM with a Passive Input Stage and 99.2dB SNDR, Shenyang Li, Delft University of Technology

ID#: 308 Session #: C5.4
Current Mirrors with Tapered Stacked-Gates for Area Saving or Noise Improvement in 3nm FinFET Process, Chu-En Hsia, Taiwan Semiconductor Manufacturing Company

ID#: 310 Session #: C15.3

A Smart Contact Lens System with 433MHz Wireless Power and Data Transfer at a Modulation Index Down to 0.02%, Heesung Roh, POSTECH

ID#: 316 Session #: T5.1
Product Performance Aware 3rd Generation GAA Platform Transistor Design with Extreme Small Local Layout Effect and Transistor Variation, Dongchan Jeong, Samsung Electronics

ID#: 319 Session #: C16.1
An Offset-Compensated Charge-Transfer Pre-Sensing Bit-Line Sense-Amplifier for Low-Voltage DRAM, Kyeongtae Nam, Samsung Electronics

ID#: 322 Session #: C17.4
A 0.6-1 V VIN Soft-Switching Low Dropout Regulator With 31.3 A/mm2 Current Density, 99.99% Current Efficiency, and 2.04 fs FoM, Jeongmyeong Kim, KAIST

ID#: 324 Session #: C21.1
A 96.4%-Efficiency Single-Duty-Cycled Buck-Boost Converter Achieving 1.9mV Ripple and 2.1mV Mode-Change Fluctuation for Mobile OLED Displays, Jae-Hyun Kim, KAIST

ID#: 327 Session #: T11.4
First Experimental Demonstration of Self-aligned Flip FET (FFET): a Breakthrough Stacked Transistor Technology with 2.5T Design, Dual-side Active and Interconnects, Haoran Lu, School of Integrated Circuits, Peking University, Beijing, China

ID#: 328 Session #: C15.2
A 2000-Volumes/s 3D Ultrasound Imaging Chip with Monolithically-Integrated 11.7x23.4mm² 2048-Element CMUT Array and Arbitrary-Wave TX Beamformer, Nuriel Rozsa, Delft University of Technology

ID#: 329 Session #: C2.5
A 12V-to-1V 100A Inverted Pyramid Trans-Inductor Voltage Regulator Converter with 93.6% High Efficiency and Fast Transient Response, Yu-Chen Kuo, EE, National Yang Ming Chiao Tung University

ID#: 333 Session #: C12.2
A 450&[micro]W@50fps Wake-Up Module Featuring Auto-Bracketed 3-Scale Log-Corrected Pattern Recognition and Motion Detection in a 1.5Mpix 8T Global Shutter Imager, Arnaud Verdant, CEA Leti

ID#: 337 Session #: T7.4
Unlimited Bi-directional Back-Bias in FD-SOI Technology With New Dual Isolation Integration, Remy Berthelon, STMicroelectronics

ID#: 339 Session #: C8.2
A 470&[mu]W, 102.6dB-DR, 20kHz BW calibration-free &[Delta]&[Sigma] Modulator with SFDR in excess of 110dBc using an Intrinsically Linear 13-Level DAC, Matteo Dalla Longa, Infineon Technologies Austria AG

ID#: 340 Session #: TFS2.2
A Design Methodology for Back-side Power and Clock Routing Co-Optimization, Pruek Vanna-iampikul, Georgia Institute of Technology

ID#: 341 Session #: C4.2
A Current-Source-Free Constant-Current Wireless Adiabatic Neural Stimulator Achieving a 5.5-27.7x Improved RF-to-Electrode Stimulation Efficiency Factor, Siddharth Agarwal, University of California, San Diego, La Jolla, CA

ID#: 349 Session #: C21.2

A 1.8V-Input 0.2-to-1.5V-Output 2.5A 930mA/mm³ Always-Balanced Dual-Path Hybrid Buck Converter with Seamlessly All-VCR-Coverable Tri-Mode Operation, Dae-Hyeon Kim, KAIST

ID#: 358 Session #: T6.4
Up to 57% Reduction in Effective Resistivity of Word Lines of 3D-NAND Memory by Grain-size Control, Material Selection, and Seam Removal, Hiroshi Terada, Tokyo Electron Ltd.

ID#: 373 Session #: T7.3
Assessment of the transient self-heating effect and its impact on the performance of Watt-level RF power amplifier in a FinFET technology, Thanh Viet Dinh, NXP Semiconductors

ID#: 378 Session #: C16.3
A 7GHz High-Bandwidth 1R-1RW SRAM for Arm HPC Processor in 3nm Technology, Rahul Mathur, Arm

ID#: 381 Session #: T17.4
Cell to Core-Periphery Overlap (C2O) based on BCAT for next generation DRAM, Kiseok Lee, DRAM Technology Development, Samsung Electronics Co. Ltd.

ID#: 382 Session #: C14.1
A 0.296pJ/bit 17.9Tb/s/mm² Die-to-Die Link in 5nm/6nm FinFET on a 9&[mu]m-pitch 3D Package Achieving 10.24Tb/s Bandwidth at 16Gb/s PAM-4, Mu-Shan Lin, TSMC

ID#: 384 Session #: T14.1
Concatenated Continuous Driving for Extending Lifetime of Spin Qubits towards a Scalable Silicon Quantum Computer, Takuma Kuno, Hitachi, Ltd.

ID#: 398 Session #: C5.3
A 5.8W, 0.00086% THD+N, 118dB PSRR Class-D Audio Amplifier with Passive Output Common-Mode Compensation Technique for Wide Output Power Range, Inhwan Cho, Samsung Electronics

ID#: 399 Session #: T6.3
Mechanical Stress Effects on Dielectric Leakage and Interconnection Integrity in 3D NAND Flash Memory, Se Hoon Lee, Samsung Electronics Co., Ltd.

ID#: 400 Session #: T15.2
Revealing Mechanism of Non-accumulative Disturb and Approach Toward Disturb Suppression in HZO/Si FeFET Memory, Masaki Otomo, The University of Tokyo

ID#: 409 Session #: T6.2
Innovative Barrier Metal-less Metal Gate Scheme leading to Highly Reliable Cell Characteristics for 8th Generation 512Gb 3D NAND Flash Memory, Hang-Ah Park, Samsung Electronics Co., Ltd.

ID#: 410 Session #: C24.3
A 5nm 60GS/s 7b 64-way Time Interleaved Partial loop unrolled SAR ADC achieving 34dB SNDR up to 32GHz, Claudio Nani, Marvell, Pavia

ID#: 415 Session #: C12.3
A 430-&[mu]A 68.2-dB-SNR 133-dBSPL-AOP CMOS-MEMS Digital Microphone based on Electrostatic Force Feedback Control, Qi Zhang, Zhejiang University

ID#: 419 Session #: C16.5

A 14nm 128Mb eMRAM Implemented with 17.88Mb/mm2 at 0.60V for Auto-G1 Applications, Gyuseong Kang, Foundry Business, Samsung Electronics

ID#: 425 Session #: JFS4.3
A Subcellular-Resolution Multimodal CMOS Biosensor Array with 16K Ion-Selective Pixels for Real-Time Monitoring Potassium Dynamics, Hangxing Liu, ETH Zürich

ID#: 426 Session #: JFS4.1
Highly Sensitive Multimodal CMOS Antifouling Sensor Array with Multi-Use Electrodes for Single-Cell-Level Profiling of Biophysical and Biochemical Parameters, Hangxing Liu, ETH Zürich

ID#: 436 Session #: T5.4
Thermal Considerations for Block-Level PPA Assessment in Angstrom Era: A Comparison Study of Nanosheet FETs (A10) & Complementary FETs (A5), Subrat Mishra, IMEC

ID#: 440 Session #: C14.2
A 1.1pJ/b/lane, 1.8Tb/s Chiplet over XSR-MCM Channels using 113Gb/s PAM-4 Transceiver with Signal Equalization and Envelope Adaptation using TX-FFE in 5nm CMOS, Gautam Gangasani, Marvell Technology Inc.

ID#: 444 Session #: JFS3.5
High thermal conductivity AlN films for advanced 3D Chiplets, Takeshi Takagi, The Univ. of Tokyo

ID#: 445 Session #: C13.1
Empowering Local Differential Privacy: A 5718 TOPS/W Analog PUF-based In-Memory Encryption Macro for Dynamic Edge Security, Chih-Sheng Lin, Industrial Technology Research Institute

ID#: 454 Session #: C1.4
A 200-Gb/s PAM-4 transmitter with 1.6-Vppd output swing and clock skew correction in 12-nm FinFET, Boyang Zhang*, Peking University

ID#: 464 Session #: T13.1
71 GHz-f_{max} &[beta]-Ga₂O₃-on-SiC RF power MOSFETs with record P_{out}=3.1 W/mm and PAE=50.8% at 2 GHz, P_{out}= 2.3 W/mm at 4 GHz, and low microwave noise figure, Min Zhou, Xidian University

ID#: 466 Session #: T3.5
Single-crystalline monolayer MoS₂ arrays based high-performance transistors via selective-area CVD growth directly on silicon wafers, Guixu Zhu, University of Science and Technology of China (USTC)

ID#: 467 Session #: T12.2
Ge-doped In2O3: First Demonstration of Utlizing Ge as Oxygen Vacancy Consumer to Break the Mobility/Reliability Tradeoff for High Performance Oxide TFTs, Jiayi Wang, High-Frequency High-Voltage Device and Integrated Circuits R&D Center, Institute of Microelectronics, Chinese Academy of Sciences

ID#: 469 Session #: C18.2
A Low-OSR 5th-Order Noise Shaping SAR ADC Using EF-EF-CIFF Structure with PVT-Robust Differential V-T-V Converter, Yu-Hsiang Huang, National Tsing Hua University

ID#: 470 Session #: C1.2
A 2 &[mult] 56 Gb/s <b style="font-size: 10.5pt; font-family: Century, serif; text-align:, Xuxu Cheng, Southern University of Science and Technology

ID#: 475 Session #: C27.4
E-Textile Battery-Less Walking Step Counting System with <23 pW Power, Dual- Function Harvesting from Breathing, and No High-Voltage CMOS Process, Anil Gundu, National University of Singapore

ID#: 477 Session #: JFS5.1
A 336 x 240 backside-illuminated 3D-stacked 7&[mu]m SPAD for LiDAR sensor with PDE 28% at 940nm and under 0.4% depth accuracy up to 10m, Jaehyung Jang, SK hynix Inc., CIS Development

ID#: 482 Session #: T2.3
In-depth Analysis of the Hafnia Ferroelectrics as a Key Enabler for Low Voltage & QLC 3D VNAND Beyond 1K Layers: Experimental Demonstration and Modeling, Giuk Kim, KAIST

ID#: 485 Session #: C17.5
A 400-ns-Settling-Time Hybrid Dynamic Voltage Frequency Scaling Architecture and Its Application in a 22-Core Network-on-Chip SoC in 12-nm FinFET Technology, Erik Loscalzo, Columbia University

ID#: 492 Session #: T9.1
Integration of Si-Interposer and High Density MIM Capacitor on 2.5D Foveros Face-to-Face Architecture, Chris Pelto, Intel

ID#: 494 Session #: T3.1
Record Performance in GAA 2D NMOS and PMOS using Monolayer MoS₂ and WSe₂ with scaled contact and gate length, Wouter Mortelmans, Intel

ID#: 495 Session #: C6.2
A 512x512 SPAD Laser Speckle Autocorrelation Imager in Stacked 65/40nm CMOS, Robert Henderson, University of Edinburgh

ID#: 502 Session #: T12.1
Overcoming Performance Limitation of IGZO FET by iCVD Fluorine Doping, SEUNG HYUN OH, KAIST

ID#: 504 Session #: JFS5.2
A Temporal Noise Reduction via 40% Enhanced Conversion Gain in Dual-Pixel CMOS Image Sensor with Full-Depth Deep-Trench Isolation and Locally Lowered-Stack Technology, Seunghwan Lee, Samsung Electronics

ID#: 506 Session #: T15.5
Engineering HZO by Flat Amorphous TiN with 0.3nm Roughness Achieving Uniform c-axis Alignment, Record High Breakdown Field (~10nm HZO), and Record Final 2P_r of 56 &[mu]C/cm² with Endurance > 4E12, Zefu Zhao, Graduate Institute of Electronics Engineering, National Taiwan University

ID#: 507 Session #: C28.4
An 11.4mm² 40.2Gbps 17.4pJ/b/iteration Soft-Decision Open Forward Error Correction Decoder for Optical Communication, Cheng-Hsun Lu, University of Michigan

ID#: 511 Session #: C9.3
A -96.5 dBm-Sensitivity, 14 dBm peak power, Self-Interference Resistant IR-UWB Radar Transceiver Supporting Child Presence Detection and Precision Positioning, Hyun-Gi Seok, Samsung Electronics

ID#: 522 Session #: T15.1

Low-Damage Processed and High-Pressure Annealed High-&[kappa] Hafnium Zirconium Oxide Capacitors near Morphotropic Phase Boundary with Record-Low EOT of 2.4&[Aring] & high-&[kappa] of 70 for DRAM Technology, Venkateswarlu Gaddam, KAIST

ID#: 525 Session #: TFS2.1
Expanding Design Technology Co-Optimization Potentials with Back-Side Interconnect Innovation, Byung-Sung Kim, Samsung Electronics

ID#: 527 Session #: C25.4
A Jammer-Mitigating 267Mb/s 3.78mm² 583mW 32x8 Multi-User MIMO Receiver in 22FDX, Florian Bucheli, ETH Zurich

ID#: 531 Session #: C9.1
A 132-to-163 GHz 4TX/4RX Distributed MIMO FMCW Radar Transceiver with Real-time Reference-Clock Synchronization Enabling Cooperative Coherent Multistatic Imaging System, Ruichen Wan, Tsinghua University

ID#: 537 Session #: JFS2.1
NeRF-Navi: A 93.6-202.9&[mu]J/task Switchable Approximate-Accurate NeRF Path Planning Processor with Dual Attention Engine and Outlier Bit-Offloading Core, Seryeong Kim, KAIST

ID#: 543 Session #: C8.4
A 0.38mW 200kHz-BW 92.1dB-DR Single-Opamp 4th-order Continuous-Time Delta-Sigma Modulator with 3rd-order Noise Coupling, Kent Edrian Lozada, Korea Advanced Institute of Science and Technology

ID#: 549 Session #: T5.3
Ge(110) GAA Nanosheet / Si(100) Tri-gate Nanosheet Monolithic CFETs Featuring Record-high Hole Mobility, Seong Kwang Kim, KAIST

ID#: 551 Session #: T17.1
DRAM-peri FinFET – A Thermally-stable High-Performance Advanced CMOS RMG Platform with Mo-based pWFM for sub-10nm DRAM, Jishnu Ganguly, imec

ID#: 555 Session #: T1.5
First Demonstration of Fully Integrated 16 nm Half-Pitch Selector Only Memory (SOM) for Emerging CXL Memory, Myoungsub Kim, R&D, SK hynix Inc.

ID#: 556 Session #: T1.3
A confined storage nitride 3D-NAND cell with WL airgap for cell-to-cell interference reduction and improved program performances, Davide Resnati, Micron Technology, Inc.

ID#: 562 Session #: C26.2
A 0.8V Capacitively-Biased BJT-Based Temperature Sensor with an Inaccuracy of &[plusmn]0.4&[deg]C (3&[sigma]) from -40&[deg]C to 125&[deg]C in 22nm CMOS, Zhong Tang, Vango Technologies, Inc

ID#: 566 Session #: T13.3
Hybrid Integration of 3D-RF Interconnects on AlGaN/GaN/Si HEMT RF Transistor featuring 2.2W/mm P_{sat} & 41% PAE @28GHz using a Robust and Cost-Effective Chiplet Heterogeneous Bonding Technique, Alexis Divay, CEA-Leti

ID#: 567 Session #: TFS1.1
Amorphous Oxide Semiconductors for Monolithic 3D Integrated Circuits, Suman Datta, Georgia Tech

ID#: 573 Session #: C2.3

A Fully Integrated 48-V GaN Driver Using Parallel-Multistep-Series Reconfigurable Switched-Capacitor Bank Achieving 7.7nC/mm² On-Chip Bootstrap Driving Density, Xuchu Mu, University of Macau

ID#: 574 Session #: C14.5
A 800Gb/s Transceiver for PAM-4 Optical Direct-Detection applications in 5nm FinFet Process, Marco Sosio, Marvell Technology

ID#: 575 Session #: T9.5
Material, Process and System Level Analysis for Parasitic Reduction of Next Generation Logic Technology in conjunction with Backside Power Delivery, Ashish Pal, Applied Materials

ID#: 578 Session #: C14.3
A 0.9pj/b 9.8-113Gb/s XSR Serdes with 6-tap TX FFE and AC coupling RX in 3nm FinFet Technology, A. Chowdhury, Marvell Technology, Toronto, Canada

ID#: 580 Session #: C25.3
A Mixed-signal 3D Footstep Planning SoC for Motion Control of Humanoid Robots with Embedded Zero-Moment-Point based Gait Scheduler and Neural Inverse Kinematics, Qiankai Cao, Northwestern University

ID#: 581 Session #: T16.3
Positive to Negative Schottky Barrier Transition in Metal/Oxide Semiconductor Contacts by Tuning Indium Concentration in IGZO, Sumi Lee, Purdue University

ID#: 583 Session #: C13.2
A 4.7-to-5.3Gbps Fault-Injection Attack Resistant AES-256 Engine Using Isomorphic Composite Fields in Intel 4 CMOS , Raghavan Kumar, Intel

ID#: 584 Session #: T8.2
A Vertical Channel-All-Around FeFET with Thermally Stable Oxide Semiconductor Achieving High &[Delta]I_{on} > 2&[mu]A/cell for 3D Stackable 4F² High Speed Memory, Shoichi Kabuyanagi, Kioxia Corporation

ID#: 590 Session #: TFS1.3
Demonstration of On-Chip Switched-Capacitor DC-DC Converters using BEOL Compatible Oxide Power Transistors and Superlattice MIM Capacitors, Sunbin Deng, Georgia Institute of Technology

ID#: 591 Session #: C10.3
A 99.2TOPS/W Transformer Learning Processor with Approximated Attention Score Gradient Computation and Ternary Vector-based Speculation, Ping-Sheng Wu, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan

ID#: 606 Session #: T10.2
14nm FinFET node embedded MRAM technology for automotive non-volatile RAM applications with endurance over 1E12-cycles, Joosung Oh, Samsung Electronics Co., Ltd.

ID#: 616 Session #: TFS2.4
Demonstration of Logic-Block Performance-Power Gain by 1^{_{st}} Generation Back Side Power Delivery Network for SoC and HPC Applications beyond 2nm Node, Hidenobu Fukutome, Samsung Electronics Co., Ltd.

ID#: 622 Session #: C13.3
A 67F2Reconfigurable PUF Using 1T2R RRAM Switching Competition in 28nm CMOS with 5e-9 Bit Error Rate, Yue Cao, Fudan University

ID#: 623 Session #: TFS1.2
P-type SnO Semiconductor Transistor and Application, Chun-Chen Wang, Taiwan Semiconductor Manufacturing Company, Ltd.

ID#: 632 Session #: T15.3
BEOL Compatible Ultra-Low Operating Voltage (0.5 V) and Preconfigured Switching Polarization States in Effective 3 nm Ferroelectric HZO Capacitors, Jiyoung Kim, The University of Texas at Dallas

ID#: 635 Session #: C26.3
A 0.29pJ/step Fully Discrete-Time Charge Domain Bridge-to-Digital Converter for Force Sensing in Spinal Implants Using RC Bridge <br class="t-last-br">, Tim Keller, ETH Zurich

ID#: 636 Session #: C29.3
A 79.3fs_{rms} Jitter Fractional-N Digital PLL Based on a DTC Chopping Technique, Riccardo Moleri, Politecnico di Milano

ID#: 639 Session #: C20.2
A PVT Robust Signed 8-Bit Analog Compute-In-Memory Accelerator with Integrated Activation Functions for AI Applications, Hechen Wang, Intel Labs

ID#: 644 Session #: JFS3.4
Integration and Characterization of High Thermal Conductivity Materials for Heat Dissipation in Stacked Devices, W.-Y. Woon, TSMC

ID#: 645 Session #: C27.2
A 92.8% Power Reduction Event-Driven Dual-Mode Touch Analog Front-End IC Featuring 620&[mu]W Self-Capacitance Sensing and 500fps Mutual-Capacitance Sensing, Jonghang Choi, Sungkyunkwan University

ID#: 659 Session #: C4.4
A Fully Dynamic 1st-Order &[Delta]-&[Delta]&[Sigma] Modulator with a 468mVpp Input Range for Electrical Impedance Tomography Systems, Haidam Choi, KAIST

ID#: 662 Session #: T8.3
A Novel Chalcogenide Based CuGeSe Selector Only Memory (SOM) for 3D Xpoint and 3D Vertical Memory Applications, Wei-Chih Chien, Macronix

ID#: 663 Session #: C10.4
A 22nm 54.94TFLOPS/W Transformer Fine-Tuning Processor with Exponent-Stationary Re-computing, Aggressive Linear Fitting, and Logarithmic Domain Multiplicating, yang wang, Tsinghua University

ID#: 665 Session #: JFS5.3
High-Resolution and Compact Integrated FMCW-LiDAR Chip with 128 Channels of Slow Light Grating Antennas, Yuya Maeda, Sony Semiconductor Solutions Corporation

ID#: 668 Session #: C29.2
A 6.5-to-6.9-GHz SSPLL with Configurable Differential Dual-Edge SSPD Achieving 44-fs RMS Jitter, &[minus]260.7-dB FO<b style="font-size: 1em; text-ali, Tianle Chen, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China

ID#: 671 Session #: C28.3
A 101mW, 280fps Scene Graph Generation Processor for Visual Context Understanding on Mobile Devices, Chun-Wei Chang, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan

ID#: 679 Session #: T13.4
Novel Material, Process and Device Innovations for Next Generation Silicon Carbide (SiC) Trench MOSFET Technology, Pratik B Vyas, Applied Materials Inc.

ID#: 684 Session #: C22.2
A 48-Gb/s Half-Rate PAM4 Optical Receiver with 0.27-pJ/bit TIA Efficiency, 1.28-pJ/bit RX Efficiency, and 0.06-mm² area in 28-nm CMOS, Chongyun Zhang, ECE Department, The Hong Kong University of Science and Technology

ID#: 688 Session #: C16.4
A 3.3GHz 1048X640 Multi-Bank Single-Port SRAM with Frequency Enhancing Techniques and 0.55V-1.35V Wide Voltage Range Operation in 3nm FinFET for HPC Applications, Ming-Chieh Huang, TSMC

ID#: 691 Session #: JFS6.5
Monolithic 3D Integration of Analog RRAM-based Fully Weight Stationary and Novel CFET 2T0C-based Partially Weight Stationary for Accelerating Transformer, H. Yang, School of Integrated Circuits, Tsinghua University

ID#: 692 Session #: T9.2
Mitigating line-break defectivity with a sandwiched TiN or W layer for metal pitch 18 nm aspect ratio 6 semi-damascene interconnects , Anshul Gupta, imec

ID#: 704 Session #: C4.3
A 5.7kfps Fast Neural Electrical Impedance Tomography IC Based on Incremental Zoom Structure with Baseline Cancellation for Peripheral Nerve Monitoring Systems, Ji-Hoon Suh, KAIST

ID#: 712 Session #: C17.3
A 6.78 MHz Wireless Power and Data Transfer System Achieving Simultaneous 52.6% End-to-End Efficiency and 4.0 Mb/s Forward Data Delivery with Interference-Free Rectifier, Quanrong Zhuang, School of Electronic Science and Engineering, Nanjing University, China

ID#: 713 Session #: T13.2
Field Plate and Package Optimization for GaN Devices and Systems, Tz-Wun Wang, EE, National Yang Ming Chiao Tung University

ID#: 721 Session #: C28.2
A Heterogeneous TinyML SoC with Energy-Event-Performance-Aware Management and Compute-in-Memory Two-Stage Event-Driven Wakeup, Yanchi Dong, Peking University

ID#: 730 Session #: T14.4
Photon-mediated charge transport and stability of physically-defined and self-organized germanium quantum dots/SON barriers in few-hole regime at T > 10 K, Chi-Cheng Lai, National Yang Ming Chiao Tung University

ID#: 748 Session #: JFS6.3
An Ultra-low Voltage Auger-Recombination Enhanced Hot Hole Injection Scheme in Implementing a 3 Bits per Cell e-DRAM CIM Macro for Inference Accelerator, T. C. Kao, National Yang Ming Chiao Tung University

ID#: 751 Session #: C8.1
A 97dB-PSRR 178.4dB-FOM_{DR} Calibration-Free VCO-&[Delta]&[Sigma] ADC Using a PVT-Insensitive Frequency-Locked Differential Regulation Scheme for Multi-Channel ExG Acquisition, Sehwan Lee, DGIST

ID#: 754 Session #: T3.3
High Performance Transistor of Aligned Carbon Nanotubes in a Nanosheet Structure, Gregory Pitner, TSMC

ID#: 757 Session #: C4.1
A Wireless Neurostimulator using Body-Coupled Link for Multisite Stimulation in Freely Behaving Animals, Taejune Jeon, Yonsei University

ID#: 763 Session #: T1.2
Highly manufacturable Self-Aigned Direct Backside Contact (SA-DBC) and Backside Gate Contact (BGC) for 3-dimensional Stacked FET at 48nm gate pitch, Jaehyun Park, Samsung Electronics

ID#: 767 Session #: C28.1
Medusa: A 0.83/4.6 &[mu]J/Frame 86/91.6%-CIFAR-10 tinyML Processor with Pipelined Pixel Streaming of Bottleneck Layers in 28nm CMOS , Rohan Doshi, Stanford University

ID#: 778 Session #: JFS3.2
3DIC System-Technology Co-Optimization with a Focus on the Interplay of Thermal, Power, Timing, and Stress Effects <br clear="all">, Victor Moroz, Synopsys

ID#: 780 Session #: C15.5
A 28nm Approximate / Binary 6T CAM for Sequence Alignment, Brian Crafton, Georgia Institute of Technology

ID#: 781 Session #: C10.1
MINOTAUR: An Edge Transformer Inference and Training Accelerator with 12 MBytes On-Chip Resistive RAM and Fine-Grained Spatiotemporal Power Gating, Kartik Prabhu, Stanford University

ID#: 783 Session #: JFS3.3
Package - System Thermal Modeling and New Material, Tsung-Yu Chen, Taiwan Semiconductor Manufacturing Company

ID#: 784 Session #: C9.4
A 28GHz 5G NR Wirelessly Powered Relay Transceiver Using Rectifier-Type 4th-Order Sub-Harmonic Mixer, Sena Kato, Tokyo Institute of Technology

ID#: 785 Session #: T17.5
Single metal BCAT breakthrough to open a new era of 12 nm DRAM and beyond, Kyosuk Chae, Samsung Electronics

ID#: 797 Session #: T14.3
First Demonstration of Superconducting Nb Contact on Heavily-Doped Group IV Semiconductor, Gerui Zheng, National University of Singapore

ID#: 800 Session #: C18.4
A 71.5-dB SNDR 475-MS/s Ringamp-Based Pipelined SAR ADC with On-Chip Bit-Weight Calibration, Chao Chen, State Key Laboratory of Integrated Chips and Systems, Fudan University, Shanghai, China

ID#: 829 Session #: T11.5
3DIC with Stacked FinFET, Inter-level Metal, and Field-Size (25x33mm²) Single-Crystalline Si on SiO₂ by Elevated-Epi, Bo-Jheng Shih, National Yang Ming Chiao Tung University

ID#: 832 Session #: C20.1
Dyamond: A 1T1C DRAM In-memory Computing Accelerator with Compact MAC-SIMD and Adaptive Column Addition Dataflow, Seongyon Hong, KAIST

ID#: 834 Session #: T8.5
Reliable Low-voltage FeRAM Capacitors for High-speed Dense Embedded Memory in Advanced CMOS, Sou-Chi Chang, Intel

ID#: 837 Session #: C27.1
An OLED Display Driver IC Embedding -63dB CMR, 80mV/nA Sensitivity, 390pA Detectable, and Column-Parallel Pixel Current Readout for Real-Time Non-Uniformity Compensation, Gyu-Wan Lim, KAIST

ID#: 838 Session #: T7.5
First Observation of Time Exponent Variations under Positive Bias Stress on a-IGZO Transistors Utilizing Ultrafast On-the-Fly Technique with 1 &[micro]s Delay , TAEWON SEO, POSTECH

ID#: 848 Session #: T15.4
Comprehensive Analysis of Duty-cycle Induced Degradations in Hf_xZr_{1-x}O₂-based Ferroelectric Capacitors: Behavior, Modeling, and Optimization, Guan Feng, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University, Shanghai, 200433, China

ID#: 855 Session #: TFS1.4
First Experimental Demonstration of Hybrid Gain Cell Memory with Si PMOS and ITO FET for High-speed On-chip Memory, Shuhan Liu, Stanford University

ID#: 857 Session #: C13.4
An In-Sensor PUF Featuring Optical Reconfigurability and Near-100% Hardware Reuse Ratio for Trustworthy Sensing, Xiaojin Zhao, Shenzhen University

ID#: 859 Session #: T6.1
Fluorine-free Word Line Molybdenum Process for Enhancing Scalability and Reliability in 3D Flash Memory, Takashi Fukushima, Kioxia Corporation

ID#: 860 Session #: C21.3
A 5.4V-Vin, 9.3A/mm² 10MHz Buck IVR Chiplet in 55nm BCD Featuring Self-Timed Bootstrap and Same-Cycle ZVS Control, Harish Krishnamurthy, Intel Corporation

ID#: 869 Session #: C15.4
An Intra-Body-Power-Transfer System Energized by an Electromagnetic Energy Harvester for Powering Wearable Sensor Nodes, Hyungjoo Cho, KAIST

ID#: 877 Session #: C12.4
A 1.5 V 132 dBSPL AOP Digital Readout Circuit for MEMS Microphone Using Self-Adaption Loop, Ling Wang, Key Laboratory of Analog Integrated Circuits and Systems (Ministry of Education), School of Integrated Circuits, Xidian University

ID#: 879 Session #: T14.2
Single-power-supply compatible cryogenic In_{0.8}Ga_{0.2}As quantum-well HEMTs with record combination of high-frequency and low-noise performance for quantum-computing applications, Ji-Hoon Yoo, Kyungpook National University

ID#: 880 Session #: C9.2
A 640-Gb/s 4&[mult]4-MIMO D-Band CMOS Transceiver Chipset, Chenxin Liu, Tokyo Institute of Technology

ID#: 895 Session #: C15.1
A 76&[mult]55 X-Ray Energy Binning Dosimeter for Closed-Loop Cancer Radiotherapy, Rahul Lall, University of California, Berkeley

ID#: 903 Session #: C17.1

A Monolithic 5.7A/mm² 91% Peak Efficiency Scalable Multi-Stage Modular Switched Capacitor Voltage Regulator with Self-Timed Deadtime and Safe Startup for 3D-ICs, Jingshu Yu, Intel Labs

ID#: 911 Session #: T16.5
A Novel Method for Extracting Asymmetric Source and Drain Resistance in IGZO Vertical Channel Transistors, Sungwon Yoo, Semiconductor R&D Center, Samsung Electronics

ID#: 915 Session #: JFS4.4
A Pulsed Electrochemistry Readout IC with Slew-rate Booting Technique and Phase-domain Δ&[Sigma] ADC for Si-Nanowire Electrical Double-layer Capacitance Measurement, Po-Hsun Chu, National Yang Ming Chiao Tung University

ID#: 917 Session #: JFS1.3
First Heterogeneous and Monolithic 3D (HM3D) Integration of InGaAs HEMTs and InP/InGaAs DHBTs on Si CMOS for Next-Generation Wireless Communication, Nahyun Rheem, KAIST

ID#: 919 Session #: C23.2
A Highly-Integrated 1536-Channel Quad-Shank Monolithic Neural Probe in 55nm CMOS for Full-Band Raw-Signal Recording, Xiaolin Yang, imec

ID#: 922 Session #: C6.4
A 7.2inch 5.5Mpixel 600mW SPAD X-ray Detector with 116.7 dB Dynamic Range, Byungchoul Park, Yonsei University

ID#: 924 Session #: C22.4
A 2&[mult]112 Gb/s 0.34 pJ/b/lane Single-Ended PAM4 Receiver with Multi-Order Crosstalk Cancellation and Signal Reutilization Technique in 28-nm CMOS, Liping Zhong, Southern University of Science and Technology

ID#: 936 Session #: JFS1.1
First Radio-Frequency Circuits fabricated in top-tier of a full 3D Sequential Integration Process at mmW for 5G applications, Jose Lugo-Alvarez, CEA-Leti

ID#: 943 Session #: C3.4
A 28nm 4170-TFLOPS/W/b and 195-TFLOPS/mm²/b Multiply-Free Fully-Digital Floating-Point Compute-In-Memory Macro with Mitchell's Approximation, Ruiqi Guo, Tsinghua University

ID#: 945 Session #: T16.4
Fluorine Plasma Treatment-Enabled ITO Transistors: Excellent Reliability and Comprehensive Understanding of Temperature Dependence from 77 K to 375 K, Xuanqi Chen, National University of Singapore

ID#: 953 Session #: C19.2
Scalable Embedded Multi-Die Active Bridge (S-EMAB) Chips with Integrated LDOs for Low-Cost Programmable 2.5D/3.5D Packaging Technology, Wei Lu, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

ID#: 955 Session #: C23.5
A 16-Ch CMI-Tolerant Neural AFE with Inherent CM Detection and Shared CM Suppression Achieving 0.006mm²/Ch and 3.1&[micro]W/Ch , Joan Aymerich, imec

ID#: 959 Session #: C19.4
A Customizable Killo-core Processor Architecture by Reusable Chiplets with Low-latency High-flexibility Die-to-Die Interconnection, Yujie Wang, Institute of Computing Technology, Chinese Academy of Sciences

ID#: 961 Session #: T7.2

Hot-Carrier-Degradation Characterization for Accurate End-of-Life Prediction with 3nm GAA Logic Technology Featuring Multi-Bridge-Channel FET, Seongkyung Kim, Samsung Electronics

ID#: 970 Session #: T8.1
Highly Scalable Vertical Bypass RRAM (VB-RRAM) for 3D V-NAND Memory , Geonhui Han, POSTECH

ID#: 971 Session #: C24.5
A 10GS/s Hierarchical Time-Interleaved ADC for RF-sampling applications, Nereo Markulic, imec

ID#: 972 Session #: T10.3
Extremely scaled perpendicular SOT-MRAM array integration on 300mm wafer, Farrukh Yasin, imec

ID#: 974 Session #: TFS2.5
Backside Power Delivery in High Density and High Performance Context: IR-drop and Block-level Power-Performance-Area Benefits, Yun Zhou, imec

ID#: 976 Session #: T11.1
V_t Fine-Tuning in Multi-V_t Gate-All-Around Nanosheet nFETs using Rare-Earth Oxide-based Dipole-First Gate Stack Compatible with CFET Integration, Hiroaki Arimura, imec

ID#: 979 Session #: T11.3
Breakthrough processes for Si CMOS devices with BEOL compatibility for 3D sequential integrated More than Moore analog applications, Daphnée Bosch, Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France

ID#: 989 Session #: C26.4
A 0.72nW, 0.006mm2 32kHz Crystal Oscillator with Adaptive Sub-Harmonic Pulse Injection from -40&[deg]C to 125&[deg]C in 22nm FDSOI, Yingjie Zhu, Southern University of Science and Technology

ID#: 992 Session #: T1.4
On the extreme scaling of transistors with monolayer MoS2 channel, Terry Hung, TSMC

ID#: 997 Session #: C23.3
A 79.2dB-SNDR Slope-Adaptive Dynamic Zoom-and-Track Incremental &[Delta]&[Sigma] Neural Recording Frontend with Resolution-Preservative 192mV/ms Transient Tracking, Sungjin Oh, University of Michigan

ID#: 1003 Session #: C13.5
A 65nm Delta-Sigma ADC based VDD-Variation-Tolerant Power-Side-Channel-Attack Monitor with Detection Capability down to 0.25&[Omega], Shota Konno, Asahi Kasei Microdevices Corporation

ID#: 1004 Session #: C23.4
A 3072-Channel Neural Readout IC with Multiplexed Two-Step Incremental-SAR Conversion and Bulk-DAC-Based EDO Compensation in 22nm FDSOI, Xiaohua Huang, imec

ID#: 1005 Session #: JFS4.2
A 65nm Neuromorphic Bio-signal Encoder with Compute-in-Entropy Architecture 7.13nJ Privacy-preserving Encoding and 2.38Mb/mm² Encoding Memory Density , Boyang Cheng, University of Notre Dame

ID#: 1012 Session #: T2.4
Unveiling Cryogenic Performance (4 to 300 K) towards Ultra-thin Ferroelectric HZO: Novel Kinetic Barrier Engineering and Underlying Mechanism <br clear="all">, Dong Zhang, Department of Electrical and Computer Engineering, National University of Singapore (NUS), 117576, Singapore

ID#: 1017 Session #: T9.4

Toward 0 V ESD protection in 2.5D/3D advanced bonding technology, SHIH-HSIANG LIN, imec

ID#: 1029 Session #: T10.4
First demonstration of high retention energy barriers and 2 ns switching, using magnetic ordered-alloy-based STT MRAM devices, Matthias Gottwald, IBM

ID#: 1034 Session #: C29.1
A 9-GHz Subsampling-Chopper PLL with Charge-Share Cancelling and Achieving 57.8-fs-rms Jitter with 15dB In-band Noise Improvement, Xiangjian Kong, Guangdong University of Technology

ID#: 1035 Session #: C6.3
A Digital Dynamic Vision Sensor with SPAD pixels and Multi-Event Generation for Motion/Vibration-Adaptive Detection, Houk Lee*, Sungkyunkwan University

ID#: 1039 Session #: T16.2
Positive Bias Stress Measurement Guideline and Band Analysis for Evaluating Instability of Oxide Semiconductor Transistors, Qi Jiang, Stanford University

ID#: 1043 Session #: T5.2
Monolithic Complementary Field Effect Transistors (CFET) demonstrated using Middle Dielectric Isolation and Stacked Contacts, Steven Demuynck, imec

ID#: 1047 Session #: T4.3
Enhancement of In₂O₃ Field-Effect Mobility Up To 152 cm²&[middot]V⁻¹&[middot]s⁻¹ Using HZO-Based Higher-k Linear Dielectric, Zehao Lin, Purdue University

ID#: 1054 Session #: C12.1
23,000-Exposures/s 360fps-Readout Software-Defined Image Sensor with Motion-Adaptive Spatially Varying Imaging Speed, Roberto Rangel, University of Toronto

ID#: 1055 Session #: T11.2
Replacement Metal Gate Process Extendible Beyond 2 nm Node with Superior Gate Conductivity, Naomi Yoshida, Applied Materials

ID#: 1057 Session #: C22.5
A 4.6pJ/b 64Gb/s Transceiver Enabling PCIe 6.0 and CXL 3.0 in Intel 3 CMOS Technology, Dong-Myung Choi, Intel Corporation

ID#: 1063 Session #: T12.4
A Dual-Gate Vertical Channel IGZO Transistor for BEOL Stackable 3D Parallel Integration for Memory and Computing Applications, Ziyi Liu, School of Integrated Circuits, ICFC, BNRist, Tsinghua University, Beijing, China.

ID#: 1065 Session #: C8.5
A 10.8GS/s, 84MHz-BW RF Bandpass &[Sigma]&[Delta] ADC with a 89dB-SFDR and a 62dB-SNDR for LTE/5G Receivers, Alhassan Sayed, Seamless Waves

ID#: 1068 Session #: C11.4
A 3.2GHz-15GHz Low Jitter Resonant Clock Featuring Rotary Traveling Wave Oscillators in Intel 4 CMOS for 3D Heterogeneous Multi-Die Systems, Vinayak Honkote, Intel Corporation

ID#: 1072 Session #: C14.4
A 4x50Gb/s NRZ 1.5pJ/b Co-Packaged and Fiber-Terminated 4-Channel Optical RX, Sashank Krishnamurthy, Intel Corporation

ID#: 1091 Session #: C11.3
A 25.4-27.5 GHz Ping-Pong Charge-Sharing Locking PLL Achieving 42 fs Jitter with Implicit Reference Frequency Doubling, Sayan Kumar, University College Dublin

ID#: 1092 Session #: JFS6.2
Cost-effective LLM accelerator using processing in memory technology, hyungdeok Lee, SK hynix

ID#: 1093 Session #: C3.2
FSNAP: An Ultra-Energy-Efficient Few-Spikes-Neuron based Reconfigurable SNN Processor Enabling Unified On-Chip Learning and Accuracy-Driven Adaptive Time-Window Tuning, Ruixin Mao, University of Electronic Science and Technology of China

ID#: 1094 Session #: T12.3
First Demonstration of Monolithic Three-dimensional Integration of Ultra-high Density Hybrid IGZO/Si SRAM and IGZO 2T0C DRAM Achieving Record-low Latency (<10ns), Record-low Energy (<10fJ) of Data Transfer and Ultra-long data retention (>5000s, Menggan Liu, Laboratory of Microelectronic Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences(CAS)

ID#: 1096 Session #: T17.2
4F² Stackable Polysilicon Channel Access Device for Ultra-Dense NVDRAM, Albert Liao, Micron

ID#: 1098 Session #: T16.1
Unveiling the Impact of AC PBTI on Hydrogen Formation in Oxide Semiconductor Transistors, Gan Liu, National University of Singapore

ID#: 1114 Session #: C22.1
A 256Gbps Microring-based WDM Transceiver with Error-free Wide Temperature Operation for Co-packaged Optical I/O Chiplets, Pavan Bhargava, Ayar Labs

ID#: 1116 Session #: T1.1
An Intel 3 Advanced FinFET Platform Technology for High Performance Computing and SOC Product Applications, Walid Hafez, Intel

ID#: 1140 Session #: C18.1
A 100kHz-BW 99dB-DR Continuous-Time Tracking-Zoom Incremental ADC with Residue-Gain Switching and Digital NC-FF, Ye-Dam Kim, KAIST

ID#: 1151 Session #: T4.2
Scaling Potential of Nanosheet Oxide Semiconductor FETs for Monolithic 3D Integration - ALD Material Engineering, High-Field Transport, Statistical Variability, Kaito Hikake, Institute of Industrial Science, The University of Tokyo

ID#: 1155 Session #: T2.2
Polar axis orientation control of hafnium-based ferroelectric capacitors with in-situ AC electric bias during rapid thermal annealing, Zhaomeng Gao, East China Normal University

ID#: 1165 Session #: T4.1
Highly Robust All-Oxide Transistors with Ultrathin In₂O₃ as Channel and Thick In₂O₃ as Metal Gate Towards Vertical Logic and Memory , Zehao Lin, Purdue University

ID#: 1180 Session #: JFS5.4
A 30fps 64 &[mult] 64 CMOS Flash LiDAR Sensor with Push-Pull Analog Counter Achieving 0.1% Depth Uncertainty at 70m Detection Range, Dongseok Cho, Yonsei University

ID#: 1184 Session #: C19.3
A 32Gb/s 0.36pJ/bit 3nm Chiplet IO using 2.5D CoWoS Package with Real-Time and Per-Lane CDR and Bathtub Monitoring , John Ma, Marvell Technology Group

ID#: 1191 Session #: T8.4
First Demonstration of BEOL-Compatible Vertical Fe-NOR, Yang Feng, Department of Electrical and Computer Engineering, National University of Singapore (NUS), 117576, Singapore

ID#: 1224 Session #: TFS1.5
On the Reliability of High-Performance Dual Gate (DG) W-doped In₂O₃ FET, Khandker Akif Aabrar, Georgia Institute of Technology

ID#: 1226 Session #: C3.1
122.7 TOPS/W Stdcell-Based DNN Accelerator Based on Transition Density Data Representation, Clock-Less MAC Operation, Pseudo-Sparsity Exploitation in 40 nm, Animesh Gupta, National University of Singapore

ID#: 1232 Session #: JFS2.2
CogniVision: End-to-End SoC for Always-on Smart Vision with mW Power in 40nm, Animesh Gupta, National University of Singapore

ID#: 1254 Session #: C27.3
A 0.9-2.6pW 0.1-0.25V 22nm 2-bit Supply-to-Digital Converter Using Always-Activated Supply-Controlled Oscillator and Supply-Dependent-Activation Buffers for Bio-Fuel-Cell-Powered-and-Sensed Time-Stamped Bio-Recording, Hiroaki Kitaike, Kyoto University

ID#: 1261 Session #: JFS3.1
Co-Optimization for Robust Power Delivery Design in 3D-Heterogeneous Integration of Compute In-Memory Accelerators, Madison Manley, Georgia Institute of Technology

ID#: 1316 Session #: JFS1.4
Terahertz Sensing with CMOS-RFIC - Feasibility Verification for Short-Range Imaging using 300GHz MIMO Radar -, Ichiro Somada, Mitsubishi Electric Corp.

ID#: 1317 Session #: JFS2.3
A Quad-Core AI Processing Unit for Generative AI in 4nm 5G Smartphone SoC, Chien-Hung Lin, MediaTek Inc.

ID#: 1318 Session #: JFS2.4
AMD Instinct&[trade] MI300X Accelerator: Packaging and Architecture Co-Optimization , Alan Smith, AMD

ID#: 1322 Session #: T17.3
A Three Dimensional DRAM (3D DRAM) Technology for the Next Decades, Joodong Park, SKhynix

ID#: 1323 Session #: C9.5
A 28GHz 4-Stream Time-Division MIMO Phased-Array Receiver Utilizing Nyquist-Rate Fast Beam Switching for 5G and Beyond, Yi Zhang, Tokyo Institute of Technology