This is a list of accepted papers with their session numbers. The titles have not had the HTML edited out. This will be taken care of before the full program is posted.

**ID#: 3 Session #: C17.2**
A uW Output Power, &#62;100V, Single-Capacitor Switched DC-DC Up/Down Converter, Rohit Rothe, University of Michigan, Ann Arbor

**ID#: 9 Session #: C20.4**
A &Delta;-Based Spike Sorting SoC with End-to-End Implementation of Event-Driven Binary Autoencoder Neural Network in Analog CIM Achieving 94.54% Accuracy and 3.11[W/Ch, Edward Choi*, Korea Advanced Institute of Science and Technology

**ID#: 12 Session #: T10.1**
A Novel Phase Change Material RF Switch with 16nm Technology to Achieve Low Voltage and Low Ron*Coef for mmWave, Hung-Ju Li, TSMC, Taiwan

**ID#: 22 Session #: C18.3**
Synthesizable 10-bit Stochastic TDC Using Common-Mode Time Dithering and Passive Approximate Adder With 0.012mm² Active Area in 12nm FinFET, Qiaochu Zhang, University of Southern California

**ID#: 25 Session #: C7.3**
A Stochastic Analog SAT Solver in 65nm CMOS Achieving 6.6μs Average Solution Time with 100% Solvability for Hard 3-SAT Problems, Qiaochu Zhang, University of Southern California

**ID#: 28 Session #: T4.5**
a-IGZO FETs with High Current and Remarkable Stability for Vertical Channel Transistor(VCT) DRAM Applications, Younjin Jang, Samsung Advanced Institute of Technology

**ID#: 29 Session #: C24.2**
A 16GS/s 10b Time-domain ADC using Pipelined-SAR TDC with Delay Variability Compensation and Background Calibration Achieving 153.8dB FoM in 4nm CMOS, Juzheng Liu, University of Southern California

**ID#: 34 Session #: C22.3**
A 20Gb/s/pin Single-Ended PAM-4 Transceiver with Pre/Post-Channel Switching Jitter Compensation and DQS-Driven Biasing for Low-Power Memory Interfaces, Kyunghwan Min, Samsung Electronics

**ID#: 43 Session #: T2.1**
HZO-based Nonvolatile SRAM Array with 100% Bit Recall Yield and Sufficient Retention Time at 85°C, Yusuke Shuto, Sony Semiconductor Solutions Corp.

**ID#: 48 Session #: T7.1**
A New Industry Standard Compact Model Integrating TCAD into SPICE, Sanghoon Myung, Samsung Electronics

**ID#: 50 Session #: C23.1**
SPIRIT: A Seizure Prediction SoC with a 17.2nJ/cls Unsupervised Online-Learning Classifier and Zoom Analog Frontends, Adelson Chua, University of California, Berkeley

**ID#: 52 Session #: C21.4**
48V-to-1V Integrated Hybrid DC-DC Converters based on a Star-Delta Switching Network with 5x/8x Duty Expansion, Chen Kong Teh, Toshiba Electronic Devices & Storage Corporation

**ID#: 100 Session #: C2.2**
A Monolithic GaN-based Gate Driver for LLC-SRC with Three-Phase Startup Clamping Achieving 23.2 µA I<sub>Q</sub> and 98.6% Peak Efficiency, Chi-Yu Chen, EE, National Yang Ming Chiao Tung University

ID#: 103  Session #: C5.1
A 15.4ppm/°C GaN-based Voltage Reference with Process-Variation-Immunity and High PSR for EV Power Systems, Po-Jui Chiu, EE, National Yang Ming Chiao Tung University

ID#: 106  Session #: C6.1
3D-Stacked 1Megapixel Time-Gated SPAD Image Sensor with 2D Interactive Gating Network for Image Alignment-Free Sensor Fusion, Kazuhiro Morimoto, Canon Inc.

ID#: 114  Session #: T4.4
Highly Enhanced Memory Window of 17.8V in Ferroelectric FET with IGZO Channel via Introduction of Intermediate Oxygen-deficient Channel and Gate Interlayer, Sijung Yoo, Samsung Advanced Institute of Technology

ID#: 121  Session #: T6.5
A Metal Dual Work-function Gate (MDWG) for the continuous scaling of DRAM Cell Transistors, Junsoo Kim, Samsung Electronics

ID#: 126  Session #: C25.1
A 5.6 &mu;W 10-Keyword End-to-End Keyword Spotting System Using Passive-Averaging SAR ADC and Sign-Exponent-Only Layer Fusion with 92.7% Accuracy, Sungjin Park, Seoul National University

ID#: 129  Session #: C3.5
A 278-514M Event/s ADC-Less Stochastic Compute-In-Memory Convolution Accelerator for Event Camera, Jiyue Yang, University of California, Los Angeles

ID#: 131  Session #: C19.1
An On-Chip Current-Sink-Free Adaptive-Timing Power Impedance Measurement (PIM) Unit for 3D-IC in 5nm FinFET Technology, Tsung-Che Lu, TSMC

ID#: 133  Session #: C11.1
A 0.9V Rail-to-Rail Ultra-Low-Power Fully Integrated Clock Generator </b> </b>Achieving 23fJ/Cycle in 28nm CMOS</b>, Sander Derksen, NXP Semiconductors

ID#: 136  Session #: C1.3
A 56-Gb/s 17-mW NRZ Receiver in 0.018 mm<sup>2</sup>, Kshitiz Tyagi, University of California Los Angeles

ID#: 139  Session #: C2.1
A Monolithic Low-&leak Cross-Coupled GaN Driver with &Delta;&Phi;-Reduced EMI- Rejecter for 21.51dB&mu;V-EMI-Reduction and 1/10x filter-capacitor, Shi-Jun Zeng, EE, National Yang Ming Chiao Tung University

ID#: 146  Session #: C2.4
A &plasmn;100A Auto-Calibration Current Sensor with 80V Pulse-Width Modulation Attenuation and 0.15% Gain Error, Yu-Teng Liang, EE, National Yang Ming Chiao Tung University

ID#: 150  Session #: C7.1
Onyx: A 12nm 756 GOPS/W Coarse-Grained Reconfigurable Array for Accelerating Dense and Sparse Applications, Kalhan Koul, Stanford University

ID#: 160  Session #: JFS6.4
A 41.7TOPS/W@INT8 Computing-in-Memory Processor with Zig-Zag Backbone-Systolic CIM and Block/Self-Gating CAM for NN/Recommendation Applications, Zhuoyu Dai, Institute of Microelectronics of the Chinese Academy of Sciences

ID#: 164  Session #: T3.2
<b>EOT scaling via 300mm MX dry transfer - Steps toward a manufacturable process development and device integration.</b>, Souvik Ghosh, IMEC

ID#: 169  Session #: C7.4
Occamy: A 432-Core 28.1 DP-GFLOP/s/W 83% FPU Utilization Dual-Chiplet, Dual-HBM2E RISC-V-based Accelerator for Stencil and Sparse Linear Algebra Computations with 8-to-64-bit Floating-Point Support in 12nm FinFET, Gianna Paulin, ETH Zurich, Switzerland

ID#: 173  Session #: C10.2
<b>A 28nm 4.35TOPS/mm2 Transformer Accelerator with Basis-vector Based Ultra Storage Compression, Decomposed Computation and Unified LUT-assisted Cores</b>, Chen Tang, Tsinghua University

ID#: 183  Session #: C29.4
A 5GHz Fractional-N PLL with 97fs rms Jitter and -255.3dB FoM, Zhiqiang Huang, The Hong Kong University of Science and Technology (Guangzhou)

ID#: 185  Session #: C1.1
A 246-fl/b 13.3-Tb/s/mm Single-Ended Current-Mode Transceiver with Crosstalk Cancellation for Shield-Less Short-Reach Interconnect, JaeHo Lee, POSTECH

ID#: 195  Session #: C11.2
A 94fs rms Jitter and -249.3dB FoM 4.0GHz Ring-Oscillator-based MDLL with Background Calibration of Phase Offset and Injection Slope Mismatch, Dongjun Park, POSTECH

ID#: 199  Session #: JFS1.2
A 140-Gbps 1-to-21GHz Ultra-Wideband LNA Achieving 1.95-to-3dB NF Using Gm-Assisted-Feedback Noise Suppression Technique in 40nm Bulk CMOS, Sicheng Han, Fudan University

ID#: 215  Session #: C5.2
A 97.3dB SNR Bioimpedance AFE with -84dB THD Segmented-[Delta]-[Sigma]M Sinusoidal Current Generator and Passing-Through Instrumentation Amplifier, Qinjing Pan, Fudan University, Shanghai, China

ID#: 218  Session #: C1.5
<b>A 0.88pJ/bit 112Gb/s PAM4 Transmitter with 1Vppd 5-Tap Analog FFE in 7nm FinFET CMOS</b>, Zeynep Toprak Deniz, IBM Research

ID#: 219  Session #: JFS6.1
State-Independent Low Resistance Drift SiSbTe Phase Change Memory for Analog In-Memory Computing Applications, HUAI-YU CHENG, Macronix International Co., Ltd.

ID#: 238  Session #: C16.2
A 3nm Fin-FET 19.87-Mbit/mm 2RW Pseudo Dual-port 6T SRAM with High-R Wire Tracking and Sequential Access Aware Dynamic Power Reduction, Tomotaka Tanaka, TSMC Design Technology Japan

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ID#: 245  Session #: T9.3
Backside Power Delivery with relaxed overlay for backside patterning using extreme wafer thinning and Molybdenum-filled slit nano Through Silicon Vias, Peng Zhao, imec

ID#: 250  Session #: C26.1
A Scalable mK Cryo-CMOS Demultiplexer Chip for Voltage Biasing and High-Speed Control of Silicon Qubit Gates, Sushil Subramanian, Intel Corporation

ID#: 251  Session #: T12.5
Bit-cost-scalable 3D DRAM Architecture and Unit Cell First Demonstrated with Integrated Gate-around and Channel-around IGZO FETs, Feng-Min Lee, Macronix International Co., Ltd.

ID#: 254  Session #: C3.3
ETCIM: An Error-Tolerant Digital-CIM Processor with Redundancy-Free Repair and Run-Time MAC and Cell Error Correction, Yiqi Wang, Tsinghua University

ID#: 255  Session #: C7.2
A 52.01TFLOPS/W Diffusion Model Processor with Inter-Time-Step Convolution-Attention-Redundancy Elimination and Bipolar Floating-Point Multiplication, Yubin Qin, Tsinghua University

ID#: 268  Session #: C20.3
A 22nm Nonvolatile AI-Edge Processor with 21.4TFLOPS/W using 47.25Mb Lossless-Compressed-Computing STT-MRAM Near-Memory-Compute Macro, De-Qi You, National Tsing Hua University

ID#: 269  Session #: T3.4
Achieving 1-nm-Scale Equivalent Oxide Thickness Top Gate Dielectric on Monolayer Transition Metal Dichalcogenide Transistors with CMOS-Friendly Approaches, Jung-Soo Ko, Stanford University

ID#: 278  Session #: C24.1
A 12-bit 16GS/s Single-channel RF-DAC with Hybrid Segmentation for Digital Back-off and Code-dependent Free Switch Driver achieving -85dBc IMD3 in 5nm FinFET, Byeongwoo Koo, Samsung Electronics

ID#: 279  Session #: C24.4
A 12-bit 10GS/s Time-Interleaved SAR ADC with Even/Odd Channel-Correlated Absolute Error-Based Over-Nyquist Timing-Skew Calibration in 5nm FinFET, Junsang Park, Samsung Electronics

ID#: 298  Session #: C18.5
A Single-Channel, 1-GS/s, 10.91-ENOB, 81-dB SFDR, 9.2-fJ/conv.-step, Ringamp-Based Pipelined ADC with Background Calibration in 16nm CMOS, Jorge Lagos, imec

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Backside power distribution for nanosheet technologies beyond 2nm, Ruilong Xie, IBM

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A Beyond-the-rail Audio CTDSM with a Passive Input Stage and 99.2dB SNDR, Shenyang Li, Delft University of Technology

ID#: 308  Session #: C5.4
Current Mirrors with Tapered Stacked-Gates for Area Saving or Noise Improvement in 3nm FinFET Process, Chu-En Hsia, Taiwan Semiconductor Manufacturing Company

ID#: 310  Session #: C15.3
A Smart Contact Lens System with 433MHz Wireless Power and Data Transfer at a Modulation Index Down to 0.02%, Heesung Roh, POSTECH

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Product Performance Aware 3rd Generation GAA Platform Transistor Design with Extreme Small Local Layout Effect and Transistor Variation, Dongchan Jeong, Samsung Electronics

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An Offset-Compensated Charge-Transfer Pre-Sensing Bit-Line Sense-Amplifier for Low-Voltage DRAM, Kyeongtae Nam, Samsung Electronics

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A 0.6-1 V VIN Soft-Switching Low Dropout Regulator With 31.3 A/mm2 Current Density, 99.99% Current Efficiency, and 2.04 fs FoM, Jeongmyeong Kim, KAIST

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A 2000-Volumes/s 3D Ultrasound Imaging Chip with Monolithically-Integrated 11.7x23.4mm<sup>2</sup> 2048-Element CMUT Array and Arbitrary-Wave TX Beamformer, Nuriel Rozsa, Delft University of Technology

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A 12V-to-1V 100A Inverted Pyramid Trans-Inductor Voltage Regulator Converter with 93.6% High Efficiency and Fast Transient Response, Yu-Chen Kuo, EE, National Yang Ming Chiao Tung University

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A 450&[micro]W@50fps Wake-Up Module Featuring Auto-Bracketed 3-Scale Log-Corrected Pattern Recognition and Motion Detection in a 1.5Mpix 8T Global Shutter Imager, Arnaud Verdant, CEA Leti

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Unlimited Bi-directional Back-Bias in FD-SOI Technology With New Dual Isolation Integration, Remy Berthelon, STMicroelectronics

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A Design Methodology for Back-side Power and Clock Routing Co-Optimization, Pruek Vanniaimpikul, Georgia Institute of Technology

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A Current-Source-Free Constant-Current Wireless Adiabatic Neural Stimulation Achieving a 5.5-27.7x Improved RF-to-Electrode Stimulation Efficiency Factor, Siddharth Agarwal, University of California, San Diego, La Jolla, CA

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A 1.8V-Input 0.2-to-1.5V-Output 2.5A 930mA/mm\(^3\) Always-Balanced Dual-Path Hybrid Buck Converter with Seamlessly All-VCR-Coverable Tri-Mode Operation, Dae-Hyeon Kim, KAIST

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<b>Assessment of the transient self-heating effect and its impact on the performance of Watt-level RF power amplifier in a FinFET technology</b>, Thanh Viet Dinh, NXP Semiconductors

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<b>A 7GHz High-Bandwidth 1R-1RW SRAM for Arm HPC Processor in 3nm Technology</b>, Rahul Mathur, Arm

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A 0.296pl/bit 17.9Tb/s/mm\(^2\) Die-to-Die Link in 5nm/6nm FinFET on a 9&[µ]m-pitch 3D Package Achieving 10.24Tb/s Bandwidth at 16Gb/s PAM-4, Mu-Shan Lin, TSMC

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<b>Concatenated Continuous Driving for Extending Lifetime of Spin Qubits towards</b> <b>a Scalable Silicon Quantum Computer</b>, Takuma Kuno, Hitachi, Ltd.

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A 5nm 60GS/s 7b 64-way Time Interleaved Partial loop unrolled SAR ADC achieving 34dB SNDR up to 32GHz, Claudio Nani, Marvell, Pavia

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<b>A 430-&[µ]A</b> 68.2-bdB-133-dBSPL-AOP CMOS-MEMS Digital Microphone</b> <b>based on Electrostatic Force Feedback Control</b>, Qi Zhang, Zhejiang University

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A Subcellular-Resolution Multimodal CMOS Biosensor Array with 16K Ion-Selective Pixels for Real-Time Monitoring Potassium Dynamics, Hangxing Liu, ETH Zürich

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A 1.1pJ/b/lane, 1.8Tb/s Chiplet over XSR-MCM Channels using 113Gb/s PAM-4 Transceiver with Signal Equalization and Envelope Adaptation using TX-FFE in 5nm CMOS, Gautam Gangasani, Marvell Technology Inc.

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High thermal conductivity AlN films for advanced 3D Chiplets, Takeshi Takagi, The Univ. of Tokyo

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Empowering Local Differential Privacy: A 5718 TOPS/W Analog PUF-based In-Memory Encryption Macro for Dynamic Edge Security, Chih-Sheng Lin, Industrial Technology Research Institute

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A 200-Gb/s PAM-4 transmitter with 1.6-Vppd output swing and clock skew correction in 12-nm FinFET, Boyang Zhang*, Peking University

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Single-crystalline monolayer MoS₂ arrays based high-performance transistors via selective-area CVD growth directly on silicon wafers, Guixu Zhu, University of Science and Technology of China (USTC)

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Ge-doped In2O3: First Demonstration of Utilizing Ge as Oxygen Vacancy Consumer to Break the Mobility/Reliability Tradeoff for High Performance Oxide TFTs, Jiayi Wang, High-Frequency High-Voltage Device and Integrated Circuits R&D Center, Institute of Microelectronics, Chinese Academy of Sciences

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A Low-OSR 5th-Order Noise Shaping SAR ADC Using EF-EF-CIFF Structure with PVT-Robust Differential V-T-V Converter, Yu-Hsiang Huang, National Tsing Hua University

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E-Textile Battery-Less Walking Step Counting System with <23 pW Power, Dual-Function Harvesting from Breathing, and No High-Voltage CMOS Process, Anil Gundu, National University of Singapore

A 336 x 240 backside-illuminated 3D-stacked 7μm SPAD for LiDAR sensor with PDE 28% at 940nm and under 0.4% depth accuracy up to 10m, Jaehyung Jang, SK hynix Inc., CIS Development

In-depth Analysis of the Hafnia Ferroelectrics as a Key Enabler for Low Voltage & QLC 3D VNAND Beyond 1K Layers: Experimental Demonstration and Modeling, Giuk Kim, KAIST

A 400-ns-Settling-Time Hybrid Dynamic Voltage Frequency Scaling Architecture and Its Application in a 22-Core Network-on-Chip SoC in 12-nm FinFET Technology, Erik Loscalzo, Columbia University

Integration of Si-Interposer and High Density MIM Capacitor on 2.5D Foveros Face-to-Face Architecture, Chris Pelto, Intel

Record Performance in GAA 2D NMOS and PMOS using Monolayer MoS$_2$ and WSe$_2$ with scaled contact and gate length, Wouter Mortelmans, Intel

A 512x512 SPAD Laser Speckle Autocorrelation Imager in Stacked 65/40nm CMOS, Robert Henderson, University of Edinburgh

Overcoming Performance Limitation of IGZO FET by iCVD Fluorine Doping, SEUNG HYUN OH, KAIST

A Temporal Noise Reduction via 40% Enhanced Conversion Gain in Dual-Pixel CMOS Image Sensor with Full-Depth Deep-Trench Isolation and Locally Lowered-Stack Technology, Seunghwan Lee, Samsung Electronics

Engineering HZO by Flat Amorphous TiN with 0.3nm Roughness Achieving Uniform c-axis Alignment, Record High Breakdown Field (~10nm HZO), and Record Final 2P of 56 μC/cm$^2$ with Endurance >4E12, Zefu Zhao, Graduate Institute of Electronics Engineering, National Taiwan University

An 11.4mm$^2$ 40.2Gbps 17.4pJ/iteration Soft-Decision Open Forward Error Correction Decoder for Optical Communication, Cheng-Hsun Lu, University of Michigan

A -96.5 dBm-Sensitivity, 14 dBm peak power, Self-Interference Resistant IR-UWB Radar Transceiver Supporting Child Presence Detection and Precision Positioning, Hyun-Gi Seok, Samsung Electronics
Low-Damage Processed and High-Pressure Annealed High-\&[kappa] Hafnium Zirconium Oxide Capacitors near Morphotropic Phase Boundary with Record-Low EOT of 2.4\[Angstrom] & high-\&[kappa] of 70 for DRAM Technology, Venkateswarlu Gaddam, KAIST

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A Jammer-Mitigating 267Mb/s 3.78mm<sup>2</sup> 583mW 32x8 Multi-User MIMO Receiver in 22FDX, Florian Bucheli, ETH Zurich

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A 132-to-163 GHz 4TX/4RX Distributed MIMO FMCW Radar Transceiver with Real-time Reference-Clock Synchronization Enabling Cooperative Coherent Multistatic Imaging System, Ruichen Wan, Tsinghua University

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A confined storage nitride 3D-NAND cell with WL airgap for cell-to-cell interference reduction and improved program performances, Davide Resnati, Micron Technology, Inc.

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Amorphous Oxide Semiconductors for Monolithic 3D Integrated Circuits, Suman Datta, Georgia Tech

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A Fully Integrated 48-V GaN Driver Using Parallel-Multistep-Series Reconfigurable Switched-Capacitor Bank Achieving 7.7nC/mm² On-Chip Bootstrap Driving Density, Xuchu Mu, University of Macau

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A 800Gb/s Transceiver for PAM-4 Optical Direct-Detection applications in 5nm FinFet Process, Marco Sosio, Marvell Technology

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Material, Process and System Level Analysis for Parasitic Reduction of Next Generation Logic Technology in conjunction with Backside Power Delivery, Ashish Pal, Applied Materials

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A 0.9pj/b 9.8-113Gb/s XSR Serdes with 6-tap TX FFE and AC coupling RX in 3nm FinFet Technology, A. Chowdhury, Marvell Technology, Toronto, Canada

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A Mixed-signal 3D Footstep Planning SoC for Motion Control of Humanoid Robots with Embedded Zero-Moment-Point based Gait Scheduler and Neural Inverse Kinematics, Qiankai Cao, Northwestern University

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A 4.7-to-5.36Gbps Fault-Injection Attack Resistant AES-256 Engine Using Isomorphic Composite Fields in Intel 4 CMOS, Raghavan Kumar, Intel

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A Vertical Channel-All-Around FeFET with Thermally Stable Oxide Semiconductor Achieving High &[Delta]Ion of 2μA/cell for 3D Stackable 4F² High Speed Memory, Shoichi Kabuyanagi, Kioxia Corporation

ID#: 590  Session #: TFS1.3
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A 9.9TOPS/W Transformer Learning Processor with Approximated Attention Score Gradient Computation and Ternary Vector-based Speculation, Ping-Sheng Wu, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan

ID#: 606  Session #: T10.2
A 14nm FinFET node embedded MRAM technology for automotive non-volatile RAM applications with endurance over 1E12-cycles, Joosung Oh, Samsung Electronics Co., Ltd.

ID#: 616  Session #: TFS2.4
Demonstration of Logic-Block Performance-Power Gain by 1st Generation Back Side Power Delivery Network for SoC and HPC Applications beyond 2nm Node, Hidenobu Fukutome, Samsung Electronics Co., Ltd.

ID#: 622  Session #: C13.3
A 67F²Reconfigurable PUF Using 1T2R RRAM Switching Competition in 28nm CMOS with 5e-9 Bit Error Rate, Yue Cao, Fudan University
ID#: 623  Session #: TFS1.2
P-type SnO Semiconductor Transistor and Application, Chun-Chen Wang, Taiwan Semiconductor Manufacturing Company, Ltd.

ID#: 632  Session #: T15.3
BEOL Compatible Ultra-Low Operating Voltage (0.5 V) and Preconfigured Switching Polarization States in Effective 3 nm Ferroelectric HZO Capacitors, Jiyoung Kim, The University of Texas at Dallas

ID#: 635  Session #: C26.3
A 0.29pJ/step Fully Discrete-Time Charge Domain Bridge-to-Digital Converter for Force Sensing in Spinal Implants Using RC Bridge, Tim Keller, ETH Zurich

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A 79.3fs<sub>rms</sub> Jitter Fractional-N Digital PLL Based on a DTC Chopping Technique, Riccardo Moleri, Politecnico di Milano

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A PVT Robust Signed 8-Bit Analog Compute-In-Memory Accelerator with Integrated Activation Functions for AI Applications, Hechen Wang, Intel Labs

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Integration and Characterization of High Thermal Conductivity Materials for Heat Dissipation in Stacked Devices, W.-Y. Woon, TSMC

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A 92.8% Power Reduction Event-Driven Dual-Mode Touch Analog Front-End IC Featuring 620μW Self-Capacitance Sensing and 500fps Mutual-Capacitance Sensing, Jonghang Choi, Sungkyunkwan University

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A Fully Dynamic 1st-Order &[Delta]-&[Delta]&[Sigma] Modulator with a 468mVpp Input Range for Electrical Impedance Tomography Systems, Haidam Choi, KAIST

ID#: 662  Session #: T8.3
A Novel Chalcogenide Based CuGeSe Selector Only Memory (SOM) for 3D Xpoint and 3D Vertical Memory Applications, Wei-Chih Chien, Macronix

ID#: 663  Session #: C10.4
A 22nm 54.94 TFLOPS/W Transformer Fine-Tuning Processor with Exponent-Stationary Re-computing, Aggressive Linear Fitting, and Logarithmic Domain Multiplicating, Yang Wang, Tsinghua University

ID#: 665  Session #: JFS5.3
High-Resolution and Compact Integrated FMCW-LiDAR Chip with 128 Channels of Slow Light Grating Antennas, Yuya Maeda, Sony Semiconductor Solutions Corporation

ID#: 668  Session #: C29.2
A 6.5-to-6.9-GHz SSPLL with Configurable Differential Dual-Edge SSPD, Achieving 44-fs RMS Jitter, Tianle Chen, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China

ID#: 671  Session #: C28.3
A 101mW, 280fps Scene Graph Generation Processor for Visual Context Understanding on Mobile Devices, Chun-Wei Chang, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan
ID#: 679  Session #: T13.4
Novel Material, Process and Device Innovations for Next Generation Silicon Carbide (SiC) Trench MOSFET Technology, Pratik B Vyas, Applied Materials Inc.

ID#: 684  Session #: C22.2
A 48-Gb/s Half-Rate PAM4 Optical Receiver with 0.27-pJ/bit TIA Efficiency, 1.28-pJ/bit RX Efficiency, and 0.06-mm<sup>2</sup> area in 28-nm CMOS, Chongyun Zhang, ECE Department, The Hong Kong University of Science and Technology

ID#: 688  Session #: C16.4
A 3.3GHz 1048X640 Multi-Bank Single-Port SRAM with Frequency Enhancing Techniques and 0.55V-1.35V Wide Voltage Range Operation in 3nm FinFET for HPC Applications, Ming-Chieh Huang, TSMC

ID#: 691  Session #: JFS6.5
Monolithic 3D Integration of Analog RRAM-based Fully Weight Stationary and Novel CFET 2T0C-based Partially Weight Stationary for Accelerating Transformer, H. Yang, School of Integrated Circuits, Tsinghua University

ID#: 692  Session #: T9.2
Mitigating line-break defectivity with a sandwiched TiN or W layer for metal pitch 18 nm aspect ratio 6 semi-damascene interconnects, Anshul Gupta, imec

ID#: 704  Session #: C4.3
A 5.7kfps Fast Neural Electrical Impedance Tomography IC Based on Incremental Zoom Structure with Baseline Cancellation for Peripheral Nerve Monitoring Systems, Ji-Hoon Suh, KAIST

ID#: 712  Session #: C17.3
A 6.78 MHz Wireless Power and Data Transfer System Achieving Simultaneous 52.6% End-to-End Efficiency and 4.0 Mb/s Forward Data Delivery with Interference-Free Rectifier, Quanrong Zhuang, School of Electronic Science and Engineering, Nanjing University, China

ID#: 713  Session #: T13.2
Field Plate and Package Optimization for GaN Devices and Systems, Tz-Wun Wang, EE, National Yang Ming Chiao Tung University

ID#: 721  Session #: C28.2
A Heterogeneous TinyML SoC with Energy-Event-Performance-Aware Management and Compute-in-Memory Two-Stage Event-Driven Wakeup, Yanchi Dong, Peking University

ID#: 730  Session #: T14.4
Photon-mediated charge transport and stability of physically-defined and self-organized germanium quantum dots/SON barriers in few-hole regime at T > 10 K, Chi-Cheng Lai, National Yang Ming Chiao Tung University

ID#: 748  Session #: JFS6.3
An Ultra-low Voltage Auger-Recombination Enhanced Hot Hole Injection Scheme in Implementing a 3 Bits per Cell e-DRAM CIM Macro for Inference Accelerator, T. C. Kao, National Yang Ming Chiao Tung University

ID#: 751  Session #: C8.1
A 97dB-PSRR 178.4dB-FOM Calibration-Free VCO-&[Delta][Sigma] ADC Using a PVT-Insensitive Frequency-Locked Differential Regulation Scheme for Multi-Channel ExG Acquisition, Sehwang Lee, DGIST

ID#: 754  Session #: T3.3
High Performance Transistor of Aligned Carbon Nanotubes in a Nanosheet Structure, Gregory Pitner, TSMC
A Wireless Neurostimulator using Body-Coupled Link for Multisite Stimulation in Freely Behaving Animals, Taejune Jeon, Yonsei University

Highly manufacturable Self-Aligned Direct Backside Contact (SA-DBC) and Backside Gate Contact (BGC) for 3-dimensional Stacked FET at 48nm gate pitch, Jaehyun Park, Samsung Electronics

Medusa: A 0.83/4.6 μJ/Frame 86/91.6%-CIFAR-10 tinyML Processor with Pipelined Pixel Streaming of Bottleneck Layers in 28nm CMOS, Rohan Doshi, Stanford University

3DIC System-Technology Co-Optimization with a Focus on the Interplay of Thermal, Power, Timing, and Stress Effects, Victor Moroz, Synopsys

A 28nm Approximate / Binary 6T CAM for Sequence Alignment, Brian Crafon, Georgia Institute of Technology

MINOTAUR: An Edge Transformer Inference and Training Accelerator with 12 MBytes On-Chip Resistive RAM and Fine-Grained Spatiotemporal Power Gating, Kartik Prabhu, Stanford University

Package - System Thermal Modeling and New Material, Tsung-Yu Chen, Taiwan Semiconductor Manufacturing Company

A 28GHz 5G NR Wirelessly Powered Relay Transceiver Using Rectifier-Type 4th-Order Sub-Harmonic Mixer, Sena Kato, Tokyo Institute of Technology

Single metal BCAT breakthrough to open a new era of 12 nm DRAM and beyond, Kyosuk Chae, Samsung Electronics

First Demonstration of Superconducting Nb Contact on Heavily-Doped Group IV Semiconductor, Gerui Zheng, National University of Singapore

A 71.5-dB SNDR 475-MS/s Ringamp-Based Pipelined SAR ADC with On-Chip Bit-Weight Calibration, Chao Chen, State Key Laboratory of Integrated Chips and Systems, Fudan University, Shanghai, China

3DIC with Stacked FinFET, Inter-level Metal, and Field-Size (25x33mm^2) Single-Crystalline Si on SiO<sub>2</sub> by Elevated-Epi, Bo-Jheng Shih, National Yang Ming Chiao Tung University

Dyamond: A 1T1C DRAM In-memory Computing Accelerator with Compact MAC-SIMD and Adaptive Column Addition Dataflow, Seongyon Hong, KAIST

Reliable Low-voltage FeRAM Capacitors for High-speed Dense Embedded Memory in Advanced CMOS, Sou-Chi Chang, Intel
ID#: 837 Session #: C27.1
An OLED Display Driver IC Embedding -63dB CMR, 80mV/nA Sensitivity, 390pA Detectable, and Column-Parallel Pixel Current Readout for Real-Time Non-Uniformity Compensation, Gyu-Wan Lim, KAIST

ID#: 838 Session #: T7.5
First Observation of Time Exponent Variations under Positive Bias Stress on a-IGZO Transistors Utilizing Ultrafast On-the-Fly Technique with 1 &micro;s Delay, TAEWON SEO, POSTECH

ID#: 848 Session #: T15.4
Comprehensive Analysis of Duty-cycle Induced Degradations in Hf<sub>x</sub>Zr<sub>1-x</sub>O<sub>2</sub>-based Ferroelectric Capacitors: Behavior, Modeling, and Optimization, Guan Feng, State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University, Shanghai, 200433, China

ID#: 855 Session #: TFS1.4
First Experimental Demonstration of Hybrid Gain Cell Memory with Si PMOS and ITO FET for High-speed On-chip Memory, Shuhan Liu, Stanford University

ID#: 857 Session #: C13.4
An In-Sensor PUF Featuring Optical Reconfigurability and Near-100% Hardware Reuse Ratio for Trustworthy Sensing, Xiaojin Zhao, Shenzhen University

ID#: 859 Session #: T6.1
Fluorine-free Word Line Molybdenum Process for Enhancing Scalability and Reliability in 3D Flash Memory, Takashi Fukushima, Kioxia Corporation

ID#: 860 Session #: C21.3
A 5.4V-Vin, 9.3A/mm<sup>2</sup> 10MHz Buck IVR Chiplet in 55nm BCD Featuring Self-Timed Bootstrap and Same-Cycle ZVS Control, Harish Krishnamurthy, Intel Corporation

ID#: 869 Session #: C15.4
An Intra-Body-Power-Transfer System Energized by an Electromagnetic Energy Harvester for Powering Wearable Sensor Nodes, Hyungjoo Cho, KAIST

ID#: 877 Session #: C12.4
A 1.5 V 132 dBspl AOP Digital Readout Circuit for MEMS Microphone Using Self-Adaption Loop, Ling Wang, Key Laboratory of Analog Integrated Circuits and Systems (Ministry of Education), School of Integrated Circuits, Xidian University

ID#: 879 Session #: T14.2
Single-power-supply compatible cryogenic In<i><sub>0.8</sub></i>Ga<i><sub>0.2</sub></i>AOP Digital Readout Circuit for MEMS Microphone Using Self-Adaption Loop, Ji-Hoon Yoo, Kyungpook National University

ID#: 880 Session #: C9.2
A 640-Gb/s 4&Multiplication Sign 4-MIMO D-Band CMOS Transceiver Chipset, Chenxin Liu, Tokyo Institute of Technology

ID#: 895 Session #: C15.1
A 76&Multiplication Sign 55 X-Ray Energy Binning Dosimeter for Closed-Loop Cancer Radiotherapy, Rahul Lall, University of California, Berkeley

ID#: 903 Session #: C17.1
ID#: 911  Session #: T16.5
A Monolithic 5.7A/mm<sup>2</sup> 91% Peak Efficiency Scalable Multi-Stage Modular Switched Capacitor Voltage Regulator with Self-Timed Deadtime and Safe Startup for 3D-ICs, Jingshu Yu, Intel Labs

ID#: 915  Session #: JFS4.4
A Novel Method for Extracting Asymmetric Source and Drain Resistance in IGZO Vertical Channel Transistors, Sungwon Yoo, Semiconductor R&D Center, Samsung Electronics

ID#: 917  Session #: JFS1.3
A Pulsed Electrochemistry Readout IC with Slew-rate Booting Technique and Phase-domain Δ[Sigma] ADC for Si-Nanowire Electrical Double-layer Capacitance Measurement, Po-Hsun Chu, National Yang Ming Chiao Tung University

ID#: 919  Session #: C23.2
First Heterogeneous and Monolithic 3D (HM3D) Integration of InGaAs HEMTs and InP/InGaAs DHBTs on Si CMOS for Next-Generation Wireless Communication, Nahyun Rheem, KAIST

ID#: 922  Session #: C6.4
A Pulsed Electrochemistry Readout IC with Slew-rate Booting Technique and Phase-domain Δ[Sigma] ADC for Si-Nanowire Electrical Double-layer Capacitance Measurement, Po-Hsun Chu, National Yang Ming Chiao Tung University

ID#: 924  Session #: C22.4
A Highly-Integrated 1536-Channel Quad-Shank Monolithic Neural Probe in 55nm CMOS for Full-Band Raw-Signal Recording, Xiaolin Yang, imec

ID#: 936  Session #: JFS1.1
First Radio-Frequency Circuits fabricated in top-tier of a full 3D Sequential Integration Process at mmW for 5G applications, Jose Lugo-Alvarez, CEA-Leti

ID#: 943  Session #: C3.4
A 28nm 4170-TFLOPS/W/b and 195-TFLOPS/mm<sup>2</sup>/b Multiply-Free Fully-Digital Floating-Point Compute-In-Memory Macro with Mitchell's Approximation, Ruiqi Guo, Tsinghua University

ID#: 945  Session #: T16.4
Fluorine Plasma Treatment-Enabled ITO Transistors: Excellent Reliability and Comprehensive Understanding of Temperature Dependence from 77 K to 375 K, Xuanqi Chen, National University of Singapore

ID#: 953  Session #: C19.2
Scalable Embedded Multi-Die Active Bridge (S-EMAB) Chips with Integrated LDOs for Low-Cost Programmable 2.5D/3.5D Packaging Technology, Wei Lu, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

ID#: 955  Session #: C23.5
A 16-Ch CMI-Tolerant Neural AFE with Inherent CM Detection and Shared CM Suppression Achieving 0.006mm<sup>2</sup>/Ch and 3.1&[micro]W/Ch, Joan Aymerich, imec

ID#: 959  Session #: C19.4
A Customizable Kilo-core Processor Architecture by Reusable Chiplets with Low-latency High-flexibility Die-to-Die Interconnection, Yujie Wang, Institute of Computing Technology, Chinese Academy of Sciences

ID#: 961  Session #: T7.2
Hot-Carrier-Degradation Characterization for Accurate End-of-Life Prediction with 3nm GAA Logic Technology Featuring Multi-Bridge-Channel FET, Seongkyung Kim, Samsung Electronics

ID#: 970    Session #: T8.1
Highly Scalable Vertical Bypass RRAM (VB-RRAM) for 3D V-NAND Memory, Geonhui Han, POSTECH

ID#: 971    Session #: C24.5
A 10G5/s Hierarchical Time-Interleaved ADC for RF-sampling applications, Nereo Markulic, imec

ID#: 972    Session #: T10.3
Extremely scaled perpendicular SOT-MRAM array integration on 300mm wafer, Farrukh Yasin, imec

ID#: 974    Session #: TFS2.5
Backside Power Delivery in High Density and High Performance Context: IR-drop and Block-level Power-Performance-Area Benefits, Yun Zhou, imec

ID#: 976    Session #: T11.1
V-sub-t Fine-Tuning in Multi-V-sub-t Gate-All-Around Nanosheet nFETs using Rare-Earth Oxide-based Dipole-First Gate Stack Compatible with CFET Integration, Hiroaki Arimura, imec

ID#: 979    Session #: T11.3
Breakthrough processes for Si CMOS devices with BEOL compatibility for 3D sequential integrated More than Moore analog applications, Daphnée Bosch, Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France

ID#: 989    Session #: C26.4
A 0.72nW, 0.006mm2 32kHz Crystal Oscillator with Adaptive Sub-Harmonic Pulse Injection from -40[deg]C to 125[deg]C in 22nm FDSOI, Yingjie Zhu, Southern University of Science and Technology

ID#: 992    Session #: T1.4
On the extreme scaling of transistors with monolayer MoS2 channel, Terry Hung, TSMC

ID#: 997    Session #: C23.3
A 79.2dB-SNDR Slope-Adaptive Dynamic Zoom-and-Track Incremental &[Delta]&[Sigma] Neural Recording Frontend with Resolution-Preservative 192mV/ms Transient Tracking, Sungjin Oh, University of Michigan

ID#: 1003   Session #: C13.5
A 65nm Delta-Sigma ADC based VDD-Variation-Tolerant Power-Side-Channel-Attack Monitor with Detection Capability down to 0.25[Omega], Shota Konno, Asahi Kasei Microdevices Corporation

ID#: 1004   Session #: C23.4
A 3072-Channel Neural Readout IC with Multiplexed Two-Step Incremental-SAR Conversion and Bulk-DAC-Based EDO Compensation in 22nm FDSOI, Xiaohua Huang, imec

ID#: 1005   Session #: JFS4.2
A 65nm Neuromorphic Bio-signal Encoder with Compute-in-Entropy Architecture 7.13nJ Privacy-preserving Encoding and 2.38Mb/mm² Encoding Memory Density, Boyang Cheng, University of Notre Dame

ID#: 1012   Session #: T2.4
Unveiling Cryogenic Performance (4 to 300 K) towards Ultra-thin Ferroelectric HZO: Novel Kinetic Barrier Engineering and Underlying Mechanism, Dong Zhang, Department of Electrical and Computer Engineering, National University of Singapore (NUS), 117576, Singapore

ID#: 1017   Session #: T9.4
Toward 0 V ESD protection in 2.5D/3D advanced bonding technology, SHIH-HSIANG LIN, imec

ID#: 1029  Session #: T10.4
First demonstration of high retention energy barriers and 2 ns switching, using magnetic ordered-alloy-based STT MRAM devices, Matthias Gottwald, IBM

ID#: 1034  Session #: C29.1
A 9-GHz Subsampling-Chopper PLL with Charge-Share Cancelling and Achieving 57.8-fs-rms Jitter with 15dB In-band Noise Improvement, Xiangjian Kong, Guangdong University of Technology

ID#: 1035  Session #: C6.3
A Digital Dynamic Vision Sensor with SPAD pixels and Multi-Event Generation for Motion/Vibration-Adaptive Detection, Houk Lee*, Sungkyunkwan University

ID#: 1039  Session #: T16.2
Positive Bias Stress Measurement Guideline and Band Analysis for Evaluating Instability of Oxide Semiconductor Transistors, Qi Jiang, Stanford University

ID#: 1043  Session #: T5.2
Monolithic Complementary Field Effect Transistors (CFET) demonstrated using Middle Dielectric Isolation and Stacked Contacts, Steven Demuynck, imec

ID#: 1047  Session #: T4.3
Enhancement of InO<sub>2</sub> Field-Effect Mobility Up To 152 cm<sup>-1</sup>&middot;V<sup>-1</sup>&middot;s<sup>-1</sup> Using HZO-Based Higher-k Linear Dielectric, Zehao Lin, Purdue University

ID#: 1054  Session #: C12.1
23,000-Exposures/s 360fps-Readout Software-Defined Image Sensor with Motion-Adaptive Spatially Varying Imaging Speed, Roberto Rangel, University of Toronto

ID#: 1055  Session #: T11.2
Replacement Metal Gate Process Extendible Beyond 2 nm Node with Superior Gate Conductivity, Naomi Yoshida, Applied Materials

ID#: 1057  Session #: C22.5
A 4.6pJ/b 64Gb/s Transceiver Enabling PCIe 6.0 and CXL 3.0 in Intel 3 CMOS Technology, Dong-Myung Choi, Intel Corporation

ID#: 1063  Session #: T12.4
A Dual-Gate Vertical Channel IGZO Transistor for BEOL Stackable 3D Parallel Integration for Memory and Computing Applications, Ziyi Liu, School of Integrated Circuits, ICFC, BNRist, Tsinghua University, Beijing, China.

ID#: 1065  Session #: C8.5
A 10.8GS/s, 84MHz-BW RF Bandpass &[Sigma]&[Delta] ADC with a 89dB-SFDR and a 62dB-SNDR for LTE/5G Receivers, Alhassan Sayed, Seamless Waves

ID#: 1068  Session #: C11.4
A 3.2GHz-15GHz Low Jitter Resonant Clock Featuring Rotary Traveling Wave Oscillators in Intel 4 CMOS for 3D Heterogeneous Multi-Die Systems, Vinayak Honkote, Intel Corporation

ID#: 1072  Session #: C14.4
A 4x50Gb/s NRZ 1.5pJ/b Co-Packaged and Fiber-Terminated 4-Channel Optical RX, Sashank Krishnamurthy, Intel Corporation
A 25.4-27.5 GHz Ping-Pong Charge-Sharing Locking PLL Achieving 42 fs Jitter with Implicit Reference Frequency Doubling, Sayan Kumar, University College Dublin

Cost-effective LLM accelerator using processing in memory technology, hyungdeok Lee, SK hynix

FSNAP: An Ultra-Energy-Efficient Few-Spikes-Neuron based Reconfigurable SNN Processor Enabling Unified On-Chip Learning and Accuracy-Driven Adaptive Time-Window Tuning, Ruixin Mao, University of Electronic Science and Technology of China

First Demonstration of Monolithic Three-dimensional Integration of Ultra-high Density Hybrid IGZO/Si SRAM and IGZO 2T0C DRAM Achieving Record-low Latency (10ns), Record-low Energy (10fJ) of Data Transfer and Ultra-long data retention (5000s, Menggan Liu, Laboratory of Microelectronic Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences (CAS)

<b>4F<sup>2</sup> Stackable Polysilicon Channel Access Device for Ultra-Dense NVDRAM</b>, Albert Liao, Micron

An Intel 3 Advanced FinFET Platform Technology for High Performance Computing and SOC Product Applications, Walid Hafez, Intel

A 256Gbps Microring-based WDM Transceiver with Error-free Wide Temperature Operation for Co-packaged Optical I/O Chiplets, Pavan Bhargava, Ayar Labs

An Intel 3 Advanced FinFET Platform Technology for High Performance Computing and SOC Product Applications, Walid Hafez, Intel

Scaling Potential of Nanosheet Oxide Semiconductor FETs for Monolithic 3D Integration - ALD Material Engineering, High-Field Transport, Statistical Variability, Kaito Hikake, Institute of Industrial Science, The University of Tokyo

Polar axis orientation control of hafnium-based ferroelectric capacitors with in-situ AC electric bias during rapid thermal annealing, Zhaomeng Gao, East China Normal University

Highly Robust All-Oxide Transistors with Ultrathin In<sub>2</sub>O<sub>3</sub> as Channel and Thick In<sub>2</sub>O<sub>3</sub> as Metal Gate Towards Vertical Logic and Memory, Zehao Lin, Purdue University

A 30fps 64 & 64 CMOS Flash LiDAR Sensor with Push-Pull Analog Counter Achieving 0.1% Depth Uncertainty at 70m Detection Range, Dongseok Cho, Yonsei University
A 32Gb/s 0.36pJ/bit 3nm Chiplet IO using 2.5D CoWoS Package with Real-Time and Per-Lane CDR and Bathtub Monitoring, John Ma, Marvell Technology Group

First Demonstration of BEOL-Compatible Vertical Fe-NOR, Yang Feng, Department of Electrical and Computer Engineering, National University of Singapore (NUS), 117576, Singapore

On the Reliability of High-Performance Dual Gate (DG) W-doped In$_2$O$_3$ FET, Khandker Akif Aabrar, Georgia Institute of Technology

122.7 TOPS/W Stdcell-Based DNN Accelerator Based on Transition Density Data Representation, Clock-Less MAC Operation, Pseudo-Sparsity Exploitation in 40 nm, Animesh Gupta, National University of Singapore

CogniVision: End-to-End SoC for Always-on Smart Vision with mW Power in 40nm, Animesh Gupta, National University of Singapore

A 0.9-2.6pW 0.1-0.25V 22nm 2-bit Supply-to-Digital Converter Using Always-Activated Supply-Controlled Oscillator and Supply-Dependent-Activation Buffers for Bio-Fuel-Cell-Powered-and-Sensed Time-Stamped Bio-Recording, Hiroaki Kitaike, Kyoto University

Co-Optimization for Robust Power Delivery Design in 3D-Heterogeneous Integration of Compute In-Memory Accelerators, Madison Manley, Georgia Institute of Technology

Terahertz Sensing with CMOS-RFIC - Feasibility Verification for Short-Range Imaging using 300GHz MIMO Radar, Ichiro Somada, Mitsubishi Electric Corp.

A Quad-Core AI Processing Unit for Generative AI in 4nm 5G Smartphone SoC, Chien-Hung Lin, MediaTek Inc.

AMD Instinct\textregistered\ MI300X Accelerator: Packaging and Architecture Co-Optimization, Alan Smith, AMD

A Three Dimensional DRAM (3D DRAM) Technology for the Next Decades, Joodong Park, SKhynix

A 28GHz 4-Stream Time-Division MIMO Phased-Array Receiver Utilizing Nyquist-Rate Fast Beam Switching for 5G and Beyond, Yi Zhang, Tokyo Institute of Technology