

HILTON HAWAIIAN VILLAGE
HONOLULU, HAWAII | JUNE 14-18, 2026

ADVANCING THE AI FRONTIER

through VLSI Innovation

FINAL CALL FOR PAPERS

Paper Submission Deadline: 23:59 PST Monday, January 26, 2026
www.vlsisymposium.org

Symposium Scope

The Symposium calls for papers in the following areas:

- Advanced CMOS Platforms, Interconnect and Backside Power Delivery Network (BSPDN) Technologies
- Advanced packaging, Chiplet and Heterogeneous Integration Technologies, including 2.5D and 3D
- Analog and Mixed-Signal Circuits
- Beyond CMOS Devices That Utilize New Physics Including Spin, Optical and Quantum Computing
- Biomedical devices, circuits, and systems
- Computing/Processing in Memory
- Data converters
- Device physics, Characterization, Modeling and Reliability
- Devices and Accelerators for ML/DL and New Compute
- Digital Circuits, Hardware Security, Signal Integrity, IOs
- DTCO and Design Enablement
- Frequency Generation and Clocking Circuits
- Memory Technologies, Devices, Circuits, and Architectures
- Power Management Devices and Circuits
- Processes and Materials for CMOS Scaling and New Devices
- Processors and SoCs
- Sensors, Imagers, IoT, MEMS, Display Circuits
- Wireless and RF Devices Circuits and Systems
- Wireline and Optical Transceivers, Optical Interconnects and Processors

Paper Submission

Prospective authors must submit paper abstracts in the **three-page** paper format according to the Symposium website: www.vlsisymposium.org. Accepted papers will be published as submitted with no revisions permitted. Authors must follow detailed instructions provided in the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. Students are encouraged to apply for the prestigious Best Student Paper Award. Extended versions of outstanding papers will be invited for publication in the IEEE Transaction on Electron Devices, IEEE Journal of Solid-State Circuits, and IEEE Solid-State Circuits Letters.



Symposium Chairs:
Vijay Narayanan, IBM T.J. Watson Research Center
Ron Kapusta, Analog Devices

Symposium Co-Chairs:
Kazuhiro Endo, Tohoku University
Sugako Otani, Renesas Electronics Corporation

Program Chairs:
Benjamin Colombeau, Applied Materials
John Wu, Advanced Micro Devices

Program co-chairs:
Masaharu Kobayashi, The University of Tokyo
Makoto Takamiya, The University of Tokyo

(North America and Europe) :
Canfield Event Management
vlsi@vlsisymposium.org, +1-972-521-9902

(Asia and Japan) :
JTB Communication Design
vlsisymp@jtocom.co.jp, +81-3-5657-0777

Highlights

The Symposium will be a fully in-person event at the Hilton Hawaiian Village, Honolulu, Hawaii, with on-demand access to technical sessions available one week following the Symposium. The 5-day event will include: **Plenary Sessions, Technical Sessions, Demo Sessions, Short Courses, Evening Sessions, Workshops, SSCS/EDS Women in Engineering and Young Professionals Events and Hawaiian Luau celebration.**

Short Courses

The Symposium will offer Short Courses on Technology and Circuit.

- Technology - Technologies Shaping the Future as Key Enablers for AI
- Circuit - AI-Driven Design Acceleration: Learning Across Circuits, Technology, & Yield

Focus Sessions

In addition to the solicited topics, the Symposium will offer Focus Sessions on special areas of Technology and Circuits of joint interest, such as:

- Beyond 2nm Logic (Technology)
- Advanced Memory (Technology)
- 2.5D/3D Integration (Joint)
- AI/ML in the physical world (Joint)
- New computing, quantum, CIM (Joint)
- HPC connectivity architecture (Joint)

Evening Panel Discussion

This year, the panel discussion will focus on the following topic:

- AI: Grand Vision or Grand Delusion?

Best Student Paper Awards

Selection will be based on the quality of the paper and presentation at the Symposium. The winning student will be presented with a certificate and monetary award at the 2026 VLSI Symposium opening session.

Demonstration Session

The popular in-person demonstration session will be part of the Symposium program, providing participants with an opportunity for in-depth interaction with authors of selected papers from both Tech and Circuit.