2024 VLSI SYMPOSIUM

2024 IEEE SYMPOSIUM
ON VLSI TECHNOLOGY AND CIRCUITS

BRIDGING THE DIGITAL & PHYSICAL WORLDS
with efficiency & intelligence

HILTON HAWAIIAN VILLAGE
HONOLULU, HAWAII
JUNE 16-20, 2022

Program

Workshops

Sunday, June 16, 1:00 PM – 5:30 PM

Standing Workshop: Open-Source Design
1:00 PM, Tapa 1
Advancing SoC Design: Open-Source and ML-Driven Approaches in the Cloud

- **Cloud bursting an EDA workload with ML-driven technique for future SoC development,** by Dr. Wachirawit Ponghiran and Dr. Jinwook Jung (IBM Research)
- **Generative AI-based EDA for SoC,** by Dr. Rongjian Liang (NVIDIA)
- **Chipyard: An Open-Source Design, Simulation, and Implementation Framework for Custom RISC-V SoCs,** by Sagar Karandikar (UC Berkeley)
- **ESP: An Open-Source Platform for Agile SoC Design,** by Dr. Luca Carloni (Columbia University)
- **AMS generation frameworks: an industry perspective,** by Dr. Cooper Levy (Intel)
- **Agile SoC Design With OpenROAD and Proprietary Flows: A Retrospective,** by Dr. Austin Rovinski (NYU)
- **Agile-X: democratization base of innovative semiconductor technology,** by Dr. Makoto Ikeda (University of Tokyo)
- **Freshmen through Ph.D. students experience open-source tape-out: successes and pitfalls**, by Dr. Mark Johnson (Purdue University)

Circuits Workshop 1: High-Performance Mixed-Signal Circuits: Recent Art Balancing the Analog vs. Digital
1:00 PM, Tapa 3

The aim of this workshop is to gather prominent figures in the field to discuss recent advancements in mixed-signal circuits for high-speed / high-accuracy applications, including PLLs, ADCs, DACs, and more. Our focus lies on high-performance systems, specifically on achieving the optimal balance between pure analog performance and the integration of digital assistance / calibration to maximize system-level performance. We strive to provide the audience with a view and examples of how real-world designs (ADCs, PLLs, DACs) partition/budget their performance between raw-analog and digitally-assisted, showing what criteria are normally followed in these decisions. A secondary goal would be to comment on some of the techniques that are exploited on each side (analog, digital) to enable and realize such partitioning.

Moderators: Jorge Lagos, imec and Tetsuya Iizuka, The University of Tokyo

- **PLLs**, Tetsuya Iizuka, The University of Tokyo
- **DACs**, Martin Clara. Intel
- **ADCs**, Huseyin Dinc, Analog Devices

Technology Workshop 2: Novel Metals and Advanced Interconnects
3:15 PM, Tapa 2
Organizers: Christoph Adelmann, Zsolt Tőkei, imec

- **Novel Metals for Advanced Interconnects,** Christoph Adelmann, Imec
- **An industry perspective of beyond Cu, alternative metal interconnects,** Christopher Jezewski, Intel

- **Replacing Tungsten and Copper by Molybdenum in logic technology,** Vamsi Paruchuri, ASM International
- **The search for new materials for interconnects < 10 nm,** Daniel Gall, Rensselaer Polytechnic Institute
- **Opportunities and challenges of intermetallic compounds for future interconnects,** Junichi Koike, Tohoku University
- **Intercalated Graphene for Advanced Interconnects,** Kaustav Banerjee, Destination 2D and University of California Santa Barbara
- **Interconnect Technology/System Co-Design for VLSI Logic and Memory Systems,** Chenyun Pan
- University of Texas at Arlington

Circuits Worshop 2: BioSensory Breakthroughs: Pioneering the Future of Health Tech

3:30 PM, Tapa 3

This workshop session discusses the forefront of sensor technology and bioelectronics integration. Dr. Drew Hall (UCSD) explores the future of injectable biosensors, while Dr. Mahsa Shoaran (EPFL) discusses low-power AI-driven neural interfaces. Dr. Minkyu Je (KAIST) presents low-power bioimpedance measurement techniques, and Dr. Sufi Zafar (IBM) focuses on miniaturized biosensors. Dr. Ken Shepard (Columbia University) explores CMOS bioelectronics for efficient implantables, and Dr. Ada Poon (Stanford University) introduces a battery-free sticker-like reader for wireless passive sensors. These presentations collectively highlight the transformative potential of sensor technologies across diverse applications.

- **Injectable Biosensors: Is there a future?** Drew Hall, UCSD
- **Low-Power AI-Driven Neural Interfaces for Treating Brain Disorders,** Mahsa Shoaran, EPFL
- **Low-Power Bioimpedance Measurement Techniques for Sensing and Imaging,** Minkyu Je, KAIST
- **Silicon Device based miniaturized biosensors for Healthcare & IoT,** Sufi Zafar, IBM
- **CMOS bioelectronics for volumetrically efficient implantables,** Ken Shepard, Columbia University
- **A Battery-free Sticker-like Reader for Wireless Passive Sensors,** Ada Poon, Stanford University

Short Courses

Circuits Short Course

Monday, June 17, 8:20 a.m. – 5:00 p.m.
Tapa 2

Circuits and Systems for Heterogeneous Integration
Organizers: C. Tokunaga, Intel, T. Nezuka, MIRISE Technologies, N. Kocaman, Broadcom, K. Nii, TSMC

8:30 a.m.
Advanced Packaging Enabling Heterogeneous Integration, Liwei Wang, AMD
Abstract: The exploding demand for computation spans from the cloud to the edge, and from artificial intelligence (AI) to 5G communications, is driving the technology and design innovations beyond what Moore's law can support with raw silicon scaling. As is widely known, silicon technology node introductions have been slowing down and simultaneously delivering less benefit, while at the same time the costs per yielded mm2 of silicon are going up. This is particularly challenging because the semiconductor industry has thrived on delivering more performance and features in each Si node generation. With these trends, the cost per transistor will stop scaling in the next few years, which creates notable economic headwinds

to meeting the demand. The next aspect of the slowdown in node introductions is that scaling factors are diverging between different intellectual property (IP) types, with static random-access memory (SRAM) and especially analog circuits lagging well behind the scale factors of logic. This leads to the chip-level view of area scaling where, with a mix of logic, SRAM, and analog content, it's not feasible to shrink chip designs appreciably toward the end of this decade. The trillion-dollar question is how to architect, design, and build future systems that solve these challenges. The answer is increasingly clear that heterogeneous integration of the modular, multi-chip design/chiplets is a fundamental enabler.

9:20 a.m.
I/O design considerations for die-to-die interface, Yoshinori Nishi, NVIDIA
Abstract: Today's advanced systems feature multiple chips and chiplets on interposers, using technologies commercially known as EMIB, CoWoS, InFO, FOCoS, and several others from multiple sources. These 2D/2.5D structures require ultra-dense I/O PHYs to deliver a large amount of data between dies over a distance of a few millimeters without adding much power and area penalty to each die. In this talk, we will highlight several important use-cases of chiplets for AI and data centers, along with ongoing standardization efforts and the latest trends in I/O circuit designs for die-die interface.

10:10 a.m. Break

10:30 a.m.
Directions, Challenges and Opportunities in Heterogeneous Integration and Packaging, Chris Pelto, Intel
Abstract: In this tutorial we will focus on the evolution, current value and future scaling opportunities of heterogeneously integrated (HI) advanced packaging architectures which continue to define technology envelopes. HI is a powerful, crucial enabler for the continued growth of computing and communication performance. Advanced packaging technologies are critical enablers of HI because of their importance as compact, power efficient platforms. A roadmap of the future generated as part of an industry-academic collaboration will be discussed in this context to highlight the opportunities generated by HI. Opportunities in physical interconnect scaling, an important part of the HI Roadmap will be discussed in detail. We will also discuss the impact of package features on high speed IO and broadly describe challenges in power delivery, cooling, manufacturing and design.

11:20 a.m.
Heterogenous integration for automotive ICs, Hubert Bode, NXP
Abstract: Heterogenous integrated systems have a long history in automotive electronics. Automotive system requirements are illustrated and examples of heterogenous systems are given. Factors influencing (heterogenous) systems and their architectures are discussed. Formerly monolithic devices are now more and more build as heterogenous systems. This is caused by car architecture evolvement influencing what silicon technologies can be used effectively. Examples of heterogenous systems with partitioning and sub-system interfaces are shown. System aspects versus the automotive requirements and considerations arising out of the heterogeneous integration are discussed. An outlook is given about the car OEM's vision of future car control systems.

12:10 p.m. Lunch

1:20 p.m.

Wafer Scale System Integration Technology, Kuo-Chung Yee, TSMC

Abstract:

In recent years, advanced packaging has taken center stage of the semiconductor industry to pursue ever more energy efficient, high-performance, and cost-effective electronic systems. While wafer scale system integration technology (WSSIT) is going through revolutionary technology advances across mobile computing and HPC/AI computing applications. Such wafer scale system integration technologies include wafer scale fan-out PoP in smart mobile system, wafer scale fan-out on substrate in networking, wafer scale 2.5D interposer package in HPC/AI, wafer scale 3D chip on wafer stack in HBM, 3D V-cache, and 3D wafer on wafer stack in CIS and power delivery. Wafer scale integration features high yield, fine pitch, high density interconnects and tight integration between chiplets, leveraging installed capacity of advanced wafer-based tools & materials, design & process know-hows to enable IC-ized manufacturing with fine process control, monitor, and robust integrity. This presentation will introduce the main wafer scale integration technologies in mobile and HPC/AI applications, featuring the figure of merits (aka EEPAC) on architecture, integration process, and interconnect of various electronics compute systems. Design considerations and process challenges of WSSIT will also be discussed.

2:10 p.m.

Advancements in Co-Packaging and Co-Integration Technologies for High-Performance Memory Systems, Kyungryun Kim, Samsung and Wonkyoung Choi, Samsung

Abstract: This course presents a comprehensive examination of co-packaging and co-integration technologies for high-performance memory systems, highlighting their pivotal roles in system performance and efficiency. Due to advancements in 2.5D packaging technologies, memory and computation dies are co-packaged and connected with higher bandwidth than ever. Silicon interposer technology enables a higher bandwidth connection between memory and computation dies via densely integrated I/O lines, while die stacking technology, using through-silicon vias (TSVs) and micro-bumps, brings a large amount of memory closer to a computation die. These solutions not only provide higher performance and density but also better power efficiency via tight memory connections. As a next step, 3D packaging technologies are being developed to allow even tighter connections between memory and computation dies. In this configuration, multiple memory dies will be mounted on and connected to a computation die via TSVs and micro-bumps, and this architecture possibly enables the shortest and widest connection path between memory and computation dies. The final step of co-packaging and co-integration will involve integrating computational logic into a memory die, a so-called Processing-in-Memory (PIM) technology. This technology has emerged as a pivotal, promising solution to reduce latency and power consumption by offloading logic operations to memory. As an interim solution, the concept of custom High Bandwidth Memory (CHBM), where custom computation logic is integrated into an HBM buffer die, has emerged. Many companies are actively exploring the potential differentiation via co-integration of logic and memory based on the CHBM architecture.

3:00 p.m. **Break**

3:20 p.m.

Evolution and Future of Heterogenous 3D Integrated Circuits and their Design using EDA Tools, David Stratman, Cadence

Abstract: The past twenty years have introduced multiple waves of novel 2.5D/3D integrated circuit design, implementation, fabrication, and packaging techniques to the semiconductor industry. While some approaches have found commercial adoption and success, others remain niche and seemingly forever waiting for mainstream deployment. This paper is an introduction to the layered history of why these

three-dimensional constructs have evolved to help overcome the slowing scaling of Moore's law, the growing cost of manufacturing advanced ICs, and the increasing complexity of chip design. In addition to cataloging the various 3DIC approaches, we will also discuss the electronic design automation (EDA) industry's role in enabling the current state of the art, and goals towards driving the future. The pace of innovation in the 3DIC space has accelerated over the last five years with the industry's embrace of chiplets and growing ability to stack or bridge integrated circuits from different process nodes and even different foundries. These exciting trends and the advent of new EDA platforms and AI-driven design techniques are shaping the future of 3DIC.

4:10 p.m.

Integrated Power Delivery and Management Technologies for Heterogenous Integrated Systems, Hanh-Phuc Le, UCSD

Abstract: The semiconductor industry is betting its future of next generation microelectronic systems on heterogeneous integration (HI) for more performance density, particularly in in data center, autonomous vehicle, and mobile applications. To support this irreversible direction, it is very important to have adequate advanced technologies that can help meet the increasingly demanding requirements for integrated power delivery in terms of efficiency, size, reliability, and cost while addressing the need to simultaneously support many supply rails, large input/output voltage differences, and high output current density. In this talk, the speaker will describe a set of integrated power delivery and management techniques and technologies that could be strong candidates to address this need, including integrated power delivery architectures, advanced converter topologies, integrated passive devices, packaging strategies, and other technologies on the horizon. An example of a 2-stage HI power delivery will also be included.

Technology Short Course

Monday, June 17, 8:25 a.m. – 4:50 p.m.

Tapa 3

Advanced VLSI technologies for next generation computing

Organizers: Yue Liang, Nvidia; Shosuke Fujii, Kioxia

8:30 a.m.

CMOS Device Scaling for Power-Performance - Key Physics and Challenges, Jeff Wu, TSMC

Abstract: Along with doubling of components on a microchip every two years following Moore's law, the overall performance and power efficiency have also improved exponentially over the years, thanks to CMOS device scaling which has been the work horse behind the phenomenal performance gain. Key considerations in device architecture and design to optimize power-performance are discussed. Physics emerging or becoming more important in the extremely scaled devices will be highlighted and illustrated.

9:20 a.m.

Innovations of Material and Process Engineering in the Angstrom Era for Advanced CMOS Logic Technology, Veeraraghavan Basker, Applied Materials

Abstract: The relentless pursuit of Moore's Law scaling has led to the emergence of the Angstrom era. 3D device architectures, such as gate-all-around (GAA) transistors, provide enhanced control and scalability. Process advancements include EUV lithography, atomic layer deposition & etching, and directed self-assembly deposition enabling precise control at the atomic scale. These innovations overcome fundamental limitations, delivering significant improvements in power, performance, area & cost (PPAC)

as well as facilitating continuous advancement in CMOS technology for next generation computing applications.

This short course explores the pivotal role of material and process advancements in the Angstrom era pushing the boundaries of advanced logic CMOS technology. Firstly, it delves into the current state-of-art GAA nanosheet (NS) technology and the key challenges. Various process and device solutions to extend GAA NS for upcoming technology nodes will be discussed. The synergistic effects of integrating material and process innovations leading to enhanced device performance, reduced power consumption and area scaling in GAA NS technology will be addressed. Furthermore, this course will examine the 3D CFET/Stacked-FET architecture and its fabrication options. It will also highlight the recent progress of monolithic-CFET (m-CFET) in the industry. Lastly, key unit process bottlenecks will be illustrated in a generic m-CFET flow.

10:10 a.m. Break

10:30 a.m.
Integration Challenges for Pitch Scaling in Advanced BEOL Interconnects, Hirokazu Aizawa, TEL
Abstract: Since the introduction of device chips with copper (Cu) interconnects in 1997, this technology has been the backbone for Back-End-of-Line (BEOL) of logic devices, and it has evolved with improved metallization and integration schemes to keep pace with Moore's law. However, concerns have arisen regarding the technological constraints of Cu damascene interconnects due to continuous pitch scaling. Consequently, intensive research and development efforts are underway for the next generation of interconnect technology, exploring alternative metals and subtractive interconnect methods.

This short course aims to provide a comprehensive overview of the technical challenges associated with Cu damascene interconnects amid advanced pitch scaling. It will also discuss potential technical solutions and offer insights into the future of interconnect technology.

11:20 a.m.
Functional Backside: past, present, and STCO future, James Myers, IMEC
Abstract: Since the end of Dennard scaling, power density has become a prime concern in future technology roadmaps. Design technology co-optimization (DTCO) research has shown that using the backside of the wafer to bring power delivery networks (PDNs) closer to the transistors has significant benefits for logic density and power integrity. Now that foundries have announced support for backside PDN in future nodes, what additional functionality could be migrated or added to the backside? What system level problems could this solve? System technology co-optimization (STCO) is required to answer these questions and can propose new technology options tailored to the differing requirements of mobile, GPU, server or wearables. Eventually, the roadmap may evolve towards a complex heterogeneous device stack that is very disruptive to future designs – CMOS 2.0.

12:10 p.m. Lunch

1:20 p.m.
In-memory-computing with emerging memories, J. Joshua Yang, University of Southern California
Abstract: The rapid advancement of machine learning and artificial intelligence is propelling a pressing need for dramatically enhanced computing power, prompting the exploration of innovative computing paradigms such as in-memory computing (IMC). IMC offers a solution to the diminishing cost-effectiveness of transistor scaling and the inherent inefficiencies of traditional non-von Neumann computing

architectures in dealing with big data. This short course will discuss the special requirements on memory devices for IMC applications. It evaluates various resistive switching materials (RSMs) based on different physical principles, including redox reactions, phase transitions, spin-polarized tunneling, and ferroelectric polarization, to discern their suitability for IMC applications. Redox-reaction-based RSMs, as the most advanced among these four for IMC, will be used as an example to reveal insights into the fundamental concepts, existing challenges, and potential solutions. Additionally, it offers glimpses into chip-level demonstrations showcasing the practical implications of these emerging memories.

2:10 p.m.

Opportunities to break through limit and to enable prolongation of DRAM, Hui-Jung Kim, Samsung Electronics

Abstract: For several decades, many efforts on a VLSI technology have been made to increase the bit-density of the dynamic random access memory (DRAM), which successfully enabled a scaling down of the DRAM nodes to sub-20 nm. The success relies on structural innovations in a small dimension, among the most critical examples as (I) a recessed channel array transistor (RCAT) and a buried channel array transistor (BCAT) have facilitated vertical channel length with reliable switching performances in a small dimension, (II) an implement of BL isolation from other electrodes in one pitch of cell array structure, (III) storage capacitors, a hexagonal arrays and supporter structure expands the charge storage efficiency without a leaning of capacitor nodes in high-aspect-ratio-capacitor. However, as the scaling down continues the further reduction of the design rule to sub-10nm, DRAM will be threatened because the allowed lateral space has a limitation on characteristics of cell transistors, coupling noises of inter-wires resulting in RC delay, and charge isolation in storage capacitors.

This presentation will explore challenges in scaling of conventional 6F2 as mentioned above, and innovative opportunities which are 4F2 vertical channel transistor (VCT), vertically stacked DRAM (VSDRAM) cell structure and other candidates as structural solutions to break through scaling limit, including essential technologies on integration processes to implement.

3:00 p.m. Break

3:20 p.m.

Metrology & Inspection: Past, Present, and Future, Byoungho Lee, Hitachi High-Tech**Abstract:** Metrology&Inspection was “a good to have” process until the late 2000s. However, as process miniaturization entered below 100nm and NAND devices became 3D structures, the perception of the MI process changed to “a must have”. Currently, device development research and major process monitoring in HVM cannot be carried out without the help of MI. However, many people still do not understand exactly what MI is, and even if they do, it is very basic and often leads to misunderstandings. This training seeks to understand the basic concept of MI and its evolution. Based on this, we would like to analyze trends in MI technology and explain future directions.

4:10 p.m.

Silicon photonics for high bandwidth optical I/O, Haisheng Rong, Intel Labs

Abstract: Traditional electrical off-package I/O solutions for high-value compute silicon (e.g., CPUs, GPUs, FPGAs, and ASICs) are facing enormous scaling challenges in meeting the ever-increasing bandwidth demands. Silicon Photonics is one of the most promising technologies to circumvent these challenges and provides a viable path for high bandwidth density and energy-efficient optical-compute-interconnect. This talk will focus on high-speed silicon photonic DWDM transceivers with integrated lasers, optical amplifiers,

silicon modulators, and photodetectors co-packaged with CMOS electronic drivers and receivers to meet future optical I/O demands for AI/ML.

Demo Session & Reception

5:30 PM, Tapa 1

Opening and Plenary I

Tuesday, June 18

8:00 AM, Tapa 1-3

Chairpersons: V. Narayanan, IBM
R. Kapusta, Analog Devices

8:00 a.m. **Welcome and Opening Remarks and Awards**
G. Jurczak, Lam Research
B. Nikolić, University of California, Berkeley

P1.1 – 8:35 AM
Making Sense at the Edge (Invited). Ahmad Bahai, Texas Instruments, SVP & CTO

Semiconductor technology provides the foundation for advanced embedded sensing and actuating technologies across a broad range of applications enabling data driven intelligent systems. Advances in nanotechnology, analog and digital signal processing, embedded/edge machine learning algorithms, connectivity and battery technology have enabled high performance sensing and actuation which was inaccessible a decade ago. Yet in many sensing and actuating modalities, nature offers a significantly more efficient edge computing sensory solution leveraging the hierarchical physical, analog and digital signal processing to optimize performance and energy consumption. In this talk, we review some examples of low power adaptive biosensors as well as bio inspired sensor fusion and how they inspire innovative new devices, circuits and ML systems for intelligent sensing and actuating.

P1.2 - 9:15 AM
Mobility Evolution: Electrification and Automation (Invited), Kazuoki Matsugatani, DENSO Corporation, Senior Director, R&D Center

The automotive industry faces two challenges: environmental impact reduction and safety enhancement. Particularly, efforts to achieve zero CO2 emissions and zero traffic fatalities are urgent issues for the coming decade. Electrification, the transition from internal combustion engines to electric motors, profoundly alters vehicle mechanics. Automation, transferring driving control from humans to computers, integrates software and information technologies into the vehicle system. In both electrification and automation, semiconductor devices' evolution is key. For electrification, the power device managing current from the battery to the motor is crucial for inverter operation. Additionally, an analog sensing device measuring current to and from the battery delivers essential data regarding the battery's state of charge and health. As for automation, various sensors – including camera, radar, lidar and sonar – that monitor outside and inside of the vehicle are required. Furthermore, high-performance computers and wireless communication devices are required to process sensor data, establish a connection between the vehicle and an external network, and control the vehicle on behalf of the human driver. This plenary talk will introduce and explain the functions of these semiconductor devices.

Session T1: Technology Highlights
10:15 AM, Tapa 1-3

Co-Chairs: Ben Colombeau, Applied Materials
Toshifumi Irisawa, National Institute of AIST

10:15 AM

T1.1 An Intel 3 Advanced FinFET Platform Technology for High Performance Computing and SOC Product Applications, Walid Hafez[1], D Abanulo[1], M Abdelkader[1], S An[1], C Auth[1], D Bahr[1], V Balakrishnan[1], R Bambery[1], M Beck[1], S Bhowmick[1], J Biggs-houck[1], J Birdsall[1], D Caselli[1], H.-Y. Chang[1], Y Chang[1], R Chaudhuri[1], S Chauhan[1], C Chen[1], V Chikarmane[1], K Chikkadi[1], T Chu[1], C Connor[1], R DeAlba[1], Y Deng[1], D Diana[1], Y Dong[1], P Elfick[1], T Elko-hansen[1], B Fallahazad[1], Y Fang[1], D Gala[1], C Geppert[1], S Govindaraju[1], H Grunes[1], L Guler[1], Z Guo[1], A Gupta[1], M Hattendorf[1], S Havelia[1], J Hazra[1], A Islam[1], A Jain[1], S Jaloviar[1], M Jamil[1], M Jang[1], M Kabir[1], J Kameswaran[1], E Karl[1], S Kelgeri[1], A Kennedy[1], C Kilroy[1], J Kim[1], Y Kim[1], D Krishnan[1], G Lee[1], H.-P. Lee[1], Q Li[1], H Lin[1], A Luk[1], Y Luo[1], P Macfarlane[1], A Mamun[1], K Marla[1], D Mayeri[1], E Mckenna[1], A Miah[1], K Mistry[1], M Mleczko[1], S Moon[1], D Nardi[1], S Natarajan[1], J Nathawat[1], C Nolph[1], C Nugroho[1], P Nyhus[1], A Oni[1], P Packan[1], D Pak[1], A Paliwal[1], R Pandey[1], I Paredes[1], K Park[1], L Paulson[1], A Pierre[1], P Plekhanov[1], C Prasad[1], R Ramaswamy[1], J Riley[1], J Rode[1], R Russell[1], S Ryu[1], H Saavedra[1], T Salisbury[1], J Sandford[1], F Shah[1], K Shang[1], P Shekhar[1], A Shu[1], E Skoug[1], J Sohn[1], J Song[1], M Sprinkle[1], J Su[1], A Tan[1], T Troeger[1], R Tsao[1], A Vaidya[1], C Wallace[1], X Wang[1], H Wang[1], C Ward[1], S Wickramaratne[1], T Wu[1], Z Xia-hua[1], S Xu[1], P Yashar[1], J Yaung[1], Y Yu[1], M Zilm[1], B Grimm[1], M Bhargava[1], M Wills[1], C Destefano[1], D Garg[1], B Sell[1] [1]Intel

An advanced Intel 3 FinFET technology is presented that has been optimized to provide 10% logic scaling, a full node of performance improvement and improved reliability compared to Intel 4. Through transistor enhancements, interconnect optimization, and design co-optimizations up to 18% performance gain at iso-power is achieved over Intel 4.

10:40 AM

T1.2 Highly Manufacturable Self-Aligned Direct Backside Contact (SA-DBC) and Backside Gate Contact (BGC) for 3-dimensional Stacked FET at 48nm Gate Pitch, Jaehyun Park[1], Juhun Park[1], Kyuman Hwang[1], Jinchan Yun[1], Dahye Kim[1], Sungil Park[1], Jejune Park[1], Jinwook Yang[1], Jae Won Jeong[1], Chuljin Yun[1], Jinho Bae[1], Sam Park[1], Daihong Huh[1], Sanghyeon Kim[1], Seungeun Baek[1], Suk Yang[1], Inhae Zoh[1], Junghan Lee[1], Tae-sun Kim[1], Younsu Ha[1], Sun-Jung Lee[1], Sang Wuk Park[1], Bong Jin Kuh[1], Daewon Ha[1], Sangjin Hyun[1], Su Jin Ahn[1], Jaihyuk Song[1] Samsung Electronics

In this study, we have demonstrated 3-Dimensional Stacked FET (3DSFET) with Self-Aligned Direct Back-side Contact (SA-DBC) and Back-side Gate Contact (BGC) in 48nm gate pitch, which is the smallest dimension and the world's first demonstration reported so far. Simultaneous threshold voltage (Vt) targeting for both n- and pFET in common gate and n/pconnection with vertical common contact were also verified in addition to our previous report [1]. As a result, we believe that the most of key components for ultimate cell height scaling of 3DSFET has been verified to continue the logic technology scaling beyond 1nm node.

11:05 AM

T1.3 A confined storage nitride 3D-NAND cell with WL airgap for cell-to-cell interference reduction and improved program performances, Davide Resnati[1], Gianpietro Carnevale[1], Shyam Surthi[1], Chris Carlson[1], Matthew Thorum[1], Terry Kim[1], Emilio Camerlenghi[1], Richard Hill[1] [1]Micron Technology, Inc.

We demonstrated a confined storage nitride (SN) 3D-NAND cell with an innovative process flow including WL airgap formation. Airgaps strongly reduced WL parasitic capacitance which translates into better program time (t_{prog}) performances. A complete device characterization has been carried out on a test memory array. We measured substantial cell-to-cell interference (C2C) improvements and lateral charge loss (LCL) reduction, which make this cell a key enabler of further tier pitch (TP) scaling in future 3D-NAND arrays. Program-erase (PE) window limitations due to trapped charge confinement were also addressed by TCAD modeling, showing that PE window can be recovered by SN film thickness changes with no C2C penalty.

11:30 AM

T1.4 On the extreme scaling of transistors with monolayer MoS_2 channel, Terry Y.T. Hung[1], Wen-Chia Wu[1,2], D. Mahaveer Sathaiya[1], Edward Chen[1], Chen-Feng Hsu[1], Walker Yun[1], Hsiang-Chi Hu[2], Bo-Heng Liu[3], T.Y. Lee[1], Chi-Chung Kei[3], Wen-Hao Chang[2], Jin Cai[1], Jeff Wu[1], Chung-Cheng Wu[1], H.-S. Philip Wong[1], Chao-Hsin Chien[2], Chao-Ching Cheng[1], Iuliana P. Radu[1] [1]TSMC, [2]NYCU, [3]TIRI

2D transition metal dichalcogenides (TMDs) show promise for transistor scaling, but their on-scale performance had not been proven yet. This work demonstrates contact length (L_C) scaling while holding a low contact resistance (R_C) down to 11 nm. Channel length (L_{CH}) scaling shows I_{ON} can increase down to at least 12 nm with low R_C. The very scaled (L_{CH} = 19 nm and L_C = 12 nm) MoS_2 transistor with Sb-based metal contact has current density of ~1130 mA/mm at V_{DS} = 1 V, and a low R_C of ~190 Ω·mm. These scaled transistors, processed within a back-end-of-line (BEOL) thermal budget, do not exhibit subthreshold swing (S.S.) degradation or observable drain-induced barrier lowering (DIBL) down to L_{CH} = 12 nm.

11:55 AM

T1.5 First Demonstration of Fully Integrated 16 nm Half-Pitch Selector Only Memory (SOM) for Emerging CXL Memory, Myoungsub Kim[1], Yooncheol Bae[1], Jaehyuk Park[1], Jeongho Yeon[1], Hyungjoon Shim[1], Sehyun Jin[1], Hyunsoo Kim[1], Sangchul Oh[1], Gapsok Do[1], Dongyeol Yun[1], Hyung Dong Lee[1], David Ahn[1], Junghun Lee[1], Muhui Park[2], Junghyuk Yoon[2], Jeongho Yi[2], Taekseung Kim[2], Gain Park[2], Seoungju Chung[2], Junho Cheon[2], Sujin Chae[1], Namkyun Park[1], Kyunghoon Kim[2], Dongyean Oh[1], Jaeyun Yi[1], Seonyong Cha[1] [1]R&D, SK hynix Inc., [2]DRAM Development, SK hynix Inc.

In this study, understanding the switching mechanisms of selector only memory (SOM) led to implementation of TCAD, and advanced materials and processes were developed based on the optimized core circuit design and write-read scheme in the first fully integrated 16 nm half-pitch SOM for emerging Compute Express Link™ (CXL) memory. We have achieved read window margin (RWM, 750 mV) including product-level raw bit error rate (RBER) and reliability such as drift-related persistency, read disturbance (RDT), high temperature data retention (>10 years at 125 ℃) and cycle endurance (For median values, read $>10^9$, write $>10^8$, and write $>10^7$ cycles for RBER 200 ppm).

Session C1: Wireline Circuits

10:15 AM, Honolulu 1

Co-Chairs: Harold Pilo, Synopsys
Hisakatsu Yamaguchi, Fujitsu Ltd.

10:15 AM

C1.1 A 246-fJ/b 13.3-Tb/s/mm Single-Ended Current-Mode Transceiver with Crosstalk Cancellation for Shield-Less Short-Reach Interconnect, Jaeho Lee[1], Kyongsu Lee[1], Jae-Yoon Sim[1], Seon-Kyoo Lee[1] [1]POSTECH

This paper presents a 20-Gb/s/line current-mode transceiver for dense short-reach on-chip interconnect. The transceiver achieves a systematic crosstalk cancellation by balancing the crosstalk induced by capacitive and inductive coupling. The transceiver implemented in a 40nm CMOS technology shows an energy efficiency of 246fJ/b and an edge bandwidth density of 13.3Tb/s/mm.

10:40 AM

C1.2 A 2 X 56 Gb/s Single-Ended Orthogonal PAM-7 Transceiver with Encoder-Based Channel-Independent Crosstalk Cancellation in 28-nm CMOS, Xuxu Cheng[1], Hongzhi Wu[1], Liping Zhong[1], Weitao Wu[1], Quan Pan[1] [1]Southern University of Science and Technology

This paper presents a 2 × 56 Gb/s single-ended transceiver (TRX) with a channel-independent crosstalk cancellation scheme. The encoder-based crosstalk cancellation scheme (EB-XTC) encodes 2 uncorrelated PAM-4 signals to a pair of orthogonal PAM-7 signals that eliminates strong crosstalk noise in the closely coupled differential channel. The proposed TRX consists of an encoding transmitter (TX) that transmits the orthogonal PAM-7 signal with crosstalk immunity, and a decoding receiver (RX) that recovers the PAM-7 signal to PAM-4 signals. A tailless push-pull driver is proposed to enhance the linearity and signal-to-noise ratio (SNR) of the PAM-7 signal. The prototype chips are fabricated in 28-nm CMOS and achieve 56 Gb/s/pin with crosstalk immunity up to –2 dB and insertion loss compensation up to 35 dB. The overall power efficiency is 1.8 pJ/b.

11:05 AM

C1.3 A 56-Gb/s 17-mW NRZ Receiver in 0.018 mm^2, Kshitiz Tyagi[1], Behzad Razavi[1] [1]University of California Los Angeles

An NRZ receiver incorporates new architecture and circuit techniques to achieve a low power and area consumption. Realized in 28-nm CMOS technology, the full-rate RX operates at 56 Gb/s with a bit error rate less than 10^{-12} for a channel loss of over 25 dB at 28 GHz.

11:30 AM

C1.4 A 200-Gb/s PAM-4 transmitter with 1.6-Vppd output swing and clock skew correction in 12-nm FinFET, Boyang Zhang*[1,2], Zhifei Wang*[1,2], Zeze Feng[1,2], Tianchen Ye[1,2], Bingyi Ye[1,2], Zixu Wang[1,2], Weixin Gai[1,2]

[1]Peking University, [2]Beijing Advanced Innovation Center for Integrated Circuits

This work demonstrates a 200-Gb/s PAM-4 transmitter with 1.6-Vppd output swing in 12-nm FinFET technology. Novel pulse generators are proposed to reduce jitter by two orders of magnitude. The quadrature clock generator is capable of detecting and correcting three types of clock skews including duty-cycle error, quadrature error, and differential error. The power efficiency of the transmitter is 3.32 pJ/bit and the active area is 0.116 mm^2.

11:55 AM

C1.5 A 0.88pJ/bit 112Gb/s PAM4 Transmitter with 1V_{ppd} Output Swing and 5-Tap Analog FFE in 7nm FinFET CMOS, Zeynep Toprak Deniz[1], Timothy O. Dickson[1], Martin Cochet[1], Jonathan Proesel[2], John F. Bulzacchelli[1], Herschel Ainspan[1], Matthias Braendli[1], Thomas Morf[1], Michael Beakes[1], Mounir Meghelli[1] [1]IBM Reserach, [2]Nubis Communications

A 0.88pJ/bit 112Gb/s PAM4 transmitter is reported in 7nm FinFET CMOS with 1V_{ppd} output amplitude. The quarter-rate TX architecture implements a 5-tap analog FFE using tap extension circuitry, which permits higher FFE tap count than conventional quarter-rate architectures without requiring complex clocking. A key feature of the FFE construction is the use of fully re-assignable CML driver segments among FFE taps, which allows a reduced number of segments for lower capacitance and higher driver bandwidth.

Session C2: Power at High Voltage and Current

10:15 AM, Honolulu 2

Co-Chairs: Stephen Brink, Texas Instruments
Shuichi Nagai, Panasonic Industry Co., LTD

10:15 AM

C2.1 A Monolithic Low-I_{LEAK} Cross-Coupled GaN Driver with ΔΦ-Reduced EMI-Rejecter for 21.51dBμV-EMI-Reduction and 1/10x filter-capacitor, Shi-Jun Zeng[1], Hsing-Yen Tsai[1], Yu-Teng Liang[1], Ke-Horng Chen[1], Kuo-Lin Zheng[2], Chih-Chen Li[3] [1]EE, National Yang Ming Chiao Tung University, [2]Chip-GaN Power Semiconductor Corporation, [3]MediaTek, Hsinchu, Taiwan

The proposed ΔΦ-reduced EMI rejecter reduces the EMI amplitude of 21.51dBμV, passes CISPR25 specification, and reduces the filter capacitor by 1/10 times, thereby reducing the PCB size. The peak efficiency is 94.5%. In a 400V-to-48V conversion, the output power is 240W (=48V*5A) and meets the USB PD 3.1 standard.

10:40 AM

C2.2 A Monolithic GaN-based Gate Driver for LLC-SRC with Three-Phase Startup Clamping Achieving 23.2μA I_Q and 98.6% Peak Efficiency, Chi-Yu Chen[1], Tz-Wun Wang[1], Po-Jui Chiu[1], Sheng-Hsi Hung[1], Chang-Lin Go[1], Xiao-Quan Wu[1], Yu-Ting Huang[1], Ke-Horng Chen[1], Kuo-Lin Zheng[2], Ying-Hsi Lin[3], Shian-Ru Lin[3], Tsung-Yen Tsai[3] [1]EE, National Yang Ming Chiao Tung University, [2]Chip-GaN Power Semiconductor Corporation, [3]Realtek Semiconductor

To meet Energy Star and 80 Plus Titanium standards, the hybrid gate driver reduces the quiescent current to 23.2μA by reducing GaN leakage current. The auto-precharge technique can reduce the leakage current from a few milliamperes to 60.4μA, resulting in an efficiency greater than 92% at the entire output load.

11:05 AM

C2.3 A Fully Integrated 48-V GaN Driver Using Parallel-Multistep-Series Reconfigurable Switched-Capacitor Bank Achieving 7.7nC/mm² On-Chip Bootstrap Driving Density, Xuchu Mu[1], Yang Jiang[1], Rui Martins[1], Pui-In Mak[1] [1]University of Macau

This work presents a fully integrated switched-capacitor (SC) floating-domain gate driver with enhanced driving capability and reduced charge-sharing loss. The proposed driver employs a reconfigurable SC bank (RSCB) to achieve multistep gate driving and minimized bootstrapping capacitance (C_{BST}) area cost. An autonomous switching control determines the reconfiguration of the proposed RSCB by comparing the sensed gate-to-source transient voltage with a triggering level. Fabricated using a 180-nm SOI BCD process, the prototype supports a switching frequency of up to 6MHz and a 48V input for a half-bridge GaN testbench, occupying only 0.048mm² of on-chip bootstrap capacitance. The measured delivered gate charge over the C_{BST} area reaches up to 7.7nC/mm², making a 38-fold improvement over conventional techniques, also achieving a 16.2 times reduction in the required C_{BST} area compared to prior designs when driving the same power devices.

11:30 AM

C2.4 A ±100A Auto-Calibration Current Sensor with 80V Pulse-Width Modulation Attenuation and 0.15% Gain Error, Yu-Teng Liang[1], Shi-Jun Zeng[1], Yu-Tse Shih[1], Ke-Horng Chen[1], Kuo-Lin Zheng[2], Chih-Chen Li[3] [1]EE, National Yang Ming Chiao Tung University, [2]Chip-GaN Power Semiconductor Corporation, [3]MediaTek, Hsinchu, Taiwan

The proposed in-line current sensor uses a 0.1mΩ sense resistor to achieve high efficiency.It can withstand input voltages up to 80V through a high-voltage chopper and handle large common-mode transients

(20V/ns) through enhanced pulse-width-modulation attenuation stage. The gain error is reduced to within ±0.15%. Input noise density reduces to 12nV/√Hz.

11:55 AM

C2.5 A 12V-to-1V 100A Inverted Pyramid Trans-Inductor Voltage Regulator Converter with 93.6% High Efficiency and Fast Transient Response, Yu-Chen Kuo[1], Ke-Horng Chen[1], Hong-Teng Wu[1], Guan-Ye Chen[1], Kuo-Lin Zheng[2], Chih-Chen Li[3] [1]EE, National Yang Ming Chiao Tung University, [2]Chip-GaN Power Semiconductor Corporation, [3]MediaTek, Hsinchu, Taiwan

This paper proposes an inverted pyramid trans-inductor voltage regulator converter that can offer significant benefits, including extended duty cycle, reduced power loss, and lower voltage stress. It achieves a peak efficiency of 93.6%, a maximum output current of 100A, and attains an 8µs recovery time for a 90A/1µs load transition.

Session C3: AI/ML Accelerators and CiM

10:15 AM, Honolulu 3

Co-Chairs: Jaydeep Kulkarni, University of Texas at Austin
Masano Yamaoka, Hitachi, Ltd.

10:15 AM

C3.1 122.7 TOPS/W Stdcell-Based DNN Accelerator Based on Transition Density Data Representation, Clock-Less MAC Operation, Pseudo-Sparsity Exploitation in 40 nm, Animesh Gupta[1], Japesh Vohra[1], Viveka Konandur Rajanna[1], Massimo Alioto[1] [1]National University of Singapore

A DNN whose activation magnitude is represented by digital transition density is introduced for low energy, under the proposed Dyadic Digital Transition Modulation (DDTM). MAC operations are simplified into transition counting, enabling 1) activation pseudo-sparsity for lower energy, 2) clock-less neuron operation via simple up-down asynchronous counters. >100 TOPS/W in 40 nm stdcell design is on par with recent in-memory DNNs.

10:40 AM

C3.2 FSNAP: An Ultra-Energy-Efficient Few-Spikes-Neuron based Reconfigurable SNN Processor Enabling Unified On-Chip Learning and Accuracy-Driven Adaptive Time-Window Tuning, Ruixin Mao[1], Lin Tang[1], Zihan Xia[1], Zhaomin Zhang[1], Aoyu Shen[1], Yu Long[1], Jinhong Guo[2], Yunpeng He[3], Lai Zhang[3], Shujuan Wang[3], Liang Zhou[1], Liang Chang[1], Shanshan Liu[1], Jun Zhou[1] [1]University of Electronic Science and Technology of China, [2]Shanghai Jiao Tong University, [3]Chipintelli Technology Co., Ltd

This paper presents an ultra-energy-efficient few-spikes-neuron (FSN) based reconfigurable spiking neural network (SNN) processor enabling unified on-chip learning and accuracy-driven adaptive time-window tuning. Fabricated in 55nm CMOS process, the proposed design outperforms state-of-the-art designs in accuracy, energy efficiency (up to ×84) and speedup (up to ×740) for same or similar application tasks.

11:05 AM

C3.3 ETCIM: An Error-Tolerant Digital-CIM Processor with Redundancy-Free Repair and Run-Time MAC and Cell Error Correction, Yiqi Wang[1], Zhen He[1], Chenggang Zhao[1], Zihan Wu[1], Mingyu Gao[1], Huiming Han[1], Shaojun Wei[1], Yang Hu[1], Fengbin Tu[2], Shouyi Yin[1] [1]Tsinghua University, [2]The Hong Kong University of Science and Technology

This work presents an Error-Tolerant digital Computing-in-Memory (CIM) processor ETCIM. It has three key features to solve the hard error correction overhead, soft error correction incompatibility and latency problem of traditional methods on digital CIM: 1) A Fault-Adaptive CIM Initializer (FACI) and input feeder reduce the hard error repair overhead by up to 8.47x power and 18.16x area savings. 2) A Block-wise ECC

(BW-ECC) CIM suits digital CIM's structure and corrects soft multiply-accumulation (MAC) errors; 3) A Progressive Cell Error Corrector (PCEC) hides soft cell error correction latency during computation, reducing the total latency by up to 96.8%.

11:30 AM

C3.4 A 28nm 4170-TFLOPS/W/b and 195-TFLOPS/mm^2/b Multiply-Free Fully-Digital Floating-Point Compute-In-Memory Macro with Mitchell's Approximation, Ruiqi Guo[1], Xiaofeng Chen[1], Lei Wang[1], Fengbin Tu[2], Shaojun Wei[1], Yang Hu[1], Shouyi Yin[1] [1]Tsinghua University, [2]Hong Kong University of Science and Technology

This work presents a SRAM-based digital-domain compute-in-memory (DCIM) macro with three contributions: 1) A floating-point DCIM structure to convert bit-serial multiplication into bit-parallel addition by Mitchell Approximate Multiply (MAM); 2) A Mitchell MAC unit with optimized full-adder, adder-tree and 2's complement unit to achieve higher area efficiency; 3) A DCIM bank with latches to save dynamic power by exploiting sparse MAM results. The fabricated 28-nm DCIM achieves 65.15 TFLOPS/W energy efficiency and 3.04 TFLOPS/mm^2 area efficiency for BF16; it is 4170TFLOPS/W/b, 195TFLOPS/mm^2/b, normalized per bit.

11:55 AM

C3.5 A 278-514M Event/s ADC-Less Stochastic Compute-In-Memory Convolution Accelerator for Event Camera, Jiyue Yang[1], Alexander Graening[1], Wojciech Romaszkan[1], Vinod Kurian Jacob[1], Puneet Gupta[1], Sudhakar Pamarti[1] [1]University of California, Los Angeles

We present a Compute-In-Memory (CIM) convolution accelerator for object tracking applications using event camera, which is a new imaging technology that significantly improves latency and dynamic range over conventional cameras. Previous works proposed an efficient ADC-less Stochastic CIM for deep learning but need to store 2^N stochastic bits for an n-bit number. We propose to store binary numbers in memory and convert them to stochastic bits by in-situ Stochastic Number Generators on the fly, which reduce the storage requirement by >10x. The CIM macro embeds 32 tiny MAC units per weight and uses an early termination technique to skip unnecessary computation of zeros. The accelerator achieves energy efficiency of 485 TOPS/W and throughput of 278-514 Mevent/s. The proposed SCIM macro can also be used to accelerate convolution in most deep learning applications.

Session T2: Non-Volatile Memory Technology - Hafnia Based Ferroelectrics-1

1:30 PM, Tapa 1

Co-Chairs: Elisa Vianello, CEA-Leti
Deoksin Kil, SK hynix Inc.

1:30 PM

T2.1 HZO-based Nonvolatile SRAM Array with 100% Bit Recall Yield and Sufficient Retention Time at 85 &[deg]C, Yusuke Shuto[1], Jun Okuno[1], Tsubasa Yonai[1], Ryo Ono[1], Peter Reinig[2], Maximilian Lederer[2], Konrad Seidel[2], Ruben Alcala[3], Thomas Mikolajick[3,4], Uwe Schroeder[3], Taku Umebayashi[1], Kentaro Akiyama[1] [1]Sony Semiconductor Solutions Corp., [2]Fraunhofer IPMS, [3]NaMLab gGmbH, [4]TU Dresden

For the first time, a 16-Kbit nonvolatile SRAM (NVSRAM) array based on a metal/ferroelectric/metal capacitor using a sub-10-nm-thick $HfZrO_x$ (HZO) layer has been experimentally demonstrated to obtain 100% bit yield. This capacitor is formed using the same integration process as that of a previously developed ferroelectric random-access memory (FeRAM) array on the same wafer. Its sequential operations of nonvolatile data store (Store), cutoff of power supply (power-gating: PG), and data recall (Recall) are completely executed employing a robust Recall sequence, achieving 100%-bit recall after a

200-s PG period at 85 ˚C even with sufficiently low operation voltage. The results indicate that our HZO-based NVSRAM and FeRAM hybrid memory system can provide ultra-low power advantages in a System-on-Chip for Internet of Things edge computing.

1:55 PM

T2.2 Polar axis orientation control of hafnium-based ferroelectric capacitors with *in-situ* AC electric bias during rapid thermal annealing, Zhaomeng Gao[1], Tianjiao Xin[1,2], Kai Du[3], Qiwendong Zhao[1], Yiwei Wang[1], Cheng Liu[1], Yilin Xu[1], Rui Wang[1], Guangjie Shi[1], Yunzhe Zheng[1], Yonghui Zheng[1,4], Yan Cheng[1,2,4], Hangbing Lyu[3,5]
[1]East China Normal University, [2]Shanghai Institute of Microsystem and Information Technology (CAS), [3]Huawei Technologies Co., [4]Hualu Technologies Co., [5]Institute of Microelectronics (CAS)

Hafnium-based ferroelectric (FE) thin films, prepared via atomic layer deposition (ALD), suffered from random oriented polar axis (PA), posing challenges and complexities for device scaling and variation. To effectively control the PA orientation and enhance polarization, we employed *in-situ* AC electric bias (E) during rapid thermal annealing (RTA) treatment (i.e. RTA+E). The main findings are as follows: (1) The PA of the FE phase is stochastic formed during RTA cooling stage from tetragonal (T-) to orthogonal (O-) transition; (2) Applying E during cooling significantly enhances polarization in hafnium-based FE capacitors up to ~121.6% increase; (3) The RTA+E method effectively controls the O-PA orientation towards the out-of-plane E direction. These findings solidly demonstrate that the PA orientation of O-grain can be controlled in fluorite-type FE thin films.

2:20 PM

T2.3 In-depth Analysis of the Hafnia Ferroelectrics as a Key Enabler for Low Voltage & QLC 3D VNAND Beyond 1K Layers: Experimental Demonstration and Modeling, Giuk Kim[1], Hyojun Choi[1], Hunbeom Shin[1], Sangho Lee[1], Sangmok Lee[1], Yunseok Nam[1], Minhyun Jung[1], Ilho Myeong[2], Kijoon Kim[2], Suhwan Lim[2], Kwangsoo Kim[2], Wanki Kim[2], Daewon Ha[2], Jinho Ahn[3], Sanghun Jeon[1] [1]KAIST, [2]Samsung Electronics, [3]Hanyang University

In this work, we experimentally demonstrate a remarkable performance improvement, boosted by the interaction of charge trapping & ferroelectric (FE) switching effects in metal-band engineered gate interlayer (BE-G.IL)-FE-channel interlayer (Ch.IL)-Si (MIFIS) FeFET. The MIFIS with BE-G.IL (BE-MIFIS) facilitates the maximized **'positive feedback'** (Posi. FB.) of dual effects, leading to low operation voltage (V_{PGM}/V_{ERS}: +17/-15 V), a wide memory window (MW: 10.5 V) and negligible disturb at a biased voltage of 9 V. Furthermore, our proposed model verifies that the performance enhancement of the BE-MIFIS FeFET is attributed to the intensified posi. FB. This work proves that the hafnia FE can play as a key enabler in extending the technology development of 3D VNAND, which is currently approaching a state of stagnation.

2:45 PM

T2.4 Unveiling Cryogenic Performance (4 to 300 K) towards Ultra-thin Ferroelectric HZO: Novel Kinetic Barrier Engineering and Underlying Mechanism, Dong Zhang[1], Yang Feng[1,2], Zijie Zheng[1], Chen Sun[1], Qiwen Kong[1], Gan Liu[1], Zuopu Zhou[1], Jixuan Wu[2], Jiezhi Chen[2], Xiao Gong[1] [1]Department of Electrical and Computer Engineering, National University of Singapore (NUS), 117576, Singapore, [2]School of Information Science and Engineering, Shandong University, 266237 Qingdao, China

We perform comprehensive and in-depth investigation into the cryogenic characteristics of FE HZO thin films with varying thicknesses (3/5/7/10 nm) across a temperature range (4~300 K), assisted by first-principle calculations as well as extensive material and electrical characterizations. We propose and experimentally demonstrated, for the first time, an innovative cryogenic barrier engineering approach for P_r enhancement, particularly valuable for ultra-thin HZO films.

Session JFS1: RF, mmWave, and THz Technologies
1:30 PM, Tapa 2

Co-Chairs: Bogdan Staszewski, University College Dublin
Rihito Kuroda, Tohoku University

1:30 PM
JFS1.1 First Radio-Frequency Circuits fabricated in top-tier of a full 3D Sequential Integration Process at mmW for 5G applications, Jose Lugo-Alvarez[1], Jean-Baptiste David[1], Alexandre Siligaris[1], Vincent Puyal[1], Guillaume Moritz[1], Tadeu Mota-Frutuoso[1], Valerie Lapras[1], Claire Fenouillet-beranger[1], Laurent Brunet[1], Pierre Vincent[1], Didier Lattard[1], Xavier Garros[1], Francois Andrieu[1], Perrine Batude[1] [1]CEA-Leti
This work describes for the first time, RFIC stacked at the top-tier of a 3D sequential integration. The analog silicon RF circuits, sequentially fabricated at 500°C above a digital circuit layer with 28nm FDSOI industrial platform, present performance in line with standard thermal budget FDSOI devices. Thanks to this advanced 3DSI stack, top-tier VCO and LNA functional demonstrators are designed in the 30 GHz band. Additionally, a signal integrity study is carried out using a ring oscillator aggressor, integrated on bottom-tier below the VCO core, highlighting the interoperability of an aggressive vertical co-integration between fast digital and RF blocks. This work provides insights into the crosstalk issue arising from the ultra-thin distance between tiers, a characteristic feature of 3DSI.

1:55 PM
JFS1.2 A 140-Gbps 1-to-21GHz Ultra-Wideband LNA Achieving 1.95-to-3dB NF Using Gm-Assisted-Feedback Noise Suppression Technique in 40nm Bulk CMOS, Sicheng Han[1], Yun Wang[1], Yunhao Li[1], Wen Zuo[1], Wei Li[1], Yue Lin[2], Hongtao Xu[1] [1]Fudan University, [2]ICLegend Micro
This paper presents an ultra-wideband low-noise amplifier (LNA) with gm-assisted-feedback noise suppression technique for ultra-wideband RF front-end. Compared to the traditional resistive feedback wideband LNAs, the proposed LNA blocks the noise current from the feedback resistor with a simple additional gm-cell, thus achieving a lower overall NF. A source coupling transformer is also utilized to maintain a wideband flat gain. Fabricated in a 40-nm bulk CMOS process, the LNA prototype achieves a measured bandwidth of 1-to-21-GHz, NF of 1.95-to-3-dB, S21 of 20.6-to-22.4-dB, while consuming 21.6 mA from a 1.2 V power supply. It reports the lowest and the flattest NF among the recent-published bulk CMOS ultra-wideband LNAs, it also supports ultra-wideband modulation signal with a date rate of 140 Gbps.

2:20 PM
JFS1.3 First Heterogeneous and Monolithic 3D (HM3D) Integration of InGaAs HEMTs and InP/InGaAs DHBTs on Si CMOS for Next-Generation Wireless Communication, Nahyun Rheem[1], Jaeyong Jeong[1], Yoonje Suh[1], Chanjik Lee[1], Bong Ho Kim[1], Joon Pyo Kim[1], Seong Kwang Kim[1,2], Hyeong-Rak Lim[1], Jongmin Kim[3], Dae-Hwan Ahn[4], Jae-Hoon Han[4], Jongwon Lee[5], Sanghyeon Kim[1] [1]KAIST, [2]Semiconductor R&D Center, Samsung Electronics, Co. Ltd, [3]KANC, [4]KIST, [5]Chungnam National University
Heterogeneous and monolithic 3D (HM3D) integration of III-V and Si CMOS technologies enables high-frequency, multifunctionality, and power-efficient RF systems for nextgeneration wireless communication such as 6G and beyond. In this work, for the first time, we demonstrate HM3D integration of InGaAs HEMTs (for LNAs) and InP/InGaAs DHBTs (for PAs) on Si CMOS by direct wafer bonding. The top InGaAs HEMTs exhibit f_T and f_{MAX} of 354 GHz and 611 GHz with a high g_m of 1.5 S/mm. Concurrently, the top InP/InGaAs DHBTs show f_T and f_{MAX} of 129 GHz and 47 GHz with a DC gain of 29 and a breakdown voltage of 5.9V. Notably, these results are obtained without any degradation of the bottom Si CMOS. This

innovative HM3D integration, combining III-V technologies for PAs and LNAs with Si CMOS technology for analog/digital functionalities will play an essential role in next-generation wireless communication systems.

2:45 PM

JFS1.4 Terahertz Sensing with CMOS-RFIC - Feasibility Verification for Short-Range Imaging using 300GHz MIMO Radar (Invited), Ichiro Somada[1], Akihito Hirai[1], Akinori Taira[1], Keigo Nakatani[1], Kazuaki Ishioka[1], Takuma Nishimura[1], Koji Yamanaka[1] [1]Mitsubishi Electric Corp.

For solving various social issues, sensing technology has gained significant interest. Terahertz waves, which combine the high resolution of light and transparency of radio waves, enable visualization of obstacles behind internal structures. So, it offers potential for new solutions. This paper introduces the overview of a short-distance sensing system based on the full digital MIMO radar concept, the design and fundamental evaluation results of 300GHz terahertz CMOS devices, as well as the achievements of imaging using 300GHz terahertz wave based on actual measurements. Since the terahertz band can obtain an ultra-wideband spectrum, several milli-meter resolution imaging can be performed in azimuth, elevation, and depth direction. We show the feasibility of the security gate application with the measured high-resolution tomographic images.

Session JFS2: Processors & Compute

1:30 PM, Tapa 3

Co-Chairs: Yan Li, Western Digital
Noriyuki Miura, Osaka University

1:30 PM

JFS2.1 NeRF-Navi: A 93.6-202.9μJ/task Switchable Approximate-Accurate NeRF Path Planning Processor with Dual Attention Engine and Outlier Bit-Offloading Core, Seryeong Kim[1], Seokchan Song[1], Wonhoon Park[1], Junha Ryu[1], Sangyeob Kim[1], Gwangtae Park[1], Soyeon Kim[1], Hoi-Jun Yoo[1][1]KAIST

A Neural Radiance Field-based Path Planning (NeRF-PP) processor (NeRF-Navi) is proposed for fast and energy-efficient 3D navigation with 3 key features: 1) Dual Attention Neural Path Planning (DANP) engine for fast and energy-efficient NeRF-PP acceleration, 2) Approximate-Accurate (A^2) core with error compensation reduction tree (ECRT) and bit sparsity boosting logic (BSBL) for low power computation, 3) Outlier Channel Bit Offloading Core (OCBOC) for throughput enhancement. NeRF-Navi is fabricated in a 28nm CMOS process and evaluated in the 3D real-world map. As a result, NeRF-Navi successfully demonstrates real-time NeRF-PP on edge devices consuming only 93.6-202.9 μJ/task with 0.57-1.39 ms latency at 0.9V and 200MHz.

1:55 PM

JFS2.2 CogniVision: End-to-End SoC for Always-on Smart Vision with mW Power in 40nm, Animesh Gupta[1,1], Japesh Vohra[1], Massimo Alioto[1] [1]National University of Singapore

A full vision system on chip with hierarchical execution from sensor to AI and communications is presented. Always-on system power is aggressively reduced to the mW level through activity reduction, gating any subsequent vision pipeline stage starting from the lowest semantic level of the scene. The system comprises an imager with dual-architecture in/near-sensor saliency detection, on-the-fly novelty detection, DNN with on-chip scheduler for weight memory reduction, WiFi transmitter, wake-up receiver for cloud-pushed DNN model update and software programmable orchestration via RISC-V. Average 2.1-mW power at 30 fps is achieved with a SqueezeNet V1.0 model running entirely on chip.

2:20 PM

JFS2.3 A Quad-Core AI Processing Unit for Generative AI in 4nm 5G Smartphone SoC (Invited), Chien-Hung Lin[1], Jeng-Yun Hsu[1], Cheng-Ying Yu[1], Chia-Wei Hsu[1], Yi-Min Tsai[1], Kuo-Sheng Wu[1], Chung-Lun Huang[1], Meng-Han Hsieh[1], Tsung-Yao Lin[1] [1]MediaTek Inc.

This work presents the quad-core AI processing unit (APU) for efficient execution of generative artificial intelligence (GenAI) applications on smartphones. GenAI applications featured with billions of computations and memory accesses are out of tune with smartphone platforms. The APU applies mixed-precision and hybrid-precision operations, inter-core direct data link, zero-overhead layer fusion, and data broadcasting to reduce 50% of dram footprint and 90% of dram BW. The 4nm 5G smartphone powered by the APU takes less than 1 second to generate an image with optimized stable diffusion (SD) and outputs more than 20 tokens per second with 7B speculative large language model (LLM).

2:45 PM

JFS2.4 AMD Instinct™ MI300X Accelerator: Packaging and Architecture Co-Optimization (Invited), Alan Smith[1], Gabriel Loh[1], John Wuu[1], Samuel Naffziger[1], Tyrone Huang[1], Hugh McIntyre[1], Ramon Mangaser[1], Wonjun Jung[1], Raja Swaminathan[1] [1]AMD

The AMD Instinct™ MI300X accelerator utilizes multiple advanced packaging technologies for a heterogeneous integration solution for emerging AI/ML and HPC workloads. These include microbump 3D memory stacks, 2.5D silicon interposers, and 3D hybrid bonding. The combination of these advanced packaging technologies enabled architectural innovations and generational performance uplifts that cannot be achieved with traditional technologies and Moore's Law scaling A modular 3D chiplet design also enables reuse of the MI300X components to enable the MI300A APU.

Session C4: Biomedical Stimulation and Imaging

1:30 PM, Honolulu 1

Co-Chairs: Carolina Mora Lopez, imec
Kenichi Matsunaga, NTT Corporation

1:30 PM

C4.1 A Wireless Neurostimulator using Body-Coupled Link for Multisite Stimulation in Freely Behaving Animals, Taejune Jeon[1], Byeongseol Kim[2], Changuk Lee[3], Danbi Ahn[4], Daerl Park[1], Jaesuk Sung[5], Hee Young Kim[6], Heon-Jin Choi[1,5], Joonsung Bae[2], Youngcheol Chae[1] [1]Yonsei University, [2]Kangwon National University, [3]University of California, [4]Daegu Haany University, [5]NFormare, [6]Yonsei University College of Medicine

This paper presents a wireless neurostimulators for multisite stimulation in freely behaving animals. The neurostimulator IC is wirelessly powered via a 16MHz body-coupled link, and controlled by forward telemetry, which provides stimulation parameters via amplitude shift keying (ASK) modulation. It can provide various stimulation protocols with a maximum current of 225µA, achieving the highest end-to-end efficiency of 1.72% at a TX/RX distance of 10cm. Moreover, multisite stimulation is fully validated through *in vivo* experiments.

1:55 PM

C4.2 A Current-Source-Free Constant-Current Wireless Adiabatic Neural Stimulator Achieving a 5.5-27.7x Improved RF-to-Electrode Stimulation Efficiency Factor, Siddharth Agarwal[1], Gael Pillonnet[2], Hongyu Lu[1], Nader Sherif Kassem Fathy[1], Patrick P. Mercier[1] [1]University of California, San Diego, La Jolla, CA, [2]Univ. Grenoble Alpes, CEA, Leti, Grenoble

This paper presents a wireless neurostimulator that combines the features of rectification, regulation, voltage boosting, and current generation into a single inductor-less power stage, which eliminates both cascaded losses and current source losses while enabling direct adiabatic driving of a wide range of electrode impedances (80nF-to-2μF + 10Ω-to-2kΩ). The stimulator replenishes 99.5% of the energy stored in the inherent electrode capacitance and balances pre-shorting residual charge to under 0.5% (0.6nC) for 50μA-to-2mA stimulation currents. It achieves an RF-to-Electrode Stimulation Efficiency Factor ($SEF_{RF\text{-}to\text{-}Electrode}$) of 11.1, which exceeds prior art by 5.5-27.7x.

2:20 PM

C4.3 A 5.7kfps Fast Neural Electrical Impedance Tomography IC Based on Incremental Zoom Structure with Baseline Cancellation for Peripheral Nerve Monitoring Systems, Ji-Hoon Suh[1], Haidam Choi[1], Yoontae Jung[1], Sohmyung Ha[2], Minkyu Je[1] [1]KAIST, [2]New York University Abu Dhabi

Fast electrical impedance tomography (EIT) can localize and record neural activities of peripheral nerves in real time, but prior EIT systems do not support high enough frame rate (<500fps) to catch neural activities. Towards the real-time neural EIT, we propose a power- and hardware-efficient EIT system based on baseline-cancelling incremental zoom structure with 47μW and 0.055mm^2/ch, and a novel image update scheme, focused refresh, boosting the frame rate to 5.7kfps.

2:45 PM

C4.4 A Fully Dynamic 1st-Order 1st-Order Δ-ΔΣ Modulator with a 468mVInput Range for Electrical Impedance Tomography Systems, Haidam Choi[1], Gichan Yun[1], Ji-Hoon Suh[1], Sein Oh[1], Song-I Cheon[1], Yoontae Jung[1], Sohmyung Ha[2], Minkyu Je[1] [1]KAIST, [2]New York University Abu Dhabi

This paper presents an imaging IC with readout front-ends (RFEs) based on a 1st-order Δ-ΔΣ modulator (Δ-ΔΣM) for electrical-impedance-tomography (EIT) systems. This allows the utilization of the readout data from all the electrodes, including even the current-injecting electrodes, without saturation, thus achieving much higher imaging contrast. The proposed EIT system achieves an input range of 468 mV_{pp}, corresponding to 1.56 kΩ when using a maximum current of 150 μA.

Session C5: Analog Techniques

1:30 PM, Honolulu 2

Co-Chairs: Axel Thomsen, Cirrus Logic
Chun Shiah, Etron Technology

1:30 PM

C5.1 A 15.4ppm/ºC GaN-based Voltage Reference with Process-Variation-Immunity and High PSR for EV Power Systems, Po-Jui Chiu[1], Tz-Wun Wang[1], Chi-Yu Chen[1], Sheng-Hsi Hung[1], Yu-Ting Huang[1], Xiao-Quan Wu[1], Ke-Horng Chen[1], Kuo-Lin Zheng[2], Chih-Chen Li[3] [1]EE, National Yang Ming Chiao Tung University, [2]Chip-GaN Power Semiconductor Corporation, [3]MediaTek, Hsinchu, Taiwan

The proposed GaN-based voltage reference generator has a low temperature coefficient (TC) of 15.4ppm/°C, a small deviation of V_{REF} at different process corners with a standard deviation of 0.22%, a great line sensitivity of 0.0023%/V, and a great power-supply rejection (PSR) of -187dB and -114dB at 100Hz and 50MHz, and10.9μW.

1:55 PM

C5.2 A 97.3dB SNR Bioimpedance AFE with -84dB THD Segmented-ΔΣM Sinusoidal Current Generator and Passing-Through Instrumentation Amplifier, Qinjing Pan[1], Qi Luo[1], Tianxiang Qu[1], Liheng Liu[1], Xiao Li[2], Min Chen[2], Zhiliang Hong[1], Jiawei Xu[1] [1]Fudan University, Shanghai, China, [2]CHIPSEA, Shenzhen, China

This paper presents a high-precision bioimpedance (BioZ) analog front-end (AFE) to detect changes in tissue electrical properties as prognostic indicators for heart failure, cancer, and chronic pulmonary disease. To increase the BioZ measurement accuracy, a low-distortion sinusoidal current generator (CG) is proposed. It utilizes a lookup table (LUT) with segmented delta-sigma modulator (ΔΣM) for efficient bits extension of the IDAC, and a current amplifier (CA) to isolate the IDAC from dynamic load (e.g., BioZ, electrode impedance, and parasitic capacitors) without nonlinearity penalty. The BioZ readout proposes a pass-through IA (PT-IA) to optimize the noise performance for large and complex BioZ. Manufactured in a 0.18µm CMOS process, the overall AFE, including the CG and readout, achieves -84dB THD, 97.3dB SNR (BW=4Hz), and 0.57mΩ/√Hz sensitivity at 1Hz, while the CG and readout consume 86.7-196.5µW and 54.8µW, respectively. Impedance cardiography (ICG) has been successfully demonstrated with dry electrodes.

2:20 PM

C5.3 A 5.8W, 0.00086% THD+N, 118dB PSRR Class-D Audio Amplifier with Passive Output Common-Mode Compensation Technique for Wide Output Power Range, Inhwan Cho[1], Moo-Yeol Choi[1], Jaehyeok Byun[1], Ji-Hun Lee[1], Myungjin Lee[1], Dongsu Kim[1], Jongwoo Lee[1] [1]Samsung Electronics

This paper presents a Class-D audio amplifier (CDA) with a passive output common-mode compensation (POCMC) technique for high linearity over a wide output power range. Moreover, a complementary tri-wave common-mode feedback (CTRI-CMFB) is also proposed to improve PSRR. The CDA achieves 0.00086% THD+N, 118dB PSRR, and a maximum output power of 5.8W (THD+N=1%) with an efficiency of 93.2% on an 8Ω load. The chip was fabricated in a 0.13µm BCD process and occupies an active area of 1.46mm^2.

2:45 PM

C5.4 Current Mirrors with Tapered Stacked-Gates for Area Saving or Noise Improvement in 3nm FinFET Process, Chu-En Hsia[1], Yung-Shun Chen[1], Chin-Ho Chang[1], Benny Lai[1], Ching Lin Jen[1], Yung-Chow Peng[1], Victor Li[1] [1]Taiwan Semiconductor Manufacturing Company

A tapered stacked-gates device offers the advantages of saving area and reducing noise and mismatch, and it is universally applicable to many circuits. The proposed current-mirror design in bandgap reference (BGR) and current control oscillator (ICO) circuits use tapered stacked-gates for current mirror. Different numbers of transistors are used in the stacked stages, which reduces the number of source-side transistors and results in a 24% area reduction while maintaining the same mismatch and noise performance according to experimental result. In addition, using the same number of devices, this design can achieve better performance with almost 45% noise and 28% mismatch reduction in simulation. Overall, this non-formal stacked-gates transistor circuit design shows promising potential for analog circuit applications.

Session C6: SPAD Sensors

1:30 PM, Honolulu 3

Co-Chairs: Bruce Rae, STMicroelectronics
Tomohiro Takahashi, Sony Semiconductor

1:30 PM

C6.1 3D-Stacked 1Megapixel Time-Gated SPAD Image Sensor with 2D Interactive Gating Network for Image Alignment-Free Sensor Fusion, Kazuhiro Morimoto[1], Naoki Isoda[1], Hiroshi Sekine[1], Tomoya Sasago[1], Yu Maehashi[1], Satoru Mikajiri[1], Kenzo Tojima[1], Mahito Shinohara[1], Ayman Tarek Abdelghafar[1],

Hiroyuki Tsuchiya[1], Kazuma Inoue[1], Satoshi Omodani[1], Kazuma Chida[1], Alice Ehara[1], Junji Iwata[1], Tetsuya Itano[1], Yasushi Matsuno[1], Katsuhito Sakurai[1], Takeshi Ichikawa[1] [1]Canon Inc.
We present a 5µm-pitch, 3D-BSI 1Mpixel time-gated SPAD image sensor with 2D interactive gating network, enabling image alignment-free sensor fusion. The SPAD image sensor operates at 1,310fps for global shutter 2D imaging, and event vision sensing with 0.76ms temporal resolution under 0.02lux. Range-gated imaging result demonstrates a feasibility of robust imaging under harsh environments. The proposed gating network architecture enables background suppression in 3D depth measurement under 50klux ambient light.

1:55 PM

C6.2 A 512 x 512 SPAD Laser Speckle Autocorrelation Imager in Stacked 65/40nm CMOS, Robert K. Henderson[1], Francesco Mattioli Della Rocca[1,2], Edbert J. Sie[3], Ahmet T. Erdogan[1], Lars Fisher[1], Andrew B Matheson[1], Neil Finlayson[1], Alistair Gorman[1], Istvan Gyongy[1], Hanning Mai[1,2], Thierry Lachaud[4], Russell Forsyth[4], Francesco Marsili[3] [1]University of Edinburgh, [2]now with Sony Europe Technology Centre, [3]Meta Platforms Inc., [4]STMicroelectronics
We present a single-photon avalanche diode (SPAD) autocorrelation imager implemented in 65/40nm 3D-stacked CMOS for laser speckle blood flow monitoring. The shared per-pixel SRAM architecture provides a compact 41.68 mm pitch 128x128 resolution parallel autocorrelation function operating at 0.5T Op/s and a lag-time of 1ms. SNR gains due to high BSI SPAD NIR sensitivity and on-chip averaging extends source-detector separation to 40 mm indicative of the sensitivity required to discriminate extracerebral artifacts from deep-tissue blood flow in future wearable neuromonitoring systems.

2:20 PM

C6.3 A Digital Dynamic Vision Sensor with SPAD pixels and Multi-Event Generation for Motion/Vibration-Adaptive Detection, Houk Lee*[1], Jinpyo Han*[1], Junhee Cho[2], Heesung Lee[2], Seong-Jin Kim[3], Jung-Hoon Chun[1,2], Jaehyuk Choi[1,2] [1]Sungkyunkwan University, [2]SolidVue, [3]UNIST
This paper introduces a digital dynamic vision sensor (DVS) with single-photon avalanche diode (SPAD). The sensor operates in a fully digital manner, eliminating circuit noise and non-uniformity. To provide a motion-adaptive optimum frame rate and minimize vibration-event noise (VEN) caused by sensor vibrations, the sensor generates multiple events via quantized delta (QD) signal. Thanks to the QD, the sensor detects the relative speed of moving objects, adjust the frame rate accordingly, and filter out VEN, thereby allowing only essential events from the objects. Furthermore, the sensor incorporates event-driven threshold control (EDTC) logic to ensure the optimal number of events. The EDTC and VEN filter offers data reduction of 72.8% and 64.5%, respectively.

2:45 PM

C6.4 A 7.2 inch 5.5M pixel 600mW SPAD X-ray Detector with 116.7 dB Dynamic Range, Byungchoul Park[1], Hyun-seung Choi[2], Jinwoong Jeong[3], Jimin Cheon[4], Myung-Jae Lee[2], Youngcheol Chae[1] [1]Yonsei University, [2]Korea Institute of Science and Technology, [3]Rayence, [4]Kumoh National Institute of Technology
This paper presents the *first* 7.2-inch wafer-level SPAD X-ray detector for radiography and industrial applications. A digital SPAD pixel achieves high SNR at low dose and wide DR. Large power consumption of the photon counting at high dose is effectively mitigated by using an extrapolation method, and the overflow flag of the photon counter is flexibly selected for further power reduction. High throughput is achieved with a pipelined readout chain of the pixel output. Implemented in a 65nm CMOS process, the detector consists of 3296×1680 pixels with a pixel pitch of 49.5µm, corresponding to an area of 16.5× 8.9cm^2, and consumes only 600mW at 13frames/s, while achieving a DR of 116.7dB. The detector’s global

shutter operation delivers high-quality images without motion artifacts. Excellent radiation hardness of up to 10,000Gy is also achieved.

Session JFS3: Thermal Management and Power Delivery in 3D Integration
3:25 PM, Tapa 1

Co-Chairs: Russell McMullan, AMD
Sun-Wan Hong, Sogang University

3:25 PM
JFS3.1 Co-Optimization for Robust Power Delivery Design in 3D-Heterogeneous Integration of Compute In-Memory Accelerators (Invited), Madison Manley[1], Ankit Kaul[1], James Read[1], Yandong Luo[1], Xiaochen Peng[1], Shimeng Yu[1], Muhannad Bakir[1] [1]Georgia Institute of Technology
In this work, we quantify the impact of power supply noise (PSN) in 3D-HI architectures on the errors in ADC and RRAM array outputs and optimize the 3D PDN and ADC designs to maximize inference accuracy in compute-in-memory (CIM) hardware. We propose a device-HI-application-level evaluation methodology to evaluate the impact of PDN design parameters on CIM inference accuracy. For our assumed 3D CIM hardware, an areal distribution of through-silicon vias (TSVs) and µ-bumps, and a fine-tuned PSN-aware successive approximation register-ADC (SAR-ADC) achieves a 90% inference accuracy compared to 47% with a baseline 3D design at iso-power and iso-area. These insights can be useful for multi-die design convergence for edge intelligent CIM chips.

3:50 PM
JFS3.2 3DIC System-Technology Co-Optimization with a Focus on the Interplay of Thermal, Power, Timing, and Stress Effects (Invited), Victor Moroz[1], Xiaopeng Xu[1], Alexei Svizhenko[1], Xi-Wei Lin[1], Sergey Popov[1], Henry Sheng[1], Kenneth Larsen[1] [1]Synopsys
3DIC chiplet stacking is taking the industry by storm. It provides huge benefits in terms of logic-to-memory connection bandwidth expansion, power reduction, and manufacturing cost reduction. However, it brings a number of new challenges that have to be addressed to make 3DIC solutions successful. First, we look at the bigger picture of diverse STCO factors that have to be resolved, and then focus on the interplay of four effects that play a key role in 3DIC designs: thermal, power, timing, and stress, and show their interplay. Careful analysis and balance of all four major factors are necessary to pull off a successful 3DIC solution.

4:15 PM
JFS3.3 Package - System Thermal Modeling and New Material (Invited), Tsung-Yu Chen[1], Tsung-Yu Chen[1], Kris Chuang[1], Wensen Hung[1], Tsung-Shu Lin[1], Yen-Ming Chen[1] [1]Taiwan Semiconductor Manufacturing Company
A holistic Die-Package-System level thermal modeling methodology incorporating local details, global features and new material adoption are undoubtedly a key enabler to unleash the innovations of future advanced packaging technology development. Three key aspects were addressed to demonstrate such capabilities to guide the future 3D Fabric technology roadmap in HPC/AI industry applications such as instance level thermal modeling technique, Lid/Ring package type evaluation and advanced material/process impact to the die-package-system thermal performance. In summary, new material with process-friendly & better thermal conductivity from die level FEoL (front-end) & BEoL dielectric material, package level TIM1 and lid as well as system level TIM1.5 and TIM2 are key knobs to boost overall Die-Package-System thermal performance.

4:40 PM

JFS3.4 Integration and Characterization of High Thermal Conductivity Materials for Heat Dissipation in Stacked Devices, W.-Y. Woon[1], J.-H. Jhang[1], K.-K. Hu[1], C.-C. Shih[1], J.-F. Hsu[1], J.-P. Lin[1], Y. Wu[2], A. Kasperovich[3], M. Malakoutian[3], R. Soman[3], J. Kim[3], H.-K. Wei[1], M. Nomura[2], S. Chowdhury[3], S. Sandy Liao[1]
[1]TSMC, [2]University of Tokyo, [3]Stanford University

Heat dissipation is one of the most imminent performance limiting challenges in new device architectures involving backside power delivery network and 3D-stacking. In this work, we evaluate integration schemes and propose high thermal conductivity materials as heat spreader bonding layer for heat dissipation improvement. Analysis of potential integration issues, investigation of process solutions, and thermal characterization for complex film stacks are presented.

5:05 PM

JFS3.5 High thermal conductivity AlN films for advanced 3D Chiplets, Takeshi Takagi[1], Takeki Ninomiya[1], Masaaki Niwa[1], Soken Obara[1], Takeshi Momose[1], Yukihiro Shimogaki[1], Kasahiro Nomura[1], Hiroshi Fujioka[1], Masakazu Mori[2], Tadahiro Kuroda[1] [1]The Univ. of Tokyo, [2]Ryukoku Univ.

A novel “Cool 3D chiplet” concept is proposed, showcasing remarkable heat dissipation through the integration of aluminum nitride (AlN), an insulating material with high thermal conductivity. We conducted simulations analyzing the thermal impact of AlN as an interlayer dielectric (ILD) for the back-side power delivery network (BSPDN), a TSV insulating film, and a molding material for the packaging. Furthermore, we explored appropriate AlN deposition techniques for each application. The results demonstrate the feasibility of building advanced 3D chiplets with enhanced heat dissipation by employing the AlN in each layer that makes up the 3D chiplet, from the device level to the packaging level.

Session T3: Novel Channel Materials for Advanced CMOS
3:25 PM, Tapa 2

Co-Chairs: Anabela Veloso, imec
Masahiko Kanda, Toshiba Electronic Devices & Storage Corporation

3:25 PM

T3.1 Record Performance in GAA 2D NMOS and PMOS using Monolayer MoS_2 and WSe_2 with scaled contact and gate length, Wouter Mortelmans[1], Pratyush Buragohain[1], Carly Rogan[1], Ande Kitamura[1], Chelsey Dorow[1], Kevin O'Brien[1], Rahul Ramamurthy[1], Jennifer Lux[1], Ting Zhong[1], Shane Harlson[1], Eric Gillispie[1], Tyrone Wilson[1], Adedapo Oni[1], Ashish Penumatcha[1], Mahmut Kavrik[1], Kirby Maxey[1], Azimkhan Kozhakhmetov[1], Chia-Ching Lin[1], Sudarat Lee[1], Andrey Vyatskikh[1], Nazmul Arefin[1], Paul Fischer[1], Joshua Kevek[1], Tristan Tronic[1], Matthew Metz[1], Scott Clendenning[1], Uygar Avci[1] [1]Intel

2D transition metal dichalcogenides are promising candidates as channel material choice in ultimately scaled CMOS. We report record performance in GAA 2D NMOS transistors using monolayer MoS_2 with three advances: scaled gate length (Lg) down to 25nm, scaled contact length (Lc) of 38nm, and the elimination of the low-k “inter-layer” in the gate stack enabling the first fully high-k GAA 2D device. We achieve 90% yield for scaled Lg <50nm with SS of 86mV/dec and on-currents reaching 485µA/µm. Drive currents of 342µA/µm are maintained after contact length scaling down to ~40nm. We report the first BTI on any 2D GAA device and *deposited* high-k interface, showing HfO_2 may be advantageous for 2D reliability compared to typical Al_2O_3 inter-layers. Signs of short-channel effects are observed at the shortest Lg, identifying EOT scaling as essential area of improvement. We also report record ION=92µA/µm in scaled Lg GAA PMOS transistors with monolayer WSe_2.

3:50 PM

T3.2 EOT scaling via 300mm MX_2 dry transfer - Steps toward a manufacturable process development and device integration., Souvik Ghosh[1], Anastasiia Kruv[1], Quentin Smets[1], Tom Schram[1], Damien Leech[1], Taotao Ding[2], Vikram Turkani[3], Benjamin Groven[1], Anish Dangol[1], Gernot Probst[2], Thomas Uhrmann[2], Marcus Wimplinger[2], Inge Asselberghs[1], Cesar Lockhart de la Rosa[1], Steven Brems[1], Gouri Sankar Kar[1] [1]IMEC, [2]EV Group, [3]PulseForge

We demonstrate a low-temperature automation-compatible, and reproducible 300mm MX_2 dry transfer process. We have successfully transferred 300mm WS_2 in a repeatable process flow with >99.5% morphological yield. In-FAB integrated transistors fabricated via this route have >99% electrical yield on best wafers and is comparable to that obtained from analogous direct-grown WS_2 integrated wafers. Further, we also demonstrate back-EOT scaling down to 2nm that is otherwise out of scope via high temperature direct growth. This transfer process facilitates a viable route to implement scaled MX_2 devices for FEOL CFET, and BEOL active circuits.

4:15 PM

T3.3 High Performance Transistor of Aligned Carbon Nanotubes in a Nanosheet Structure, Gregory Pitner[1], Nathaniel Safron[1], Tzu-Ang Chao[1,2], Shengman Li[3], Shreyam Natani[4], San-Lin Liew[1], Carlo Gilardi[1,3], Hsin-Yuan Chiu[1,2], Sheng-Kai Su[1], Andrew Bechdolt[5], Gilad Zeevi[5], Zichen Zhang[4], Matthias Passlack[1], Vincent D.-H. Hou[1], Harshil Kashyap[4], Chao-Hsin Chien[2], Prabhakar Bandaru[4], Andrew Kummel[4], H.-S. Philip Wong[1,3], Subhasish Mitra[3], Iuliana Radu[1] [1]TSMC, [2]NYCU, [3]Stanford University, [4]U.C. San Diego, [5]Stanford

This work demonstrates the first nanosheet FET built on an array of dense aligned carbon nanotubes. In this device structure, the gate surrounds an aligned array of CNTs with ≈3 nm pitch. At a channel length of 70 nm the drive current exceeds 1 mA/µm at -0.5 V V_{DS} with sub-V_T slope of 135 mV/dec, and an I_{MIN} of 76 nA/µm. R_C of 20.5 Ω-µm is extracted by transmission line method. This is record-high performance for transistors with CNT channel. However, reducing D_{IT} and channel variability are necessary to enable energy-efficient CMOS applications.

4:40 PM

T3.4 Achieving 1-nm-Scale Equivalent Oxide Thickness Top Gate Dielectric on Monolayer Transition Metal Dichalcogenide Transistors with CMOS-Friendly Approaches, Jung-Soo Ko[1], Alex Shearer[1], Sol Lee[2], Kathryn Neilson[1], Marc Jaikissoon[1], Kwanpyo Kim[2], Stacey Bent[1], Krishna Saraswat[1], Eric Pop[1] [1]Stanford University, [2]Yonsei University

Two-dimensional (2D) transition metal dichalcogenides (TMDs) are promising for future nanoscale transistors but reducing their gate dielectric equivalent oxide thickness (EOT) remains a key challenge. Here, we report ultrathin top-gate dielectrics on monolayer (1L) TMDs using industry-compatible approaches, achieving 1-nm-scale EOT. We show atomic layer deposition (ALD) of HfO_2 on both 1L MoS_2 and WSe_2 using Si seed, realizing 0.9 nm EOT with subthreshold swing SS ≈ 70 mV/dec, low leakage, and negligible hysteresis on MoS_2. We also demonstrate direct ALD of ultrathin alumina (AlO_x) on 1L MoS_2 with good uniformity and quality by engineering the precursor. Combining our findings, we show that the threshold voltage can be controlled by the thickness of the interfacial dielectric layer on the 2D transistor channel.

5:05 PM

T3.5 Single-crystalline monolayer MoS_2 arrays based high-performance transistors via selective-area CVD growth directly on silicon wafers, Guixu Zhu[1], Xiaodong Zhang[1], Haotian Fang[1], Dongdong Sun[1], Luyang Wang[2], Zujian Dai[1], Lizi Wei[1], Qiuyang Lin[3], Ao Li[1], Yufeng Min[1], Qiuxia Lu[1], Lixin He[1], Dongsheng Song[2], Yuanyuan Shi[1] [1]University of Science and Technology of China (USTC), [2]Anhui University, [3]imec, Leuven, Belgium

Here we present a method that fabricates massive arrays of single-crystalline monolayer (ML) MoS_2-based transistors directly on silicon wafers without a 2D-layer transfer process (2D-LTP). Inspired by epitaxial growth, quasi-terrace Al_2O_3 triangle-arrays are designed on silicon wafers, facilitating selective-area growth (SAG) of single-crystalline ML MoS_2 arrays. The SAG MoS_2 arrays based back-gate (BG) transistors show a maximum mobility of 62.8 cm^2/Vs and I_{on}/I_{off} ratio of 2.5×10^8. The study paves the way for high throughput, Si-compatible, transfer-free, and controllable integration of single-crystalline transition metal dichalcogenides (TMDs) based transistors.

Session T4: Oxide Channel FET for Logic and Memory Applications-1

3:25 PM, Tapa 3

Co-Chairs: Max Shulaker, MIT
Masaharu Kobayashi, The University of Tokyo

3:25 PM

T4.1 Highly Robust All-Oxide Transistors with Ultrathin In_2O_3 as Channel and Thick In_2O_3 as Metal Gate Towards Vertical Logic and Memory, Zehao Lin[1], Zhuocheng Zhang[1], Chang Niu[1], Hongyi Dou[1], Ke Xu[1], Mir Md Fahimul Islam[1], Jian-Yu Lin[1], Changhyuck Sung[2], Minji Hong[2], Daewon Ha[2], Haiyan Wang[1], Muhammad Ashraful Alam[1], Peide Ye[1] [1]Purdue University, [2]Samsung Electronics Co.

In this work, we report for the first time atomic-layer-deposited (ALD) all-oxide transistors toward 3-D vertical integration, with thick ALD In_2O_3 as gate electrodes, and In_2O_3 itself as contact. The all-oxide thin-film transistors (TFTs) show an on/off ratio over 10^6, high uniformity, and very robust reliability with a threshold voltage shift (ΔV_{TH}) of 5 mV and 50 mV in positive and negative bias stress (PBS and NBS) tests. The vertically all-oxide TFTs demonstrate good control from side wall with on/off ratio over 10^5 and maximum current (I_{max}) over 160 μA/μm. And vertically all-oxide ferroelectric field-effect transistors (Fe-FETs) exhibit a memory window (MW) of 1.85 V, with an endurance and retention extended to 10^{12} cycles and 10 years. This illustrates the vertically all-oxide device based on ALD oxide semiconductor (OS) is a good candidate toward future high-density integrated circuits.

3:50 PM

T4.2 Scaling Potential of Nanosheet Oxide Semiconductor FETs for Monolithic 3D Integration - ALD Material Engineering, High-Field Transport, Statistical Variability, Kaito Hikake[1], Sung-hun Kim[1], Xingyu Huang[1], Kota Sakai[1], Zhuo Li[1], Tomoko Mizutani[1], Takuya Saraya[1], Toshiro Hiramoto[1], Takanori Takahashi[2], Mutsunori Uenuma[2], Yukiharu Uraoka[2], Masaharu Kobayashi[1,3] [1]Institute of Industrial Science, The University of Tokyo, [2]Nara Institute of Science and Technology, [3]d. lab, The University of Tokyo

We have investigated the scaling potential of nanosheet oxide semiconductor FETs (NS OS FETs) for 3D LSI application in terms of ALD material engineering, high-field transport, and statistical variability, for the first time. We have developed and systematically compared ALD-grown InGaO, InZnO and InGaZnO FETs. We have fabricated sub-100nm gate length NS OS FETs and demonstrated unsaturated carrier velocity behavior. We have obtained statistical variability data of NS OS FETs and showed a comparable variability against Si CMOS. This work provides an evidence of scalability of NS OS FETs for 3D LSI application.

4:15 PM

T4.3 Enhancement of In_2O_3 Field-Effect Mobility Up To 152 cm^2·V-1·s-1[1] Using HZO-Based Higher-k Linear Dielectric, Zehao Lin[1], Chang Niu[1], Hyeongjun Jang[2], Taehyun Kim[2], Yizhi Zhang[1], Haiyan Wang[1], Changwook Jeong[2], Peide Ye[1] [1]Purdue University, [2]Ulsan National Institute of Science and Technology

In this work, we report high-performance ALD In_2O_3 TFTs using HZO as a linear higher-k dielectric. By properly inserting a thin Al_2O_3 layer between two asymmetric HZO layers and annealing the HZO-Al_2O_3-HZO stack capped with In_2O_3, the k value of the linear dielectric is boosted to 30. This results in an EOT of

1.9 nm with physical thickness of 15.5 nm and meanwhile In_2O_3 field-effect mobility is boosted to 152 $cm^2 \cdot V^{-1} \cdot s^{-1}$, simultaneously. Such enhancements enable high-performance TFTs with record saturation current exceeding 2 mA/µm with a L_{ch} of 1 µm, and maximum current reaches 7 mA/µm with L_{ch} of 30 nm. Higher-k dielectrics also enhance the electrostatic control of the channel with negligible hysteresis, on/off ratio over 10^{11}, and DIBL less than 40 mV/V at L_{ch} of 35 nm. This work demonstrates a promising and straightforward methodology to enhance the mobility of oxide semiconductor channel by using linear higher-k dielectrics.

4:40 PM

T4.4 Highly Enhanced Memory Window of 17.8V in Ferroelectric FET with IGZO Channel via Introduction of Intermediate Oxygen-deficient Channel and Gate Interlayer, Sijung Yoo[1], Donghoon Kim[1], Duk-Hyun Choe[1], Hyun Jae Lee[1], Yunseong Lee[1], Sanghyun Jo[1], Yoonsang Park[1], Ki Hong Kim[1], Kyooho Jung[1], Moonil Jung[1], Kwang-Hee Lee[1], Jee-Eun Yang[1], Sangwook Kim[1], Seung-Geol Nam[1] [1]Samsung Advanced Institute of Technology

We demonstrated a novel Ferroelectric Field-Effect Transistor (FeFET) with an IGZO channel, featuring a record-high memory window (MW) of up to 17.8V. A significant advancement is achieved by two strategies. Firstly, the introduction of an intermediate oxygen-deficient channel, which offers sufficient depletion charge to ensure full-loop polarization switching. Secondly, inserting a thin gate interlayer (G.IL), which further increases the MW by the contribution of injected charge through G.IL. With a sub-12nm gate stack thickness and an operation voltage below 15V, the device exhibits promising potential for high-density, low-power non-volatile memory applications.

5:05 PM

T4.5 A-IGZO FETs with High Current and Remarkable Stability for Vertical Channel Transistor(VCT) DRAM Applications, Younjin Jang[1], Jee-Eun Yang[1], Na-Rae Han[1], Ha-Jun Sung[1], Jung-kyun Kim[1], Youngkwan Cha[1], Kwang-Hee Lee[1], Kyooho Jung[1], Moonil Jung[1], Wonsok Lee[2], Min Hee Cho[2], Sangwook Kim[1] [1]Samsung Advanced Institute of Technology, [2]Samsung Electronics

We report the a-IGZO channel FET exhibited high I_{on} (22 µA/µm with $V_{GS} = V_{th}$+1 V and V_{DS} = 1 V) and excellent NBTI characteristics (ΔV_{th} < 1 mV at 3 MV/cm, 85°C). In order to realize such a high performance device, there are several considerations, one of which is finding the optimal composition that increases mobility and keeps device reliability characteristics stable, and the next is to understand the effects of various process conditions on channel behavior and effectively suppress oxygen vacancies (V_O) while lowering hydrogen (H) concentration. Specifically, we tried to apply an interlayer to contact metal, reduced the H in the bottom oxide, and finally optimized the condition of a gate oxide (G_{ox}) process and O_2 treatment method that could efficiently minimize defect states in the device.

Session C7: Processors I

3:25 PM, Honolulu 1

Co-Chairs: Priyanka Raina, Stanford University
Chia-Hsiang Yang, National Taiwan University

3:25 PM

C7.1 Onyx: A 12nm 756 GOPS/W Coarse-Grained Reconfigurable Array for Accelerating Dense and Sparse Applications, Kalhan Koul[1], Maxwell Strange[1], Jackson Melchert[1], Alex Carsello[1], Yuchen Mei[1], Olivia Hsu[1], Taeyoung Kong[1], Po-Han Chen[1], Huifeng Ke[1], Keyi Zhang[1], Qiaoyi Liu[1], Gedeon Nyengele[1], Akhilesh Balasingam[1], Jayashree Adivarahan[1], Ritvik Sharma[1], Zhouhua Xie[1], Christopher Torng[2], Joel Emer[3], Fredrik Kjolstad[1], Mark Horowitz[1], Priyanka Raina[1] [1]Stanford University, [2]University of Southern California,[3]Massachusetts Institute of Technology

This work presents Onyx, the first coarse-grained reconfigurable array for both dense and sparse applications. We add composable sparse primitives that accelerate arbitrary sparse tensor algebra kernels with support for higher-order tensors, multiple inputs, and fusion. Onyx also has application-specialized compute and area-optimized memory tiles for image processing and machine learning applications. We achieve up to 565x better energy-delay product (EDP) for sparse kernels vs. CPUs with sparse libraries, and up to 76% and 85% lower EDP for image processing and ML, respectively, vs. state-of-the-art.

3:50 PM

C7.2 A 52.01TFLOPS/W Diffusion Model Processor with Inter-Time-Step Convolution-Attention-Redundancy Elimination and Bipolar Floating-Point Multiplication, Yubin Qin[1], Yang Wang[1], Xiaolong Yang[1], Zhiren Zhao[1], Shaojun Wei[1], Yang Hu[1], Shouyi Yin[1] [1]Tsinghua University

This paper proposes an energy-efficient diffusion model processor with three features: 1) a semantic-segment sparse convolution engine removes 88.5% of duplicated convolution layer (CL) computations. 2) a resemble trivial attention exponent inheritance design improves attention layer (AL) computation efficiency by 16.7×. 3) a bipolar floating-point multiplier saves 25.4% multiplication effort by avoiding ineffective mantissa multiplication for both CL and AL. It achieves a peak efficiency of 52.01TFLOPS/W and reduces energy by 23.14× and 3.94× compared to state-of-the-art CL and AL processors.

4:15 PM

C7.3 A Stochastic Analog SAT Solver in 65nm CMOS Achieving 6. .6µs Average Solution Time with 100% Solvability for Hard 3-SAT Problems, Qiaochu Zhang[1,2], Shiyu Su[1,3], Zerui Liu[1], Hsiang-Chun Cheng[1], Zhengyi Qiu[1,3], Mayank Palaria[1], Jiacheng Ye[1], Deming Meng[1], Buyun Chen[1], Sushmit Hossain[1], Wei Wu[1], Mike Shuo-Wei Chen[1] [1]University of Southern California, [2]University of Virginia, [3]University of Waterloo

This paper presents a stochastic analog SAT solver, featuring a fast open-loop architecture with continuous-time self-loopback pull-up switches, a discrete-time scrambling scheme, and a cost-efficient hybrid random code generator. The SAT prototype in 65nm achieves orders of magnitude improvement in speed and energy efficiency compared to prior ASIC SAT solvers.

4:40 PM

C7.4 Occamy: A 432-Core 28.1 DP-GFLOP/s/W 83% FPU Utilization Dual-Chiplet, Dual-HBM2E RISC-V-based Accelerator for Stencil and Sparse Linear Algebra Computations with 8-to-64-bit Floating-Point Support in 12nm FinFET, Gianna Paulin[1], Paul Scheffler[1], Thomas Benz[1], Matheus Cavalcante[2], Tim Fischer[1], Manuel Eggimann[1], Yichao Zhang[1], Nils Wistoff[1], Luca Bertaccini[1], Luca Colagrande[1], Gianmarco Ottavi[3], Frank Kagan Gürkaynak[1], Davide Rossi[3], Luca Benini[1,3] [1]ETH Zurich, Switzerland, [2]Stanford University, USA, [3]University of Bologna, Italy

We present Occamy, a 432-core RISC-V dual-chiplet 2.5D system for efficient sparse linear algebra and stencil computations on FP64 and narrow (32-, 16-, 8-bit) SIMD FP data. Occamy features 48 clusters of RISC-V cores with custom extensions, two 64-bit host cores, and a latency-tolerant multi-chiplet interconnect and memory system with 32 GiB of HBM2E. It achieves leading-edge utilization on stencils (83 %), sparse-dense (42 %), and sparse-sparse (49 %) matrix multiply.

Session C8: Oversampled Converters

3:25 PM, Honolulu 2

Co-Chairs: Stacy Ho, MediaTek
Tetsuya Iizuka, The University of Tokyo

3:25 PM

C8.1 A 97dB-PSRR 178.4dB-FOM_{DR} Calibration-Free VCOΔΣ ADC Using a PVT-Insensitive Frequency-Locked Differential Regulation Scheme for Multi-Channel ExG Acquisition, Sehwan Lee[1,2], Taeryoung Seol[1], Geunha Kim[1], Minyoung Song[1], Gain Kim[1], Jong-Hyeok Yoon[1], Arup K. George[1], Junghyup Lee[1]
[1]DGIST, [2]Samsung Electronics

This paper proposes a 97dB-PSRR, 178.4dB-FOM_{DR} calibration-free 16-channel VCO-ΔΣ ADC system using a PVT-insensitive frequency-locked differential regulation (FLDR) scheme suitable for wireless ExG Acquisition. Thanks to the FLDR, the SNDR degradation in all 16 channels is less than 1dB over 1.4-2V supply and 20-60°C temperature ranges. Implemented in a 0.18µm standard CMOS process, the proposed system consumes 172µW from a 1.4V supply and occupies 2.7mm^2 active area, while a single channel consumes 4.2µW and 0.12mm^2, respectively.

3:50 PM

C8.2 A 470µW, 102.6dB-DR, 20kHz BW calibration-free ΔΣ Modulator with SFDR in excess of 110dBc using an Intrinsically Linear 13-Level DAC, Matteo Dalla Longa[1,2], Francesco Conzatti[1], Omar Ismail[2], John Gabriel Kauffman[2], Maurits Ortmanns[2] [1]Infineon Technologies Austria AG, [2]Ulm University

This paper presents the first true multibit Discrete Time ΔΣ Modulator (DTΔΣM) to achieve a SFDR in excess of 110dBc without the need for Dynamic Element Matching (DEM) or calibration. The high linearity is obtained using a 13-level intrinsically linear DAC in the feedback loop. Over Process-Voltage-Temperature (PVT) variations, the SFDR is consistently between 105 and 115dBc for all measured devices. The prototype achieves a DR of 102.3dB and an SNDR of 100.7dB in a 20kHz BW, consuming 500µW from a 1.8V supply, resulting in a Schreier FoM of 178.3dB.

4:15 PM

C8.3 A Beyond-the-rail Audio CTDSM with a Passive Input Stage and 99.2dB SNDR, Shenyang Li[1], Sundeep Javvaji[1], Victor Pecanins-Martínez[1], Eren Aydin[1], Robert Van Veldhoven[2], Kofi Makinwa[1] [1]Delft University of Technology, [2]NXP Semiconductors

This paper presents a 3rd order continuous-time delta-sigma modulator (CTDSM) for audio applications. Its loop filter efficiently realizes complex conjugate NTF zeros by combining a passive RC filter and a Gm-C based resonator. The latter is built around a capacitively-coupled chopper OTA, which enables a beyond-the-rail input range. Implemented in 65nm CMOS, the proposed CTDSM achieves 99.2dB SNDR and 100dB DR in a 24kHz BW while consuming only 80.7µW. This results in a state-of-the-art Schreier FoMSNDR of 184dB.

4:40 PM

C8.4 A 0.38mW 200kHz-BW 92.1dB-DR Single-Opamp 4th-order Continuous-Time Delta-Sigma Modulator with 3rd-order Noise Coupling, Kent Edrian Lozada[1], Ye-Dam Kim[1], Ho-Jim Kim[2], Youngjae Cho[2], Michael Choi[2], Seung-Tak Ryu[1] [1]Korea Advanced Institute of Science and Technology, [2]Samsung Electronics

This work proposes a digital-intensive 4th-order continuous-time delta-sigma modulator (CTDSM) realizing 3rd-order noise-shaping through digital noise coupling (DNC), while the remaining 1st-order noise-shaping is done by an analog loop filter (LF). Fabricated in 28-nm CMOS, the proposed architecture achieves 89.0-dB SNDR, 92.1-dB DR, and 103.9-dB SFDR in a 200-kHz bandwidth (BW), while consuming only 0.38mW at 12.8MS/s. This results in a state-of-the-art Schreier Figure of Merit (FoM_S) of 179.3dB and Walden FoM_W of 41.2fJ/conv.-step.

5:05 PM

C8.5 A 10.8GS/s, 84MHz-BW RF Bandpass ΣΔ ADC with a 89dB-SFDR and a 62dB-SNDR for LTE/5G Receivers, Alhassan Sayed[1], Michel Vasilevski[1], Mahmoud Tarek Abdelmomen[1], Shadi Turk[1], Ahmed Ghoniem[2], Cristobal Perez[3], Cyril Voillequin[4], Haralampos Stratigopoulos[5], Marie-Minerve Louerat[5], Eric Wantiez[3], Hassan Aboushady[1] [1]Seamless Waves, [2]insspectrum, [3]Nokia, [4]Thales, [5]Sorbonne University, LIP6, CNRS
The LTE/5G multi-standard RF BP ΣΔ ADC reported in this paper achieves an SFDR of 89dB and an SNDR of 62dB on a 84MHz-BW centered at F0=2.7GHz. The ADC, sampled at Fs=10.8GHz, has an RF Noise Figure of 29dB, and an Input Intercept Point of +8dBm. When OFDM modulated signals are applied to the ADC, the measured EVM is 1.25% for a 10MHz/64-QAM/LTE, 1.6% for a 20MHz/64-QAM/LTE, and 2.0% for a 40MHz/64-QAM/5G signal.

Session C9: Wireless Transceivers

3:25 PM, Honolulu 3

Co-Chairs: Vanessa Chen, Carnegie Mellon University
Wei Deng, Tsinghua University

3:25 PM

C9.1 A 132-to-163 GHz 4TX/4RX Distributed MIMO FMCW Radar Transceiver with Real-time Reference-Clock Synchronization Enabling Cooperative Coherent Multistatic Imaging System, Ruichen Wan[1], Wei Deng[1], Qixiu Wu[1], Haikun Jia[1], Rui Wu[2], Angxiao Yan[1], Haowen Cai[3], Sanming Hu[3], Zhihua Wang[1], Baoyong Chi[1]
[1]Tsinghua University, [2]National Key Laboratory of Microwave Imaging Technology, Aerospace Information Research Institute, Chinese Academy of Science, [3]Southeast University
This work introduces a D-band 4TX/4RX distributed MIMO radar transceiver with real-time reference-clock synchronization for multistatic imaging system. The proposed synchronized radar system eliminates the time error, frequency error, and slope error of local oscillator (LO) signals between radar stations to ensure the correct acquisition and analysis of radar signals, which enables the combination of target data from multitude of transmitting and receiving stations coherently. In addition, several circuit design techniques including harmonic extraction series power synthesis and harmonic suppression frequency doubling are investigated. This work achieves better detection performance than the traditional MIMO radar with the same number of channels, demonstrating its advantages in future cooperative coherent multistatic imaging system.

3:50 PM

C9.2 A 640-Gb/s 4 X 4-MIMO D-Band CMOS Transceiver Chipset, Chenxin Liu[1], Zheng Li[1], Yudai Yamazaki[1], Hans Herdian[1], Chun Wang[1], Anyi Tian[1], Jun Sakamaki[1], Han Nie[1], Xi Fu[1], Sena Kato[1], Wenqian Wang[1], Hongye Huang[1], Shinsuke Hara[2], Akifumi Kasamatsu[2], Hiroyuki Sakai[1], Kazuaki Kunihiro[1], Atsushi Shirane[1], Kenichi Okada[1] [1]Tokyo Institute of Technology, [2]National Institute of Information and Communications Technology
This work presents a D-band (114-170GHz) CMOS transceiver (TRX) chipset covering a 56GHz signal-chain bandwidth. An 8-way low-Q power-combined power amplifier (PA), a 2-way low-Q power-combined low noise amplifier (LNA), wideband-impedance-transformation mixers, and common-source-based cascaded distributed amplifiers (DA) are proposed to improve bandwidth and linearity. The proposed TRX chipset achieves 200-Gb/s data rate by 32QAM in the single-input single-output (SISO) over-the-air (OTA) measurement. A 120-Gb/s data rate by 16QAM is realized with a 15m distance. A 640-Gb/s 4×4 multi-input multi-output (MIMO) is also demonstrated in this work.

4:15 PM

C9.3 A -96.5 dBm-Sensitivity, 14 dBm peak power, Self-Interference Resistant IR-UWB Radar Transceiver Supporting Child Presence Detection and Precision Positioning, Hyun-Gi Seok[1], Wan Kim[1], Sinyoung Kim[1], Jae-Keun Lee[1], Chanho Kim[1], Chanbin Ko[2], Junseong Park[2], Wonkang Kim[1], Jongpill Cho[1], Seungyoung Bae[1], Youngsea Cho[1], Wonjun Jung[1], Junhyeong Kim[1], Sumin Kang[1], Hyeokju Na[1], Byoungjoong Kang[1], Honggul Han[1], Hoon Kang[1], Minki Ahn[1], Chiyoung Ahn[1], Sukjin Jung[1], Hyukjun Sung[1], Seunghyun Oh[1], Jae-Eun Lee[2], Jongwoo Lee[1], Joonsuk Kim[1] [1]Samsung Electronics, [2]Bitsensing

This paper presents a radar-enabled IR-UWB system by adopting a self-interference resistant RF transceiver. It shows that child presence detection using IR-UWB radar is possible by implementing a radar system including PHY, MAC, and APP processor. RF transceiver shows high receiver sensitivity and transmitter peak power with low power. Furthermore, a radar dedicated transmitter is used to improve the transmitter signal isolation to the receiver. Proposed notch pulse shaping filter is adopted to satisfy the spectrum emission mask specification. Additionally, a low noise amplifier with wide gain ranges is proposed to improve the sensitivity and support various applications such as radar and positioning detection application. The UWB transceiver achieves -96.5 dBm sensitivity at BPRF 6.81 Mb/s and 14 dBm transmitter peak power and supports the UWB channel 5 and 9.

4:40 PM

C9.4 A 28GHz 5G NR Wirelessly Powered Relay Transceiver Using Rectifier-Type 4th-Order Sub-Harmonic Mixer, Sena Kato[1], Shu Date[1], Tao Ruoxin[1], Yasuto Narukiyo[1], Hiroki Hayashi[1], Keito Yuasa[1], Michihiro Ide[1], Takashi Tomura[1], Kenichi Okada[1], Atsushi Shirane[1] [1]Tokyo Institute of Technology

In this paper, a wirelessly powered 28GHz phased-array relay transceiver for 5G networks is proposed. The transceiver operates by rectifying a 5.7GHz WPT signal to generate DC power. The transceiver consists of a circuit that performs 4th-order sub-harmonic mixer operation while rectifying the WPT signal. The proposed circuit rectifies with efficiency of up to 54.9% and a maximum frequency conversion gain of -19.3dB. The 4×2-array antenna board implementing the chips can steer beam from -50° to +50° and the board is capable of sending and receiving 5G NR modulated signal with 400MHz bandwidth using 64QAM (MCS17).

5:05 PM

C9.5 A 28GHz 4-Stream Time-Division MIMO Phased-Array Receiver Utilizing Nyquist-Rate Fast Beam Switching for 5G and Beyond (Late News), Yi Zhang[1], Minzhe Tang[1], Jian Pang[1], Zheng Li[1], Dongfan Xu[1], Dingxin Xu[1], Yuncheng Zhang[1], Kazuaki Kunihiro[1], Hiroyuki Sakai[1], Atsushi Shirane[1], Kenichi Okada[1] [1]Tokyo Institute of Technology

This work proposes an area-efficient 28-GHz time-division MIMO beamformer supporting multi-beam MIMO (MB-MIMO) without additional hardware cost. RF signal paths can be reused for different MIMO streams by a time-division beam-switching operation, which is realized by oversampled fast-switching RF phase shifter and clock-based synchronization. A prototype fabricated in 65nm CMOS achieves 64-QAM 4x4 MIMO reception in OTA measurement using four 5G NR spatial data streams with 400MHz channel bandwidth.

Panel Session

Tuesday, June 18, 8:00 pm – 10:00 pm

Tapa 1-3

Organizers: Stacy Ho, Mediatek
Stanley SC Song, Google
Noriyuki Miura, Osaka Univ

Kazuyuki Tomida, Rapidus
C. Patrick Yue, HKUST

Will AI Bite the Industry That Feeds It?

Moderators: Masato Motomura, Tokyo Institute of Technology
Chris Mangelsdorf, Analog Devices (retired)

It's time to talk about the scary elephant in the room. The powerful new technology of AI is only possible because of the high-performance semiconductors that WE make. But is this new beast about to turn on us? Are our jobs at stake because of it, or will it usher in a new golden age of semiconductors with breakthrough innovations and countless new applications?

This Panel discussion will have two parts. Part 1 for discussion of moderated questions among panelists followed by Q&A with the audience and Part 2 for game-show competition between Chip heroes (panelists and audience) and gen-AI.

Don't miss this thought-provoking and entertaining panel discussion!

Panelists:

Serge Biesemans, IMEC
Chidi Chidambaram, Qualcomm
Chet Lenox, KLA
Euicheol Lim, SKHynix
Azalia Mirhoseini, Stanford Univ
Rangharajan Venkatesan, Nvidia
Hoi-Jun Yoo, KAIST

Wednesday, June 19, 2024
Session PL2: Plenary Session II
8:00 AM, Tapa 1-3

8:00 a.m. **Opening Remarks**
T. Tsunomura, Tokyo Electron Ltd.
M. Hamada, The University of Tokyo

P2.1 - 8:35 AM

Wireless and Future Hyperconnected World, Maryam Rofougaran, Movandi Corporation, CEO and Co-Founder

Wireless networks will become the backbone of our hyper-connected world by providing high-speed, low-latency data transmission. Through a fusion of terrestrial cellular networks, satellite communication, and local wireless area networks, this infrastructure will seamlessly support continuous connectivity for billions of devices and cater to essential needs such as emergency response, remote work, automation, and operational efficiency. The integration of sensing technologies enriches wireless networks with contextual awareness and environmental intelligence. With billions of sensors capturing real-time data, these networks empower AI-driven algorithms to optimize performance, anticipate user requirements, and overcome potential obstacles. Semiconductor breakthroughs are pivotal in realizing intelligent wireless connectivity. Advanced chip sets, featuring embedded AI accelerators, empower AI algorithms to process data locally and make informed decisions in near real-time. Energy-efficient semiconductor

designs also extend device battery life. This presentation will review key advances of wireless technology and present emerging technologies that will shape its evolution.

P2-2 9:15 AM

Photonics-Electronics Convergence Devices to Accelerate IOWN, Hidehiro Tsukano, NTT Corporation, Senior Vice President of Research and Development

IOWN (Innovative Optical Wireless Network) is an initiative to create a sustainable society that cannot be achieved with current network infrastructure. By taking advantage of optical technology for across-the-board network communications and computing, NTT is aiming to provide a new ICT platform that features high-capacity, high-quality, low-latency, and low-power consumption. The primary requirements for device technology are ultra-fine semiconductor manufacturing processes, ultra-high density assembly, and photonics-electronics convergence. Thus, NTT is promoting research and development in accordance with the roadmap to incorporate optical communications technology into the details of computing components step by step. This challenge could lead to the ultimate computing capacity that extends Moore's law, and we believe it can resolve the ever-increasing power consumption problem of information processing and contribute to the realization of carbon neutrality.

Session T5: Advanced CMOS Devices and Technology-1

10:15 AM, Tapa 1-3

Co-Chairs: Anabela Veloso, Imec
Jin Cai, TSMC

10:15 AM

T5.1 Product Performance Aware 3rd Generation GAA Platform Transistor Design with Extreme Small Local Layout Effect and Transistor Variation, Dongchan Jeong[1], Seungkwon Kim[1], Seulki Park[1], Sang Hyeon Lee[1], Sada-aki Masuoka[1], Byungha Choi[1], Shincheol Min[1], Sanghoon Lee[1], Minseong Lee[1], Chang-Woo Sohn[1], Jaehun Jeong[1], Yuri Yasuda-Masuoka[1], Ja-Hum Ku[1,1] [1]Samsung Electronics

A product performance aware 3rd generation MBCFET[TM] (SF2) is revealed to maximize Gate-All-Around benefit fully by introducing unique epitaxial and integration process, which overcomes the scaling and GAA structure conflict with a product gain. The product major narrow NS Tr was boosted by N/PFET +29/+46%, as well as a wide NS Tr +11/+23%. In addition, through Tr global variation reduction by 26% from FinFET, a product leakage distribution was significantly scaled by ~50%. The process can enable another level of DTCO collaboration in MBCFET[TM] for the future technology.

10:40 AM

T5.2 Monolithic Complementary Field Effect Transistors (CFET) demonstrated using Middle Dielectric Isolation and Stacked Contacts, Steven Demuynck[1], Victor Vega Gonzalez[1], Camila Toledo de Carvalho Cavalcante[1], Lucas Petersen Barbosa Lima[1], Karen Stiers[1], Cassie Sheng[1], Anne Vandooren[1], Maryam Hosseini[1], Daisy Zhou[1], Hans Mertens[1], Thomas Chiarella[1], Juergen Boemmels[1], Roger Loo[1], Erik Rosseel[1], Clement Porret[1], Yosuke Shimura[1], Anjani Akula[1], Geert Mannaert[1], Subhobroto Choudhury[1], Vincent Brissonneau[1], Emmanuel Dupuy[1], Tanushree Sarkar[1], Nathali Franchina Vergel[1], Antony Peter[1], Nicolas Jourdan[1], Jean-Philippe Soulie[1], Kevin Vandersmissen[1], Farid Sebaai[1], Pallavi Putarame Gowda[1], Kenneth Lai[1], Andrea Mingardi[1], Sujan Sumar Sarkar[1], Koen Dhave[1], BT Chan[1], Alfonso Sepulveda Marquez[1], Robert Langer[1], Il Gyo Koo[1], Efrain Altamirano Sanchez[1], Katia Devriendt[1], Paulina Rincon Delgadillo[1], Frederic Lazzarino[1], Jerome Mitard[1], Jef Geypen[1], Eva Grieten[1], Dmitry Batuk[1], Yi-Fan Chen[1], Frederik Verbeek[1], Frank Holsteyns[1], Sujith Subramanian[1], Naoto Horiguchi[1], Serge Biesemans[1] [1]imec

This work reports on the first demonstration of monolithic CFET CMOS co-integrating Middle Dielectric Isolation (MDI), Inner Spacers (ISP) and Stacked frontside patterned Contacts. The flow results in functional CMOS devices on a common gate architecture. The MDI formation is done before source drain (SD) recess for optimal bottom junction (BJ) formation. The paper discusses the challenges of using stacked contacts to form the top device junction (TJ). Finite accuracy of bottom device contact (BC) registration from frontside results in a limited process latitude to access the top device channel for TJ formation while keeping the integrity of MDI and ISP. Top device survival rate increases from 11% to 79% by eliminating the frontside BC. We show feasibility of moving BC to the wafer backside with registration accuracy below 3nm.

11:05 AM

T5.3 Ge(110) GAA Nanosheet / Si(100) Tri-gate Nanosheet Monolithic CFETs Featuring Record-high Hole Mobility, Seong Kwang Kim[1,2], Hyeong-Rak Lim[1], Jaeyong Jeong[1], Youngkeun Park[1], Jejune Park[2], Sungil Park[2], Jaehyun Park[2], Daewon Ha[2], Byung Jin Cho[1], Sanghyeon Kim[1] [1]KAIST, [2]Samsung Electronics

In this study, we demonstrated heterogeneous 3D monolithic CFETs (mCFETs) by utilizing Ge (110)/<110> gate-all-around (GAA) nanosheet p-FETs as the top-tier transistors and Si (100)/<110> tri-gate n-FETs as the bottom-tier transistors. By minimizing the mobility difference between electrons and holes through this transport combination of heterogeneous channels, we demonstrated its potential for the next-generation logic. Notably, we achieved a record-high hole mobility of 1200 $cm^2/V{\cdot}s$ (normalized by footprint to account CFET drivability) in the Ge (110)/<110> GAA nanosheet p-FETs with flat top and bottom surfaces. These channels were successfully employed in heterogeneous mCFETs to see the feasibility for high-performance logic devices.

11:30 AM

T5.4 Thermal Considerations for Block-Level PPA Assessment in Angstrom Era: A Comparison Study of Nanosheet FETs (A10) & Complementary FETs (A5), Subrat Mishra[1], Bjorn Vermeersch[1], Venkateswarlu Sankatali[1], Halil Kukner[1], Gioele Mirabelli[1], Fabian Bufler[1], Moritz Brunion[1], Dawit Burusie Abdi[1], Herman Oprins[1], Dwaipayan Biswas[1], Odysseas Zografos[1], Francky Catthoor[1], Pieter Weckx[1], Geert Hellings[1], James Myers[1], Julien Ryckaert[1] [1]IMEC

In this paper, we make a thermal-aware block-level PPA comparison study for nanosheet transistors and complementary field effect transistors, expected to be used in future Angstrom nodes, namely A10 and A5 respectively. We report block-level scaling results from A10 to A5 node on an open-source many-core architecture: 2.5% increase in F_{max}, 25% reduction in power, 27% reduction in energy per cycle, achieved with 35% area reduction and a consequent increase in power density by 15% under nominal 0.7V/25C. The PPA analysis methodology has been augmented with a fast package-level thermal simulator to enable early self-consistent thermal estimation that accounts for exponential leakage power increase with temperature, which is important for dynamic thermal management applications. The analysis reveals a reduction of 64mV in Vdd and 10% in frequency required for A5 node to maintain same $T_{j,max}$ as A10 node operating at 0.7V, still resulting in a 40% gain in system throughput.

Session C10: Transformer Processors

10:15 AM, Honolulu 1

Co-Chairs: Ben Keller, NVIDIA
Youngjoo Lee, POSTECH

10:15 AM

C10.1 MINOTAUR: An Edge Transformer Inference and Training Accelerator with 12 MBytes On-Chip Resistive RAM and Fine-Grained Spatiotemporal Power Gating, Kartik Prabhu[1], Robert M. Radway[1],

Jeffrey Yu[1], Kai Bartolone[1], Massimo Giordano[1], Fabian Peddinghaus[1], Yonatan Urman[1], Win-San Khwa[2], Yu-Der Chih[2], Meng-Fan Chang[2], Subhasish Mitra[1], Priyanka Raina[1] [1]Stanford University, [2]TSMC
MINOTAUR is the first energy-efficient edge SoC for inference and training of Transformers (and other networks, e.g., CNNs) with all memory on-chip. MINOTAUR leverages a configurable 8-bit posit-based accelerator, fine-grained spatiotemporal power gating enabled by on-chip resistive-RAM (RRAM) for dynamically adjustable bandwidth, and on-chip fine-tuning through full-network low-rank adaptation (LoRA). MINOTAUR achieves an average utilization of 93% and 74% and energy of 8.1 mJ and 7.3 mJ on ResNet-18 and MobileBERT$_{TINY}$ inference respectively, and on-chip fine-tuning within 1.7% of off-line training without RRAM-induced energy limitations or endurance degradations.

10:40 AM

C10.2 A 28nm 4.35TOPS/mm2 Transformer Accelerator with Basis-vector Based Ultra Storage Compression, Decomposed Computation and Unified LUT-assisted Cores, Chen Tang[1], Xinyuan Lin[1], Zongle Huang[1], Wenyu Sun[1], Hongyang Jia[1], Yongpan Liu[1,1] [1]Tsinghua University

The area-efficient Transformer accelerator exploiting matrix redundancy is presented with four features: 1) A proposed basis-vector decomposition sparing 25.5x model storage for Transformer like Bert-Base, allowing full on-chip inference on devices with about 13MB memory like smartphones, at only 1.28% accuracy loss. 2) An area-efficient self-programming LUT-assisted computing cell by result prefetch; 3) A unified task-insensitive core supporting fast decomposed computing, resulting in a remarkable 73% energy saving; 4) A NoC design facilitating hybrid data reuse to reduce communication. It achieves 4.35 TOPS/mm^2 dense area efficiency, 4 times than the state-of-the-art counterpart at same fabrication level. It also demonstrates 213%-429% higher overall energy efficiency.

11:05 AM

C10.3 A 99.2TOPS/W Transformer Learning Processor with Approximated Attention Score Gradient Computation and Ternary Vector-based Speculation, Ping-Sheng Wu[1], Yu-Cheng Lin[1], Chia-Hsiang Yang[1]
[1]Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan

This work presents the *first* Transformer learning processor supporting both inference and training acceleration. By applying algorithm-architecture optimizations, including approximated gradient computation and ternary vector-based speculation, the training complexity is reduced by up to 94.2%. Adoption of the 8-bit block floating-point (Block-FP) format enables a 39-to-60% power reduction for multiply-accumulate (MAC) operations. The chip delivers a peak energy efficiency of 99.2TOPS/W, outperforming the state-of-the-art Transformer inference-only processors by 2.6-to-162×.

11:30 AM

C10.4 A 22nm 54.94TFLOPS/W Transformer Fine-Tuning Processor with Exponent-Stationary Re-computing, Aggressive Linear Fitting, and Logarithmic Domain Multiplicating, yang wang[1], Xiaolong Yang[1], Yubin Qin[1], Zhiren Zhao[1], ruiqi guo[1], zhiheng yue[1], Huiming Han[1], Shaojun Wei[1], Yang Hu[1], Shouyi Yin[1,2] [1]Tsinghua University, [2]Shanghai AI Laboratory

This paper proposes a Transformer-based processor supporting energy-efficient fine-tuning with batch-iteration-matrix multi-level optimizations. It has three key features: 1) An exponent-stationary re-computing scheduler (ESRC) reduces 44.2% of the storage requirement for each batch. 2) An aggressive linear fitting unit (ALFU) saves 47.4% of the computations in each iteration. 3) A logarithmic domain processing element (LDPE) decreases 36.3% of energy for matrix multiplications (MM) in fine-tuning. The proposed Transformer processor achieves an energy efficiency of 54.94TFLOPS/W. It reduces fine-tuning energy by 4.27× and offers 3.57× speedup for GPT-2.

Session C11: Clocking Techniques

10:15 AM, Honolulu 2

Co-Chairs: Erik Olieman, NXP Semiconductors
Satoshi Kondo, Toshiba Corp.

10:15 AM

C11.1 A 0.9V Rail-to-Rail Ultra-Low-Power Fully Integrated Clock Generator Achieving 23fJ/Cycle in 28nm CMOS, Sander Derksen[1], Maël Demarets[2,3], Gerard Villar Piqué[1], Fabio Sebastiano[3] [1]NXP Semiconductors, [2]KU Leuven, [3]Delft University of Technology

The proposed VCO comprises two voltage-stacked coupled ring oscillators, one tied to vdd and one tied to gnd, each driving part of a level-shifter circuit to prevent short-circuit currents, thus generating a rail-to-rail clock with high energy efficiency. As a potential application, the VCO is embedded in a duty-cycled RC-based FLL. In 28nm CMOS, the VCO and the FLL draw 7.4nA and 26nA from the nominal 0.9V supply, respectively, while delivering a 1MHz rail-to-rail output clock.

10:40 AM

C11.2 A 94fs$_{rms}$-Jitter and –249.3dB FoM 4.0GHz Ring-Oscillator-based MDLL with Background Calibration of Phase Offset and Injection Slope Mismatch, Dongjun Park, Heesung Roh, Seon-Kyoo Lee, and Jae-Yoon Sim, POSTECH

This paper presents a ring oscillator (RO)-based multiplying delay-locked loop (MDLL) with frequency and slope detector (FSD) that can control both the oscillation frequency and the injection signal slope. By comparing characteristics of two consecutive transitions of the RO before and after the injection, the FSD distinguishes the cause of error, i.e., mismatch in period or slope. Hence, it can individually drive two loops; 1) for locking the steady-state frequency of the RO and 2) for matching the transition slope of the reference edge to that of the internal node of the RO. As the proposed FSD efficiently mitigates each jitter source, the chip, implemented in 40nm CMOS, shows an integrated rms jitter of 94fsrms at 4GHz, achieving a FoM of -249.3dB.

11:05 AM

C11.3 A 25.4-27.5 GHz Ping-Pong Charge-Sharing Locking PLL Achieving 42 fs Jitter with Implicit Reference Frequency Doubling, Sayan Kumar[1], Patchara Sawakewang[1], Teerachot Siriburanon[1], Robert Bogdan Staszewski[1] [1]University College Dublin

We propose a ping-pong charge-sharing locking (PP-CSL) PLL which injects charge into the oscillator tank employing complemen- tary charge-sharing capacitors (C_{shared}) during both positive and negative reference clock (f_{REF}) transitions, resulting in an implicit 2x multiplication. The proposed frequency-tracking loop (FTL) and duty-cycle calibrations (DCC) are achieved simultaneously by monitoring the charge residue on Cshared. Implemented in 28 nm CMOS, the ∼27 GHz PLL achieves 42 fs of rms jitter while consuming only 14 mW with f_{REF} of 250 MHz, leading to $FoM_{jitter-N}$ of -276.6 dB.

11:30 AM

C11.4 A 3.2GHz-15GHz Low Jitter Resonant Clock Featuring Rotary Traveling Wave Oscillators in Intel 4 CMOS for 3D Heterogeneous Multi-Die Systems, Vinayak Honkote[1], Ragh Kuttappa[1], Jainaveen Sundaram[1], Satish Yada[1], Chinnusamy Kalimuthu[1], Juhi Patil[1], Richard Lee[1], Cristan Paulino[1], Paolo Aseron[1], Trang Nguyen[1], Amreesh Rao[1], Dileep Kurian[1], Mingming Xu[1], Yan Song[1], Tanay Karnik[1], Anuradha Srinivasan[1], Vivek De[1] [1]Intel Corporation.

We present a resonant clocking technique featuring rotary traveling wave oscillators (RTWOs) and a rotary oscillatory array (ROA) in Intel 4 CMOS for high-frequency, low-jitter, low-power and low-skew clock generation and distribution in 3D heterogeneous multi-die systems. The active base die incorporates an

array of four coupled RTWOs capable of dynamic frequency tuning. Three independent resonant rotary rings are implemented to demonstrate the range of native resonant frequencies with very low jitter. The circuits operate across a wide frequency (3.2GHz-15GHz) and voltage (0.55V-1.2V) range with very low measured period jitter (107fs-705fs) and minimal duty-cycle distortion (50±0.8%) suitable for multi-die high-performance GPUs.

Session C12: Sensors for Audio and Video
10:15 AM, Honolulu 3

Co-Chairs: Markus Dielacher, Infineon
Kentaro Yoshioka, Keio University

10:15 AM

C12.1 23,000-Exposures/s 360fps-Readout Software-Defined Image Sensor with Motion-Adaptive Spatially Varying Imaging Speed, Roberto Rangel[1], Xiaonong Sun[1], Ayandev Barman[1], Rahul Gulve[1], Savo Bajic[1], Jingmin Wang[1], Harry Wang[1], David B. Lindell[1], Kiriakos N. Kutulakos[1], Roman Genov[1] [1]University of Toronto

The software-defined VGA image sensor adapts to fast changes in the scene, both locally and globally, by taking advantage of programmable-size/speed super-pixels and scalable-rate SAR ADCs, respectively. Each super-pixel includes up to 8x8 pixels exposed in a rapid sequence within one frame period, yielding a 64x maximum boost of the exposure rate over the output rate, without the corresponding increase in the ADC power. At 360fps readout, this corresponds to over 23,000 exposures/s while using only 24.5mW, and comes at the cost of moderately lower *local* resolution, only in the regions with the fast changes in the scene. The 54fJ-FoM SAR ADC allows for scaling down to the 30fps 'slow' mode, yielding an additional factor of 12x savings in the output data and camera digital power, and 30% savings in the ADC power.

10:40 AM

C12.2 A 450µW@50fps Wake-Up Module Featuring Auto-Bracketed 3-Scale Log-Corrected Pattern Recognition and Motion Detection in a 1.5Mpix 8T Global Shutter Imager, Arnaud Verdant[1], William Guicquero[1], David Coriat[1], Guillaume Moritz[1], Nicolas Royer[1], Sébastien Thuries[1], Anaïs Mollard[2], Vincent Teil[2], Yann Desprez[2], Gilles Monnot[2], Pierre Malinge[2], Bruno Paille[2], Guillaume Caubit[2], Arnaud Bourge[2], Laurent Tardif[2], Stéphanie Bigault[2], Jérôme Chossat[2] [1]CEA Leti, [2]STMicroelectronics

Megapixel imagers with computer vision capabilities exhibit high acquisition performance at the expense of a power consumption preventing always-on usage. This paper presents ATIM, a wake-up solution for both 3-scale pattern recognition and motion detection, that is added to a 1360×1120 Global-Shutter commercial CIS without impairing image quality in standard readout modes. ATIM relies on self-adaptation to ambient light conditions, to improve algorithmic robustness for real-world scenarios. This module captures 9×9-downsampled 8b images using a dedicated readout and processes 6b 152×112 frames, under an overall power budget of ~450µW at 50fps.

11:05 AM

C12.3 A 430-µA 68.2-dB-SNR 133-dBSPL-AOP CMOS-MEMS Digital Microphone based on Electrostatic Force Feedback Control, Qi Zhang[1], Jiaqi Dong[1,2], Xinwen Zhang[1], Yekan Chen[1,2,3], Zipeng Cheng[1], Bo Zhao[1], Yuxuan Luo[1,2,4] [1]Zhejiang University, [2]ZJU-Hangzhou Global Scientific and Technological Innovation Center, [3]Microaiot, [4]Stomatology Hospital, School of Medicine, Zhejiang University

This paper presents a high-dynamic-range CMOS-MEMS digital microphone based on electrostatic force feedback control (EFFC). We propose to adjust the sensitivity of the capacitive acoustic transducer according to the input acoustic volume by adaptively biasing it at different voltages, so its acoustic dynamic range (DR) can be extended. A sub-sampling amplitude detector (SSAD) is proposed to achieve

fast and efficient acoustic volume detection. The volume detection result controls a fast-settling predictive referenced charge pump (PRCP) to provide closed-loop EFFC. The proposed solution achieves a signal-to-noise ratio (SNR) of 68.2 dB at 94 dBSPL and an acoustic overload point (AOP) of 133 dBSPL with 430 µA at CLK_{IN}= 3.072 MHz. The measured acoustic DR is 107.2 dB.

11:30 AM

C12.4 A 1.5 V 132 dBSPL AOP Digital Readout Circuit for MEMS Microphone Using Self-Adaption Loop, Ling Wang[1], Longjie Zhong[1], Zhangming Zhu[1] [1]Key Laboratory of Analog Integrated Circuits and Systems (Ministry of Education), School of Integrated Circuits, Xidian University

This work presents a digital readout integrate circuit (IC) for capacitive MEMS microphone, which features a self-adaption loop (SAL), allowing the single-ended system to process high sound pressure signals. A prototype is realized in a 0.153 µm CMOS process, performing 67.34 dB-A SNR at 94 dB SoundPressure-Level (SPL) with an acoustic overload point (AOP) of 132 dB SPL, consuming 738 µA at 1.5 V supply voltage.

Session TFS1: Oxide Semiconductor Applications in BEOL

1:00 PM, Tapa 1

Co-Chairs: Franck Arnaud, STMicroectronics
Tuo-Hung Hou, National Yang Ming Chiao Tung University

1:00 PM

TFS1.1 Amorphous Oxide Semiconductors for Monolithic 3D Integrated Circuits (Invited), Suman Datta[1], Shimeng Yu[1], Asif Khan[1], Sunbin Deng[1], Khandker Akif Aabrar[1], Jungyoun Kwak[1] [1]Georgia Tech

AOS FETs, with low leakage current, satisfactory carrier mobility and BEOL compatibility can enable dense memory on top of CMOS. Redesigned AOS FETs with high breakdown voltage can support efficient power delivery solutions. Such versatility positions AOS FETs to meet the evolving demands of heterogeneous compute, reshaping the technology landscape of memory and power delivery.

1:25 PM

TFS1.2 P-type SnO Semiconductor Transistor and Application (Invited), Chun-Chen Wang[1,2], Cheng-Chen Kuo[1], Cheng-Hsien Wu[1], Anni Lu[1,3], Heng-Yuan Lee[1], Chen-Feng Hsu[1], Pei-Jer Tzeng[1], Tung-Ying Lee[1], Fa-Rong Hou[4], Ming-Han Chang[5], Sheng-Chih Lai[1], Ken-Ichi Goto[1], Shimeng Yu[3], Chih-I Wu[2,4,5], C.T. Lin[1], Yu-Ming Lin[1], Xin-Yu Bao[1] [1]Taiwan Semiconductor Manufacturing Company, Ltd., [2]Graduate School of Advanced Technology, National Taiwan University, [3]Georgia Institute of Technology, [4]Graduate Institute of Electronics Engineering, National Taiwan University, [5]Graduate Institute of Photonics and Optoelectronics, National Taiwan University

In this work, high-quality p-type SnO material is developed by PVD deposition. Sub-100 nm short channel p-SnO devices are first demonstrated with current density 10~20 µA/µm, I_{on}/I_{off} over 10^4, SS ~0.4 V/dec and hole mobility ~2 cm^2/Vs. The benefits of monolithic 3D integration with oxide transistors in BEOL are projected using FPGA as example.

1:50 PM

TFS1.3 Demonstration of On-Chip Switched-Capacitor DC-DC Converters using BEOL Compatible Oxide Power Transistors and Superlattice MIM Capacitors, Sunbin Deng[1], Jungyoun Kwak[1], Junmo Lee[1], Dyutimoy Chakraborty[1], Jaewon Shin[1], Omkar Phadke[1], Sharadindu Gopal Kirtania[1], Chengyang Zhang[1], Khandker Akif Aabrar[1], Shimeng Yu[1], Suman Datta[1] [1]Georgia Institute of Technology

Through monolithic integration of back-end-of-line (BEOL) compatible enhancement and depletion-mode tungsten-doped indium oxide (IWO) power transistors and high-voltage (HV) superlattice capacitors, we

experimentally demonstrate, for the first time, an on-chip switched-capacitor (SC) DC-DC converter to support efficient power delivery in heterogeneous integrated circuits. A novel oxygen anneal treatment to the power transistors markedly improved the reliability of the transistors with a >4× reduction in V_{th} shift. The fabricated converter circuit achieved 12V-to-6V conversion with an efficiency of 82.8%. A projected power density of 1.03 W/mm^2 could be achieved by transitioning to 3D trench capacitors from current planar form.

2:15 PM

TFS1.4 First Experimental Demonstration of Hybrid Gain Cell Memory with Si PMOS and ITO FET for High-speed On-chip Memory, Shuhan Liu[1], Shengjun Qin[1], Koustav Jana[1], Jian Chen[1], Kasidit Toprasertpong[1], H.-S. Philip Wong[1] [1]Stanford University

This work experimentally demonstrates hybrid gain cell memory with Si PMOS as read transistor and ITO FET as write transistor integrated monolithically on the same chip. With Si PMOS as the read transistor, hybrid gain cell memory has the benefits of high read speed, counterbalanced capacitive coupling, optimized state allocation, and superb bias stress stability. Fabricated Si PMOS has mobility of 86.4 cm^2/Vs and the ALD ITO FET has positive V_{TH} = 0.75 V and excellent SS = 65 mV/dec. Hybrid gain cell shows measured retention of 5,000 sec under 0V WWL standby voltage. Excellent stability of < 12 mV shift for Si PMOS and ITO FET under 1,000 sec bias stress in standby mode is achieved.

2:40 PM

TFS1.5 On the Reliability of High-Performance Dual Gate (DG) W-doped In_2O_3 FET, Khandker Akif Aabrar[1], Hyeonwoo Park[1], Suman Datta[1], Sharadindu Kirtania Gopal[1], Sunbin Deng[1], Chengyang Zhang[1], Md Abdullah Al Mamun[2], Kyeongjae Cho[2], Gilbert B. Rayner Jr[3] [1]Georgia Institute of Technology, [2]University of Texas at Dallas, [3]Kurt J Lesker

We demonstrate a high performance back-end-of-line (BEOL) compatible tungsten (W)-doped In_2O_3 channel (IWO) dual gate (DG) field-effect transistor (FET) with ultra low-leakage current <10^{-15} A/µm and high I_{ON}/I_{OFF} ratio of 5.8x10^{11} at 2.5V overdrive (V_{ov}). In addition, the IWO DG FET demonstrates a record low negative bias temperature instability (NBTI) of 7.2mV, record low hot carrier degradation (HCD) of 63mV and a low positive bias temperature instability (PBTI) of 85mV at 1V V_{ov} which makes IWO DG FET a potential candidate for realizing high density embedded-DRAM for last-level cache (LLC). Furthermore, we develop a comprehensive modeling framework for assesing the reliability of amorphous oxide semiconductor (AOS) channel FETs which can provide insights into the threshold voltage (V_T) instability mechanisms and help design appropriate mitigation strategies.

Session T6: Memory Technology: NAND, DRAM-1

1:00 PM, Tapa 2

Co-Chairs: Jixin Yu, Western Digital Corp
Yuri Masuoka, Samsung Electronics

1:00 PM

T6.1 Fluorine-free Word Line Molybdenum Process for Enhancing Scalability and Reliability in 3D Flash Memory, Takashi Fukushima[1], Takayuki Kashima[1], Satoshi Seto[1], Hiroyuki Ohtori[1], Masaki Kato[1], Kaihei Katou[1], Hiroshi Takehira[1], Yohei Sugawara[1], Zhiyao Zhu[1], Kazushi Hara[1], Ryota Osanai[1], Takayuki Beppu[1], Hiroko Tahara[1], Tatsuya Ishiku[1], Kensei Takahashi[1], Tomotaka Ariga[1], Yu Ueda[2], Yuya Matamura[2], Yusuke Mukae[2], Naoki Takeguchi[2], Yosuke Maruyama[1], Ryo Nishikawa[1], Hakuba Kitagawa[1], Jun Asakawa[1], Yasuhiro Uchiyama[1], Kazuya Ohuchi[1], Katsuyuki Sekine[1] [1]Kioxia Corporation, [2]Western Digital Corporation

A state-of-the-art fluorine-free word line (WL) molybdenum (Mo) process has been established for future 3D flash memory. Application of Mo to WLs can accelerate scaling of cells in both the vertical and horizontal directions with lower RC delay and lower leakage failure rates compared to traditional tungsten. In addition to being fluorine-free, key attributes of the process are optimization of Mo recess by innovative chemical and improvement of Mo filling to remove oxygen residue in Mo voids. These techniques can extend the scaling limit of 3D flash memory.

1:25 PM

T6.2 Innovative Barrier Metal-less Metal Gate Scheme leading to Highly Reliable Cell Characteristics for 8th Generation 512Gb 3D NAND Flash Memory, Hang-Ah Park[1], Sejun Park[1], Min-Tai Yu[1], Ye-Chan Kim[1], Cheon Ho Park[1], Jung Hoon Lee[1], Jun Eon Jin[1], Dawoon Jeung[1], Hauk Han[1], Tai-Soo Lim[1], Min-Kyu Jeong[1], Mincheol Park[1], Bong-Tae Park[1], Sung Hoi Hur[1] [1]Samsung Electronics Co., Ltd.

We have successfully developed an innovative barrier metal (BM)-less metal gate scheme with high cell reliability for the 8th generation 3D NAND flash memory. This scheme allows the memory cells to significantly lower the wordline resistance by 30%, enabling a dramatic scale-down in the lateral dimension of a multi-pillar block architecture in 3D NAND. In addition, both cell interference and vertical charge loss can be enhanced by increasing fluorine (F) passivation at the trap sites in the blocking oxide (BOX). Ingenious technologies are developed to suppress degradations originating from the work function change and increased F concentration in tungsten (W) gates. Finally, enhanced cell reliabilities, inclusive of high cycle endurance and long term retention, can be acquired for the 8th generation 512Gb 3D NAND product. Our BM-less metal gate structure provides a novel approach to designing highly competitive future-generation 3D NAND flash memory.

1:50 PM

T6.3 Mechanical Stress Effects on Dielectric Leakage and Interconnection Integrity in 3D NAND Flash Memory, Se Hoon Lee[1] [1]Samsung Electronics Co., Ltd.

This paper presents a comprehensive study of stress-induced leakage in dielectrics, combining structural analysis with electrical transport properties in the latest 3D NAND Flash memory products. Stress-induced leakage is prominently observed near wide aluminum metal patterns, as changes in stress and strain significantly influence the dielectric properties. Through electrical analysis and DFT simulations, we successfully analyzed electrical transport phenomenon, which is explained by Schottky emission with decreased electrical barrier height in amorphous SiO_2 under tensile stress. We also proposed process improvements, including adjustments in annealing temperature and air-gap to mitigate leakage issues.

2:15 PM

T6.4 Up to 57% Reduction in Effective Resistivity of Word Lines of 3D-NAND Memory by Grain-size Control, Material Selection, and Seam Removal, Hiroshi Terada[1], Katsumasa Yamaguchi[2], Tsubasa Yokoi[2], Takashi Sameshima[2], Keisuke Suzuki[2], Genji Nakamura[1], Hiroyuki Nagai[1] [1]Tokyo Electron Ltd., [2]Tokyo Electron Technology Solutions Ltd.

In this work, we systematically studied the effective resistivity of word lines (WLs) of 3D NAND memory. We fabricated narrow and high-aspect-ratio wires in the similar way to the WL forming process of replacement-gate NAND and measured the resistivity of the wires. By using TiAlN liner, we increased grain size of W and achieved resistivity reduction. In addition, we found that the resistivities of the wires are equal to that of the blanket with half thickness, which indicates that the influence of electron scattering at a seam cannot be ignored in WL resistance. We demonstrated the resistivity reduction by closing seams with post-metal anneal and achieved 57% reduction in resistivity at liner-less and seam-less Mo compared to conventional W/TiN.

2:40 PM

T6.5 A Metal Dual Work-function Gate (MDWG) for the continuous scaling of DRAM Cell Transistors, Junsoo Kim[1] [1]Samsung Electronics

For the continuous scale-down of DRAM cell transistors, we have demonstrated, for the first time, a metal dual work function gate (MDWG) by replacing n+ Poly Si with an Oxide/La/TiN structure in a fully integrated DRAM.

Session TFS2: Backside of Silicon: From Power Delivery to Signaling

1:00 PM, Tapa 3

Co-Chairs: Seung-Chul Song, Google
Aaron Thean, National University of Singapore

1:00 PM

TFS2.1 Expanding Design Technology Co-Optimization Potentials with Back-Side Interconnect Innovation (Invited), Byung-Sung Kim[1], Subin Choi[1], Jung Han Lee[1], Kwangmuk Lee[1], Jisoo Park[1], Jiwook Kwon[1], Saehan Park[1], Kwanyoung Chun[1], Harsono Simka[1], Aravindh Kumar[1], Muhammed Ahosan Ul Karim[1], Ken Rim[1], Jaihyuk Song[1] [1]Samsung Electronics

This report analyzes the benefits obtained through Back-Side Interconnect (BSI) technology, encompassing Back-Side Power Delivery Network (BSPDN) and Back-Side Signal (BSS), from the perspective of Design-Technology Co-Optimization (DTCO). Through BSPDN, benefits such as metal pitch relaxation and/or cell height reduction can be achieved. Additionally, the implementation of BSS technology allows for intra-cell and inter-cell routing on the back side, leading to improved speed and greater reduction in cell area.

1:25 PM

TFS2.2 A Design Methodology for Back-side Power and Clock Routing Co-Optimization (Invited), Pruek Vanna-iampikul[1], Hang Yang[1], Jungyoun Kwak[1], Joyce X Hu[1], Amaan Rahman[1], Nesara Eranna Bethur[1], Cong Hao[1], Shimeng Yu[1], Sung Kyu Lim[1] [1]Georgia Institute of Technology

This paper presents a backside (BS) design methodology for optimizing both power delivery network (PDN) and clock routing in 3nm. A unit converter (UC) has been integrated on the backside with BS-PDN to minimize dynamic IR-drop. Additionally, our backside buffer cell with backside contact enables backside clock routing. Experimental results show that BS-PDN mitigates 57.7% IR-drop compared to FS-PDN, and UC integration further reduces IR-drop by 10.3% and package IR-drop by 83.9%. Our backside clock routing improves clock power by 32% and full-chip power-delay product by 13.6%.

1:50 PM

TFS2.3 Backside power distribution for nanosheet technologies beyond 2nm, Ruilong Xie[1], Wonhyuk Hong[2], Chen Zhang[1], Jongjin Lee[2], Kevin Brew[1], Richard Johnson[1], Nicholas Lanzillo[1], Hosadurga Shobha[1], Taesun Kim[2], Panjae Park[2], Shogo Mochizuki[1], Iqbal Saraf[1], Chanro Park[1], Lei Zhuang[1], Clifford Osborn[1], Wai Kin Li[1], Feng Liu[1], Muthumanickam Sankarapandian[1], Chung Ju Yang[1], Juntao Li[1], Lukas Tierney[1], Ruturaj Pujari[1], Yasir Sulehria[1], Yuncheng Song[1], Huimei Zhou[1], Miaomiao Wang[1], Michael Belyansky[1], Somnath Ghosh[1], Haojun Zhang[1], Koichi Motoyama[1], Debarghya Sarkar[1], Wukang Kim[1], Albert Chu[1], Tao Li[1], Fabio Carta[1], Oleg Gluschenkov[1], Joongsuk Oh[2], Matthew Malley[1], Pinlei Chu[1], Son Nguyen[1], Katherine Luedders[1], Joe Lee[1], Shahrukh Khan[1], Prabudhya Roy Chowdhury[1], Huai Huang[1], Abir Shadman[1], Stuart Sieg[1], Daniel Dechene[1], Daniel Edelstein[1], John Arnold[1], Tenko Yamashita[1], Kisik Choi[1], Kang-ill Seo[2], Dechao Guo[1], Huiming Bu[1] [1]IBM, [2]Samsung

This paper examines various approaches for integrating backside power distribution network (BSPDN) with nanosheet transistor technologies. Deep Trench Via (DTV) based BSPDN schemes, except for Shifted Frontside Via Backside Power rail (SFVBP), do not offer cell level scaling benefits, but via resistance of SFVBP could remain a bottleneck. Direct Backside Contact (DBC) based schemes offer best cell level scaling. A novel self-aligned backside contact (SABC) scheme integrated with nanosheet transistors is demonstrated with immunity to misalignments in backside contact formation. The structure exhibits good device characteristics and satisfactory reliability.

2:15 PM

TFS2.4 Demonstration of Logic-Block Performance-Power Gain by 1st Generation Back Side Power Delivery Network for SoC and HPC Applications beyond 2nm Node, Hidenobu Fukutome[1], Jinkyu Kim[1], Jaehoon Shin[1], Jeewoong Kim[1], Yongwoo Lee[1], Yoonbeom Park[1], Darong Oh[1], Soohang Chae[1], Byeolhae Eom[1], Yun Suk Nam[1], Minsung Lee[1], Seungseok Ha[1], Eun Guk Chung[1], J. Kim[1], M. Jo[1], S. H. Lee[1], S. Kim[1], Keun Hwi Cho[1], Kyoung-Woo Lee[1], Dong-won Kim[1], Hag-Ju Cho[1], Ken Rim[1], San Duk Kwon[1], Jaihyuk Song[1]
[1]Samsung Electronics Co., Ltd.

We have experimentally demonstrated effects of BSPDN on performance-power of standard cell featuring Gate-all-around (GAA) FETs scaled down for SoC technology beyond 2nm node for the first time. 1st generation (Gen) BSPDN provides high immunity of cell-level leakage with ultra-scaled cell height and we achieve 6% speed gain by optimizing metal routing. As a result, 1st Gen BSPDN could make it possible to achieve 7.5% performance or 5% power gain compared to FSPDN with logic and SRAM test chip verification.

2:40 PM

TFS2.5 Backside Power Delivery in High Density and High Performance Context: IR-drop and Block-level Power-Performance-Area Benefits, Yun Zhou[1], S.C. Song[2], Halil Kukner[1], Giuliano Sisto[1], Sheng Yang[1], Anita Farokhnejad[1], Mohamed Naeim[1,3], Moritz Brunion[1], Ji-Yung Lin[1], Odysseas Zografos[1], Pieter Weckx[1], Shashank Ekbote[2], Nick Stevens-Yu[2], David Greenlawn[2], Steve Molloy[2], Geert Hellings[1], Julien Ryckaert[1]
[1]imec, [2]Google LLC, [3]Cadence Design Systems

We evaluate block-level power-performance-area (PPA) tradeoffs of two backside power (BSPDN) options: Through Silicon Via in the Middle of Line (TSVM) and Backside Contact (BSC) in an A10 (10Å) nanosheet technology node. The benchmarking was conducted for high-performance designs in both high-performance and high-density technology scenarios taking the traditional frontside power option as the baseline. HP technology clearly benefits most since its dense PDN consumes a lot of metal routing resources on the frontside to keep an acceptable IR-drop. Introducing BSPDN frees up those metals for more efficient signal routing, resulting in 19% smaller area (8% for HD). Continued standard cell scaling by means of BSC translates into a further -25% core area, with only the densest 4.5T HD results showing signs of congestion at high frequencies.

Session C13: Security

1:00 PM, Honolulu 1

Co-Chairs: Kevin Kornegay, Morgan State University
Makoto Takamiya, The University of Tokyo

1:00 PM

C13.1 Empowering Local Differential Privacy: A 5718 TOPS/W Analog PUF-based In-Memory Encryption Macro for Dynamic Edge Security, Chih-Sheng Lin[1], Bo-Cheng Chiou[1], Yin-Jia Yang[2], Jian-Wei

Su[1], Kuo-Hua Tseng[1], Yun-Ting Ho[1], Chih-Ming Lai[1], Sih-Han Li[1], Tian-Sheuan Chang[2], Shan-Ming Chang[1], Shyh-Shyuan Sheu[1], Wei-Chung Lo[1], Shih-Chieh Chang[1], Tuo-Hung Hou[2] [1]Industrial Technology Research Institute, [2]National Yang Ming Chiao Tung University
In the realm of artificial intelligence (AI), data privacy is crucial. This study demonstrates the first In-Memory Encryption (IME) macro utilizing analog Physical Unclonable Function (aPUF) for efficient local differential privacy (LDP). The hardware utilizes a highly parallel 22-nm SRAM 4b/4b/5b (I/W/O) analog in-memory computation (aIMC) macro. Sense amplifier (SA) variation and a time-based confusion (TBC) circuit generate time-varying noise, enhancing dynamic LDP protecting strength to 4.2. Furthermore, the energy efficiency of 5718 TOPS/W underscores significant advancements in robust protection without compromising high energy efficiency, particularly benefiting edge LDP security.

1:25 PM

C13.2 A 4.7-to-5.3Gbps Fault-Injection Attack Resistant AES-256 Engine Using Isomorphic Composite Fields in Intel 4 CMOS, Raghavan Kumar[1], Sachin Taneja[1], Vivek De[1], Sanu Mathew[1] [1]Intel

A fault-injection attack (FIA) resistant AES-256 engine with 100% exploitable fault coverage is fabricated in Intel 4 CMOS. Redundant round computations using isomorphic $GF(2^4)^2$ composite-field implementations and reconfigurable byte dataflow enable real-time detection of corrupted ciphertexts, while limiting area overhead to 12%. Additive masking circuits with redundant round computations show no side-channel information leakage from 1B traces.

1:50 PM

C13.3 A 67F^2 Reconfigurable PUF Using 1T2R RRAM Switching Competition in 28nm CMOS with 5e-9 Bit Error Rate, Yue Cao[1], Honghu Yang[2], Jianguo Yang[3], Qi Liu[1], Ming Liu[1] [1]Fudan University, [2]Zhangjiang Lab, [3]Institute of Microelectronics of the Chinese Academy of Sciences

Aiming at low-cost, high-reliability hardware security in IoT applications, we demonstrated a 1Mb 1T2R RRAM Reconfigurable PUF design. A 1T2R PUF cell with a smaller size utilizes the switch time variation in the RRAM device as the entropy source, and an initialization-extraction process that exploits the cycle-to-cycle switch time variation is proposed to enable PUF reconfiguration. A self-adaptive extraction circuit and a reprogram calibration scheme are designed to improve operation power and native BER. Moreover, a symmetrical read scheme is employed to enhance power analysis resilience, by balancing the power during PUF readout. The test chip achieves a cell size of 67F^2 and a native (calibrated) BER of 0.021% (< 5e-9) with good resilience to machine learning attacks.

2:15 PM

C13.4 An In-Sensor PUF Featuring Optical Reconfigurability and Near-100% Hardware Reuse Ratio for Trustworthy Sensing, Xiaojin Zhao[1], Haibiao Zuo[1], Xiaoliang Huang[1], Shiqiao Zhang[1], Chip-Hong Chang[2] [1]Shenzhen University, [2]Nanyang Technological University

Mainstream CMOS image sensors are in dire need of having built-in security primitive to facilitate on-chip trustworthy sensing for the attestation of the visual content integrity against photo-realistic spoofing attacks made feasible by the emerging generative artificial intelligence (AI) tools. This paper presents an optically reconfigurable in-sensor strong physically unclonable function (PUF) leveraging both intrinsic dark signal non-uniformity (DSNU) and photo response non-uniformity (PRNU) of photo sensing pixels as entropy sources. The fabricated 128×128 in-sensor PUF chip features 99.735% hardware reuse ratio, ~1×10^{36}bit/F^2 area efficiency, ≈2.77×10^{42} challenge-response pairs (CRP) and high resistance against several well-known machine-learning attacks.

2:40 PM

C13.5 A 65nm Delta-Sigma ADC based VDD-Variation-Tolerant Power-Side-Channel-Attack Monitor with Detection Capability down to 0.25Ω, Shota Konno[1,2], Zachary J Ellis[2], Anupam Golder[2], Sigang Ryu[2], Daniel Dinu[3], Avinash Varna[3], Sanu Mathew[3], Arijit Raychowdhury[2] [1]Asahi Kasei Microdevices Corporation, [2]Georgia Institute of Technology, [3]Intel Corporation
In this work, a Delta-Sigma ADC based Power Side Channel Attack Monitor is proposed to accurately detect insertion of less than 1Ω. A differential conversion method utilizing Dual Integrate CAP provides signal processing to compensate for drift due to VDD variations, achieving a minimum detectable resistance of 0.25Ω including VDD variations. The ultra-low power consumption of 50uW during operation makes it suitable for IoT-secure devices.

Session C14: Very High-Speed Wireline

1:00 PM, Honolulu 2

Co-Chairs: Zhipeng Li, Marvell Semiconductor
C. Patrick Yue, Hong Kong University of Science and Technology

1:00 PM
C14.1 A 0.296pJ/bit 17.9Tb/s/mm^2 Die-to-Die Link in 5nm/6nm FinFET on a 9μm-pitch 3D Package Achieving 10.24Tb/s Bandwidth at 16Gb/s PAM-4, Mu-Shan Lin[1], Chien-Chun Tsai[1], Shenggao Li[1], Tze-Chiang Huang[1], Wen-Hung Huang[1], Kate Huang[1], Yu-Chi Chen[1], Alex Liu[1], Yu-Jie Huang[1], Jimmy Wang[1], Shu-Chun Yang[1], Nai-Chen Cheng[1], Chao-Chieh Li[1], Hsin-Hung Kuo[1], Wei-Chih Chen[1], C.H. Wen[1], Kevin Lin[1], Po-Yi Huang[1], Kenny Cheng-Hsiang Hsieh[1], Frank Lee[1] [1]TSMC
This paper presents a die-to-die link with a compute die in 5nm FinFET and a SRAM die in 6nm FinFET, with a face-to-back 3D stacking at a 9µm bond pitch. Modular design that supports full scalability is demonstrated, achieving a 10.24Tb/s aggregate bandwidth for 320 Tx lanes and 320 Rx lanes, at a PAM-4 16Gb/s per lane data rate. Each data cluster is designed with 80 Tx/Rx lanes in a 378µm*378µm footprint, achieving a bandwidth density of 17.9Tb/s/mm^2 and an energy efficiency of 0.296pJ/bit per link.

1:25 PM
C14.2 A 1.1pJ/b/lane, 1.8Tb/s Chiplet over XSR-MCM Channels using 113Gb/s PAM-4 Transceiver with Signal Equalization and Envelope Adaptation using TX-FFE in 5nm CMOS, Gautam Gangasani[1], A Mostafa[1], A Singh[1], D storaska[1], D Prabakaran[1], K mohammad[1], M baecher[1], M shannon[1], M sorna[1], M wielgos[1], P Jenkins[1], P Ramakrishna[1], U Shukla[1] [1]Marvell Technology Inc.
This paper uses 113Gb/s PAM4 transceiver in 5nm CMOS to demonstrate a 1.8Tb/s chiplet, over die-to-die extremely short-reach (XSR) intra-package links, in a 8-port configuration. The 16-channels range from 1dB-12dB of loss at $F_{baud}/2$ The chiplet performance over these channels is better than BER<10^{-9}, while consuming <1.1pJ/b power and 0.22mm^2 area per lane.

1:50 PM
C14.3 A 0.9pj/b 9.8-113Gb/s XSR Serdes with 6-tap TX FFE and AC coupling RX in 3nm FinFet Technology, A. Chowdhury[1], J. Ma[2], Y. Li[2], J. Guo[2], X. Zhang[2], P. Ramakrishna[3], J. Gu[2], Y. Wang[2], L. Liang[2], U. Shukla[3], K. Mohammad[3], H. Yan[2], Y. Sun[2], M. Lin[2], Z. Jiang[2], F. Khan[2], M. Yeoh[2], C. Su[2], J. Ding[2], M. Baecher[4], S. Parker[4], H. Wang[2], M. Seymour[4], M. Wielgos[4], Ken Chang[2] [1]Marvell Technology, [2]Marvell Technology, Santa Clara, CA, [3]Marvell Technology Inc., [4]Marvell Technology
This paper presents an OIF CEI-1125G-XSR compliant short-reach SerDes with data rate from 9.8 to 113Gb/s PAM4/NRZ, implemented in 3nm finfet technology. The quarter-rate source-series terminated (SST) transmitter is implemented with 2UI-delay based MUX, supply adjusted and impedance calibrated

DAC driver to maintain constant TX swing across PVT. The receiver utilizes a unique AC-coupling-based method before and after single-stage CTLE with 4 edge and 12 data samplers. The design has a standard 3 taps FFE and an optional 6 taps FFE, as well as continuous adapted RX CTLE to track temperature drift and achieve BER<1e-14 below 8dB and <1e-12 for loss up to 10dB on both 2D and advanced 2.5D CoWoS package.

2:15 PM

C14.4 A 4x50Gb/s NRZ 1.5pJ/b Co-Packaged and Fiber-Terminated 4-Channel Optical RX, Sashank Krishnamurthy[1], Susnata Mondal[1], Junyi Qiu[1], Joseph Kennedy[1], Soumya Bose[1], Tolga Acikalin[1], Shuhei Yamada[1], James Jaussi[1], Mozhgan Mansuri[1] [1]Intel Corporation

This paper presents a 4-channel co-packaged optical RX that integrates a photodiode array, fiber termination and a transimpedance amplifier front end (TIA-FE) IC on the same package as an RX data-path IC. To achieve high sensitivity, the TIA-FE employs bandwidth extension and in-band group delay compensation techniques that are co-optimized with a ¼-rate 2-tap feed-forward equalizer (FFE) in the RX data-path. A StrongArm latch that improves noise variance by 3.5x for iso-power is introduced. Modulated by its VCSEL-based optical TX counterpart, the optical RX demonstrates 4x50Gb/s NRZ at 1.5pJ/b with BER<1e-12 and a sensitivity of -6dBm.

2:40 PM

C14.5 A 800Gb/s Transceiver for PAM-4 Optical Direct-Detection applications in 5nm FinFet Process, Marco Sosio[1], Fabio Giunco[1], Claudio Nani[1], Ivan Fabiano[1], Travis Lovitt[1], Victor Karam[1], Domenico Albano[1], Claudio Salvatore Asero[1], Nicola Codega[2], Marco Garampazzi[1], Nicola Ghittori[1], Stanley Ho[1], Enrico Monaco[1], Benjamin Reyes[1], Paolo Rossi[1], Enrico Temporiti[1], Paolo Pascale[1], Fernando De Bernardinis[1], Shawn Scouten[1], Stephen Jantzi[1] [1]Marvell Technology, [2]Marvell

This paper presents a 5nm Finfet 8x100Gb/s electro-optical transceiver for PAM-4 optical interconnects covering DR8/2xFR4/LR8 QSFP-DD/OSFP applications. Three chip flavors, differing in only few top metal masks on TXs, have been implemented providing fully integrated 3Vpp Silicon Photonics (SiPho), 3V Open Drain (OD) and 1.5Vpp EML drivers. External VCSEL drivers are supported as well. The optical receivers are DSP based, with the analog consisting of a variable gain amplifier (VGA) and an ADC. The electrical interface, common to all chips, is compliant with the OIF CEI 112G VSR and IEEE C2M standards. The chip is available both in package and as a bare die. Both versions meet the form factor and power requirements for QSFP-DD MSA enabling less than 12W 800G modules

Session C15: Interfaces to the Human Body and Sequencing

1:00 PM, Honolulu 3

Co-Chairs: Arun Manickam, Cepheid
Takashi Tokuda, Tokyo Institute of Technology

1:00 PM

C15.1 A 76 X 55 X-Ray Energy Binning Dosimeter for Closed-Loop Cancer Radiotherapy, Rahul Lall[1], Kyoungtae Lee[2], Adam Cunha[2], Rebecca Abergel[1], Youngho Seo[1,2], Ali Niknejad[1], Mekhail Anwar[1,2] [1]University of California, Berkeley, [2]University of California, San Francisco

X-ray radiation dose delivered during cancer radiotherapy is nonlinear with biological effect on cancer cells and healthy tissues, necessitating an understanding of X-ray energy deposition at the single photon level. Here we present a single X-ray sensitive, energy binning ASIC to enable closed-loop cancer radiotherapy to personalize patient treatment. We use deep n-well (DNWELL) diodes designed at low

capacitive nodes (C_{diode}), such that the miniscule energy deposition from single X-rays at these nodes generates a voltage signal large enough to be sensed ($V_{diode}=Q_{dep}/C_{diode}$), where $V_{diode} \propto$ energy deposited. To enable single photon energy resolution without the significant power and area of high resolution ADCs, we implement an analog voltage supply (AVDDH) ~log resistor grid to create a pixel sensitivity gradient for X-ray energy binning. The ASIC is highly linear with radiation dose (10–250 cGy) and accurately tracks dose up to 3 cm deep in tissue.

1:25 PM

C15.2 A 2000-Volumes/s 3D Ultrasound Imaging Chip with Monolithically-Integrated 11.7x23.4mm^2 2048-Element CMUT Array and Arbitrary-Wave TX Beamformer, Nuriel N.M. Rozsa[1], Zhao Chen[2], Taehoon Kim[1], Peng Guo[1], Yannick Hopf[1,3], Jason Voorneveld[4], Djalma Simoes dos Santos[1], Emile Noothout[1], Zu-Yao Chang[1], Chao Chen[1,3], Vincent A. Henneken[2], Nico de Jong[1,4], Hendrik J. Vos[1,4], Johan G. Bosch[4], Martin D. Verweij[1,4], Michiel A.P. Pertijs[1] [1]Delft University of Technology, [2]Philips Innovation & Strategy, [3]Sonosilicon, [4]Erasmus MC University Medical Center

This work presents an ultrasound imaging chip with monolithically integrated 32×64 element CMUT array, capable of imaging a large field-of-view (FoV) of 60°×60°×10 cm at 2000 vol/s, the highest 3D volume rate reported to date. By combining 2× time-division multiplexing (TDM) with 2×2-element micro-beamforming, it reduces the output channelcount 8×. Equalization (EQ), trained using a pseudo-random bit-sequence (PRBS) generated on-chip, reduces crosstalk caused by TDM by 19 dB, allowing for power-efficient scaling of the on-chip cable drivers. A novel transmit (TX) beamformer, implemented as a programmable digital pipeline, enables arbitrary TX beamforming with arbitrary pulse-density modulated (PDM) waveforms and drives element-level 65 V unipolar pulsers. The chip features a layout matched to the 365- µm-pitch CMUT array, and consumes 1.30 mW/ch.

1:50 PM

C15.3 A Smart Contact Lens System with 433MHz Wireless Power and Data Transfer at a Modulation Index Down to 0.02%, Heesung Roh[1], Hyun Jin Yoo[2], Si-Youl Yoo[2], Seung Hee Pyen[3], Cheonhoo Jeon[4], Jae-Yoon Sim[1] [1]POSTECH, [2]Optroth, [3]Biiogence, [4]Dankook University

This paper presents a wireless power and data transfer system for a low modulation index (MI) of smart contact lens (SCL). Two chips, Reader and Transponder, co-optimized in a full chain of 433MHz system enable data communication even at an MI of 0.02%. The bit error rate (BER) at 0.1% MI is less than $4x10^{-6}$, representing an improvement over 250 times compared to the previous best. The full system was verified *in vitro* and *in vivo* with a live rabbit.

2:15 PM

C15.4 An Intra-Body-Power-Transfer System Energized by an Electromagnetic Energy Harvester for Powering Wearable Sensor Nodes, Hyungjoo Cho[1], Dongyoon Lee[1], Hoyong Sung[1], Heewon Choee[1], Ji-Hoon Suh[1], Injun Choi[2], Donghee Cho[2], Sohmyung Ha[3], Minkyu Je[1] [1]KAIST, [2]Samsung Electronics, [3]New York University Abu Dhabi

We present an intra-body-power-transfer (IBPT) system energized by an electromagnetic (EM) energy harvester (EH). The proposed maximum-power-point-tracking (MPPT) method for EMEH offers simple implementation and fast MPPT response (or tracking) time. Also, maximum-resonant-power-tracking (MRPT) is employed for the IBPT transmitter (TX) to track the optimal resonance frequency, which varies by the environment. A demonstration with a shoe-mounted wearable node with the proposed EMEH and IBPT TX validates the proposed whole IBPT system.

2:40 PM

C15.5 A 28nm Approximate / Binary 6T CAM for Sequence Alignment, Brian Alexander Crafton[1], Samuel Spetalnick[1], Muya Chang[1], Arijit Raychowdhury[1] [1]Georgia Institute of Technology

A dense 6T CAM implementing exact and approximate search for sequence alignment is presented. Conventional binary CAM (BCAM) returns a match when the search and stored strings match exactly, approximate CAM (ACAM) returns a match when the hamming distance (HD) between the search and stored strings is within some tolerance. Using a 6T 28nm SRAM bitcell, high density (2.54 Mb/mm2) is achieved, the macro operates up to 200MHz and consumes 0.77fJ/search/bit (BCAM) and 2.37fJ/search/bit (ACAM).

Session T7: Reliability, Characterization & Modeling of Oxide Semiconductor and Si Devices-1

3:20 PM, Tapa 1

Co-Chairs: Ashish Agrawal, Intel Corp

Tetsu Ohtou, Tokyo Electron Ltd.

3:20 PM

T7.1 A New Industry Standard Compact Model Integrating TCAD into SPICE, Sanghoon Myung[1], Donggwan Shin[1], Kyeyeop Kim[1], Yunji Choi[1], Gijae Kang[1], Songyi Han[1], Jaehoon Jeong[1], Dae Sin Kim[1] [1]Samsung Electronics

We present a complete neural compact model (NCM) that can be used in industry for the first time. This supports not only the features of the standard PDK but also the new features that can vary the process conditions in SPICE, similar to TCAD simulation. Hence, we dub this “Technology Design Kit (TDK)” to distinguish it from standard PDK. With TDK, we enhanced AC performance by 5% and reduces the optimization time by 45,000 times compared to traditional DTCO. TDK will be a new industry standard for the emerging devices in the future.

3:45 PM

T7.2 Hot-Carrier-Degradation Characterization for Accurate End-of-Life Prediction with 3nm GAA Logic Technology Featuring Multi-Bridge-Channel FET, Seongkyung Kim[1], Junkyo Jeong[1], Eunyu Choi[1], Jinyoung Kim[1], Hyewon Shim[1], Shinyoung Chung[1], Paul Jung[1] [1]Samsung Electronics

In this paper, we report the hot-carrier-degradation characterization of 3nm gate-all-around (GAA) logic technology featuring multi-bridge-channel field-effect transistor (FET) for accurate end-of-life (EOL) prediction. The commonly used power-law model is compared to the saturation model in wafer level reliability (WLR). For testing devices over EOL, a long-term hot-carrier-injection (HCI) test is conducted by using package methodology. The EOL HCI Si degradation value is revealed to be less than half of the calculated value by the power-law model. The saturation model, predicted from WLR, fits to the long-term HCI test result. EOL Vmax and %Id show that the saturation model is more accurate for predicting HCI EOL. AC HCI is conducted to verify width and delay time effects on Id degradation. Id degradation from AC HCI shows that the total width time affects HCI degradation more compared to frequency.

4:10 PM

T7.3 Assessment of the transient self-heating effect and its impact on the performance of Watt-level RF power amplifier in a FinFET technology, Thanh Viet Dinh[1], Sai-Wang Tam[1], Andries Scholten[1], Lisa Tondelli[2], Ralf Pijper[1], Sri Kondapalli[1], Juan Xie[1], Alden Wong[1], Ivan To[1], Ruben Asanovski[2], Luca Selmi[2] [1]NXP Semiconductors, [2]University of Modena and Reggio Emilia

The dynamic behavior of self-heating effect in FinFET devices has a profound impact on the performance of RF circuits. Hence an accurate assessment of such transient thermal response is critical for designing successfully thermal-sensitive RF blocks in FinFET technology. This work shows, for the first time, a physics-based multi-stage approach to evaluate the thermal network of a single RF multi-fin multi-finger

FinFET transistor and the power cell comprised of such multiple transistors. This thermal assessment approach, which has been verified by intensive characterization of both on-wafer and in-packaged RF test chips, enables the first Watt-level RF power amplifier design in a baseline FinFET node.

4:35 PM

T7.4 Unlimited Bi-directional Back-Bias in FD-SOI Technology With New Dual Isolation Integration, Remy Berthelon[1], Olivier Weber[1], Frederic Ibars[1], Bertrand Revel[1], Celine Borowiak[1], Jean-Christophe Grenier[1], Benjamin Dumont[1], Simon Desmoulins[1], Pierre-Olivier Sassoulas[1], Paul Ferreira[1], Stephan Niel[1], Stephanie Chouteau[1], Rossella Ranica[1], Franck Arnaud[1], Roberto Gonella[1]
[1]STMicroelectronics
We present a novel dual isolation scheme with standard STI and + a single diffusion break local oxidation of the film in FD-SOI technology, extending its highly efficient back-bias capability. For the first time, both Forward and Reverse modes are demonstrated on the same ring-oscillator devices from 28nm FD-SOI technology. A large range of performance/leakage tuning is achieved with record voltage drop across NMOS and PMOS wells ranging [-3V,+5V]. Leveraging this capability, we experimentally demonstrate a process-induced variability reduction of ~50% on Frequency using independent NMOS/PMOS back-biasing in several regimes.

5:00 PM

T7.5 First Observation of Time Exponent Variations under Positive Bias Stress on a-IGZO Transistors Utilizing Ultrafast On-the-Fly Technique with 1 &[micro]s Delay , TAEWON SEO[1], CHANGEON JIN[1], Yoonyoung Chung[1] [1]POSTECH
For the first time, we characterized the transition in time exponent (n) of the ΔV_{TH} under positive bias stress (PBS) on a-IGZO transistors by utilizing the ultrafast on-the-fly (UF-OTF) technique to minimize the measurement delay (t_0) to be 1 µs. Due to the significant noise induced by multiple trap and release (MTR) conductions in a-IGZO, the precise reliability measurements were not conducted in the sub-millisecond range. By utilizing the UF-OTF technique with identical measurement and stress voltages, we minimized the noise and reduced the delay to 1 µs. Our study reveals the transition in n value from 0.2 to 0.4 under PBS below 4 MV/cm, which was not observed in conventional measurements (t_0: ~ 30 ms). Through comprehensive analyses, we attribute this behavior to the creation of deep-level states and the transition of V_O^{2+} to V_O inside a-IGZO, respectively.

Session T8: Emerging Non-Volatile Memories - RRAM, FeRAM, PCM, MRAM-1

3:20 PM, Tapa 2

Co-Chairs: Shimeng Yu, Georgia Institute of Technology
Hang-Ting Lue, Macronix

3:20 PM

T8.1 Highly Scalable Vertical Bypass RRAM (VB-RRAM) for 3D V-NAND Memory , Geonhui Han[1], Youngdong Kim[1], Jeaseon Kim[1], Dongmin Kim[1], Yoori Seo[1], Jinmyung Choi[2], Jinwoo Lee[2], Donho Ahn[2], Sechung Oh[2], Donghwa Lee[1], Hyunsang Hwang[1] [1]POSTECH, [2]Samsung electronics
We firstly demonstrate highly scalable interface type RRAM based 3D V-NAND memory with WO_x resistivity switching (RS) layer and IGZO selector transistor (Tr). 3D vertical interface type RRAM integrated with IGZO Tr (VB-RRAM), utilizing bypass reading between Tr and RS layer, exhibits low voltage operation (< 5 V), multi-bit (4 bit) capability, and high uniformity of the RS layer while improving the limitations of on/off ratio. Furthermore, with scaling the channel length down to 30 nm, we achieved fast

switching speed (~ 50 us), stable endurance (> 10^7 cycles), and low switching energy consumption (5 fJ). Finally, critical V-NAND issues like read disturbance and interface layer were also evaluated.

3:45 PM

T8.2 A Vertical Channel-All-Around FeFET with Thermally Stable Oxide Semiconductor Achieving High ΔIon > 2μA/cell for 3D Stackable $4F^2$ High Speed Memory, Shoichi Kabuyanagi[1], Takamasa Hamai[1], Masayuki Murase[1], Takeru Maeda[1], Masumi Saitoh[1], Shosuke Fujii[1] [1]Kioxia Corporation

We demonstrate, for the first time, a 30nm-diameter vertical Channel-All-Around (CAA) ferroelectric FET (FeFET) with TiO_2 channel, aiming at $4F^2$ high speed memory application. Thanks to Gate-Source/Drain overlap of CAA structure and interface-layer-free nature of oxide semiconductor channel, high ΔI_{on} and stable endurance are simultaneously achieved in the smallest footprint ever (707nm^2). Low aspect ratio FeFET with thermally stable crystallized TiO_2 channel facilitates multiple memory stacking. We also show the scalability of CAA FeFET without performance degradation by contact electrode optimization and spacer oxide engineering, providing a new path for future high density and high speed memory.

4:10 PM

T8.3 A Novel Chalcogenide Based CuGeSe Selector Only Memory (SOM) for 3D Xpoint and 3D Vertical Memory Applications, Wei-Chih Chien[1], J.X. Zheng[1], C.W. Yeh[1], L.M. Gignac[2], H.Y. Cheng[1], Z.L. Liu[1], A. Grun[1], C.L. Sung[1], E.K. Lai[1], S. Cheng[1], C.W. Cheng[2], L. Buzi[2], A. Ray[2], D. Bishop[2], R.L. Bruce[2], M. BrightSky[2], H.L. Lung[1] [1]Macronix, [2]IBM

We present a new selector only memory material, CuGeSe, with low program current, fast switch speed properties and good endurance. The switching mechanism is studied in depth and element migration is verified during the switching of the material. We also discuss application of the material for 3D Xpoint and 3D vertical memory, as well as propose a modified 1/3 V testing scheme for 3D vertical memory to mitigate leakage current and improve scaling.

4:35 PM

T8.4 First Demonstration of BEOL-Compatible Vertical Fe-NOR, Yang Feng[1,2], Dong Zhang[1], Zijie Zheng[1], Chen Sun[1], Gan Liu[1], Zuopu Zhou[1], Jixuan Wu[2], Jiezhi Chen[2], Xiao Gong[1] [1]Department of Electrical and Computer Engineering, National University of Singapore (NUS), [2]School of Information Science and Engineering, Shandong University

For the first time, we present and experimentally demonstrate a Fe-NOR memory unit cell featuring a 3D stacked structure and side-Fin with the back-end-of-line (BEOL) vertical ZnO channel ferroelectric-metal-insulator-semiconductor (MFMIS) transistor. Capitalizing on the MFMIS architecture's advantages with side-Fin, the proposed unit cell offers a tunable and substantial memory window (MW) accompanied by an on/off ratio (I_{on}/I_{off}) of five orders of magnitude. The utilization of ferroelectric (FE) enables low switching voltage, leading to low programming voltage (4V) and fast programming speed (200ns) within the 3D NOR structure. Inspired by computing in memory (CIM) applications, great linearity and endurance are achieved. Benefiting from the 3D monolithic integration capability of FeFET along with the high-density flexible structure of 3D FeNOR architecture, this technology holds promise for a diverse array of applications, including storage-class memory (SCM) and CIM.

5:00 PM

T8.5 Reliable Low-voltage FeRAM Capacitors for High-speed Dense Embedded Memory in Advanced CMOS, Sou-Chi Chang[1], Christopher Neumann[1], Bernal Granados Alpizar[1], Sarah Atanasov[1], Jason Peck[1], Nafee Kabir[1], Yu-Ching Liao[1], Shriram Shivaraman[1], Wriddhi Chakraborty[1], Nazila Haratipour[1], I-Cheng Tung[1], Vladimir Nikitin[1], Gary Allen[1], Thomas Hoff[1], Adedapo Oni[1], Tristan Tronic[1], Anandi Roy[1], Hai Li[1], Fatih Hamzaoglu[1], Matthew Metz[1], Ian Young[1], Jack Kavalieros[1], Uygar Avci[1] [1]Intel

For the first time, anti-ferroelectric (AFE) hafnia-based capacitors compatible to advanced CMOS are demonstrated by (i) bit-line (BL) and plate-line (PL) WRITE (W) voltage scaling down to 1V and 1.3V, respectively, (ii) BL READ (R) voltage scaling down 0.6V, and (iii) robust 10yr reliability at elevated temperature in both fatigue and breakdown, while delivering switching charge for high-speed dense embedded memory. Also, frequency-dependent endurance in ferroelectric (FE) or AFE hafnia is shown to unveil the worst-case scenario for cache-level memory application as well as complex interactions between defects and electric field. Finally, 2.4 to 6.5X cell density over SRAM and sub-100fJ W/R cell energy are projected for embedded FeRAM, showing integrating low-voltage AFE capacitors with advanced logic has great performance potential for next-generation low-power and high-speed dense embedded memory.

Session T9: Monolithic and Heterogeneous Integration
3:20 PM, Tapa 3

Co-Chairs: Mike DeLaus, Analog Devices
Osbert Cheng, UMC

3:20 PM
T9.1 Integration of Si-Interposer and High Density MIM Capacitor on 2.5D Foveros Face-to-Face Architecture, Chris Pelto[1], Daming Wei[1], Ravi Aggarwal[1], Ramiz Ahan[1], Mark Armstrong[1], Mehmet Bebek[1], Mark Blount[1], Shafiul A Chowdhury[1], Jia Yun Chuah[1], Chris Connor[1], Thomas DeBonis[1], Babita Dhayal[1], Austin Dougless[1], Shripad Gokhale[1], Amit Jain[1], Vishal Javvaji[1], Kirankumar Kamisetty[1], Gwang-Soo Kim[1], Joel Kpetehoto[1], Chin Lee Kuan[1], Che-yun Lin[1], Guannan Liu[1], Yunzhe Ma[1], Gray Mcpherson[1], Scott Mokler[1], Sanjay Natarajan[1], Christopher Perini[1], Rahul Ramaswamy[1], Bernhard Sell[1], Ramesh Subramaniam[1], James Waldemer[1], Yang Yang[1], Yihong Yang[1], Jack Yaung[1], Babak Sabi[1] [1]Intel
Integration of different computing elements through silicon interposers enables scaling opportunities beyond Moore's law. Intel's passive Si-Interposer enables interconnections among different chiplets using Through Silicon Via (TSV) technology along with a refined 36µm micro-bump pitch in a face-to-face die configuration. The Si-Interposer houses a high-density metal-insulator-metal (HDMIM) integrated decoupling capacitor for voltage droop reduction and noise suppression. Products can either utilize HDMIM in the Si-Interposer die, a built in HDMIM in the chiplet die, or both. Paper describes HDMIM fabrication steps, electrical properties, reliability benchmarks, and performance enhancements by incorporation of Si-Interposer HDMIM.

3:45 PM
T9.2 Mitigating line-break defectivity with a sandwiched TiN or W layer for metal pitch 18 nm aspect ratio 6 semi-damascene interconnects , Anshul Gupta[1], Souvik Kundu[1], Stefan Decoster[1], Kaushik Sah[2], Gilles Delie[1], Brecht Truijen[1], Davide Tierno[1], Giulio Marti[1], Olalla Varela Pedreira[1], Bart Kenens[1], Yannick Hermans[1], Christoph Adelmann[1], Bart de Wachter[1], Ivan Ciofi[1], Gayle Murdoch[1], Andrew Cross[1], Seongho Park[1], Zsolt Tokei[1] [1]imec, [2]KLA
A novel metal stack scheme with a sub-nm, sandwiched TiN or W layer, a so-called defect mitigation layer (DML) between Ru is proposed and found to be less prone to lateral attack and line-break formation during direct-metal-etch (DME) of Ru semi-damascene (semi-D) lines compared to those without DML. With increasing thickness (t_k) of TiN-DML, we achieve up to 5x lower defect density and resistance (R) yield >99%, <5% 1σ of R on AR~4-6, CD~6-11 nm, metal pitch (MP)=18-26 nm lines. The improvement is higher on AR~6 lines than AR~4 which makes DML a promising approach to enable AR≥6 semi-D interconnects. No R penalty is found with TiN-DML for the investigated line lengths >10 µm. Thermal shock reliability test shows good quality of HAR Ru line interfaces with TiN-DML.

4:10 PM

T9.3 Backside Power Delivery with relaxed overlay for backside patterning using extreme wafer thinning and Molybdenum-filled slit nano Through Silicon Vias, Peng Zhao[1], Liesbeth Witters[1], Anne Jourdain[1], Michele Stucchi[1], Nicholas Jourdain[1], Jan Willem Maes[2], Harsh Vardhan Bana[2], Chiyu Zhu[2], Rami Chukka[1], Farid Sebaai[1], Kevin Vandersmissen[1], Nancy Heylen[1], Daniel Montero[1], Shouhua Wang[1], Koen D'Have[1], Filip Schleicher[3], Joeri De Vos[1], Gerald Beyer[1], Andy Miller[1], Eric Beyne[1] [1]imec, [2]ASM, [3]KLA

Long slit nano Through Silicon Vias (nTSV) are used for high density connections between frontside (FS)-patterned Burried Power Rails (BPR) and orthogonally patterned metal rails on the wafer backside (BS). The length of the slits can be tuned to relax overlay requirements for BS patterning that are typically stringent due to wafer grid distortions in bonding. Extreme wafer thinning stopping on 10nm $Si_{0.75}Ge_{0.25}$ etch stop layer (ESL) is enabled using an optimized thinning sequence. For the first time, low resistance barrier-free Molybdenum (Mo)-filled nTSVs are demonstrated, confirming the potential for further scaling compared to TiN/W filled counterparts.

4:35 PM

T9.4 Toward 0 V ESD protection in 2.5D/3D advanced bonding technology, SHIH-HSIANG LIN[1], Marko Simicic[1], Nicolas Pantano[1], Shih-Hung Chen[1], Geert Van der Plas[1], Eric Beyne[1], Piet Wambacq[1] [1]imec

This paper presents a methodology to help prevent overdesign of Electrostatic Discharge (ESD) protection circuits for internal I/O in 2.5D/3D bonding technologies. We explore how the voltage suppression effect mitigates voltage-driven gate oxide breakdown during stacking and emphasize the role of series resistance in reducing peak discharge current. Our findings indicate that highly variable non-contact discharges are not a concern in advanced bonding technologies, shifting the focus to more predictable contact discharges. Also, we provide guidelines to design efficient ESD protection circuits for internal IO in 2.5D/3D stacked system.

5:00 PM

T9.5 Material, Process and System Level Analysis for Parasitic Reduction of Next Generation Logic Technology in conjunction with Backside Power Delivery, Ashish Pal[1], Sefa Dag[1], Pratik B. Vyas[1], Gregory Costrini[1], Vinod Reddy[1], Veeraghavan Basker[1], Allen Yeong[1], Benjamin Colombeau[1], Bala Haran[1], Subi Kenegeri[1], El Mehdi Bazizi[1] [1]Applied Materials

The first generation of backside power delivery network (BS-PDN Gen-1), implemented with a backside power via (BPV) has been shown to introduce additional parasitic capacitances, thus degrading the standard cell performance by 2.5% compared to FS-PDN, and limits the performance benefit at processor-level. In view of this, we propose an advanced metal gate-cut (MG-cut) process with low-K dielectric gate-cut fill for capacitance reduction. Our MSCO™ platform shows that BS-PDN circuit performance can be fully recovered with these 2 modifications. In addition, these modifications in combination with BSPDN, also improve SRAM read and write delay by 8% and 17%, thus bringing significant performance benefit for next generation GAA logic nodes.

Session C16: Memory Circuits

3:20 PM, Honolulu 1

Co-Chairs: Andreas Burg, EPFL
Satoru Takase, KIOXIA Corp.

3:20 PM

C16.1 An Offset-Compensated Charge-Transfer Pre-Sensing Bit-Line Sense-Amplifier for Low-Voltage DRAM, Kyeongtae Nam[1], Jaehyuk Kim[1], Dongil Lee[1], Kyuchang Kang[1], Sangyun Kim[1], Changyoung Lee[1],

Hyunchul Yoon[1], Donggeon Kim[1], Bokyeon Won[1], Jaejoon Song[1], Incheol Nam[1], Young-Hun Seo[1], Jeong-Don Ihm[1], Changsik Yoo[1], Sangjoon Hwang[1] [1]Samsung Electronics
A bit line sense amplifier (BLSA) with offset compensated charge transfer pre-sensing (OC-CTPS) scheme is implemented using 14nm DRAM process. The offset compensation (OC) is operated by diode connection without additional size overhead for BLSA. Average fail bit rate (FBR) attributed to a mismatch of charge transfer transistor is reduced by 94 % after performing OC. Furthermore, OC-CTPS BLSA accomplishes a 3sigma window, representing the FBR under 3sigma (=0.1349%) over charge transfer time (t_{CT}). The 3sigma window has widths of 250 ps and 500 ps at temperatures of -25 ℃ and 100 ℃, respectively, without changing voltages for charge transfer. Moreover, our approach ensures robust and stable sensing even at operating voltages as low as 0.75 V, compared to conventional OC BLSA.

3:45 PM

C16.2 A 3nm Fin-FET 19.87-Mbit/mm² 2RW Pseudo Dual-port 6T SRAM with High-R Wire Tracking and Sequential Access Aware Dynamic Power Reduction, Tomotaka Tanaka[1], Yuichiro Ishii[1], Makoto Yabuuchi[1], Yumito Aoyagi[1], Masaya Hamada[1], Kazuto Mizutani[1], Koji Nii[1], Hidehiro Fujiwara[2], Isabel Wang[2], Hong-Chen Cheng[2], Hung-Jen Liao[2], Tsung-Yung Jonathan Chang[2] [1]TSMC Design Technology Japan, [2]TSMC
A 2-read/write (2RW) pseudo dual-port (PDP) 6T SRAM is developed on 3nm Fin-FET technology. To improve performance, high-R wire tracking is introduced to adjust between margin, obtaining the optimum speed over various sign-off conditions. In addition, to reduce the dynamic power, the pre-charge control circuits are newly proposed to be aware of the 1st and 2nd sequential accesses. Meaningless bitline pre-charges for the 2nd access are eliminated in either all columns or selected columns, reducing the dynamic power in bitlines by up to 43 %. The fabricated 288-kbit 2RW PDP SRAM macro achieves the highest world record of 19.87 Mbit/mm² bit-density thanks to PDP design.

4:10 PM

C16.3 A 7GHz High-Bandwidth 1R-1RW SRAM for Arm HPC Processor in 3nm Technology, Rahul Mathur[1], Rajiv Kumar Sisodia[1], Andy W Chen[1], Arjun Singh[1], Sriram Thyagarajan[1], Antonio Cubeta[1], Corentin Andrieux[1], Andrew Sowden[1], YK Chong[1] [1]Arm
This paper presents an advancement in memory architecture with the introduction of 1Read-1ReadWrite (1R1RW) High Bandwidth Instance (HBI) memory, seamlessly integrated into the Arm flagship High Performance Computing (HPC) processor. Enhancing the conventional 8T-1R1W memory, HBI features an additional read port, achieving 1R1RW capability. The utilization of HBI memory in L1-Data cache doubles the available read bandwidth and results in an improvement in processor IPC, exceeding 1%. Furthermore, leveraging the HBI-1R1RW memory architecture, HBI-Ddata memory is developed to reduce the routing congestion and delay in the CPU physical design, leading to a 13% reduction in area and a 10-15ps reduction in routing delay. A test vehicle in the state-of-the-art 3nm process demonstrates 100% yield of 1R1RW HBI and highest reported frequency of more than 7GHz and lowest reported bit density of 11.2 Mbit/mm² for any 8T SRAM memory.

4:35 PM

C16.4 A 3.3GHz 1048X640 Multi-Bank Single-Port SRAM with Frequency Enhancing Techniques and 0.55V-1.35V Wide Voltage Range Operation in 3nm FinFET for HPC Applications, Ming-Chieh Huang[1], Wei Wing Mar[1], Shankar Kanade[1], Boris Bai[1], Aditya Gayatri[1], Krishna Khairnar[1], Amy Lai[1], Yu-Hao Hsu[1], Hung-Jen Liao[1], Yih Wang[1], Tsung-Yung Jonathan Chang[1] [1]TSMC
This paper presents high-speed SRAM macros of 0.64Mbit (1024x640) and 1.28Mbit (2048x640) implemented using a high-current single port 6T bitcell. The macros achieve the best FoM defined as (density × frequency)/(read power + write power). Several performance-enhancing circuit techniques are

proposed, including wordline, global clock, and global bitline boosting. Split drivers for decoder signals are proposed to achieve an overall 37% speed improvement while avoiding a repeater area tax. A read assist circuit is proposed to improve Vmax to 1.35V. Silicon results demonstrate the ability to achieve 3.3GHz at 1.0V/100°C in 3nm FinFET technology.

5:00 PM

C16.5 A 14nm 128Mb eMRAM Implemented with 17.88Mb/mm² at 0.60V for Auto-G1 Applications, Gyuseong Kang[1], Hyunjin Shin[1], Sanggyeong Won[1], Dohui Kim[1], Kyuseong Kim[1], Soohoh Seol[1], Sunkyu Lee[1], Hangil Lee[1], Yeonho Jung[1], Jaechul Shim[2], Kiseok Suh[1], Sohee Hwang[1], Daehyun Jang[1], Sangyeop Baeck[1], Sei Seung Yoon[1] [1]Foundry Business, Samsung Electronics, [2]R&D center, Samsung Electronics

This paper presents an embedded STT-MRAM with circuit techniques to mitigate read margin degradation in high temperature for automotive grade 1 application. Local read assist circuit (LRA) can minimize resistance mismatch between data and reference read path. Temperature tracking circuit (TTC) is employed to change reference resistance adaptively and control negative wordline voltage generator for reliable read operation in high temperature. The proposed 128Mb 256-IO MRAM macro is implemented in 14nm FinFET process with 17.88Mb/mm2. Measurements results show successful 11ns read operation across -40C to 160C with 0.60V core voltage.

Session C17: Power Management Techniques

3:20 PM, Honolulu 2

Co-Chairs: Qinwen Fan, TU Delft
Po-Hung Chen, National Yang Ming Chiao Tung University

3:20 PM

C17.1 A Monolithic 5.7A/mm² 91% Peak Efficiency Scalable Multi-Stage Modular Switched Capacitor Voltage Regulator with Self-Timed Deadtime and Safe Startup for 3D-ICs, Jingshu Yu[1], Xiaosen Liu[1], Minxiang Gong[1], Nicolas Butzen[1], Sheldon Weng[1], Harish K Krishnamurthy[1], Krishnan Ravichandran[1], Ramez H Ahangharnejhad[1], Waldemer Jim[1], Pelto Christopher[1], James W Tschanz[1], Vivek De[1] [1]Intel Labs

This paper presents a monolithic Multi-stage Modular Switched Capacitor Voltage Regulator (MMSCVR) in 16nm CMOS with scalable design (up to 7A), self-timed deadtime generator, and safe startup for vertical power delivery in heterogeneous 3D-ICs. The proposed MMSCVR demonstrates 90.6% peak efficiency and 5.7A/mm² peak current density with a 3V-to-1V conversion – 4.9× higher than state-of-the-art. It is also the first monolithic 4V-to-1V MMSCVR, achieving 7.8× higher current density than prior arts with off-chip capacitors.

3:45 PM

C17.2 A μW Output Power, >100V, Single-Capacitor Switched DC-DC Up/Down Converter, Rohit Rothe[1], Jungho Lee[1], Zichen Fan[1], Li-Yu Chen[1], Donguk Seo[2], Yoonmyung Lee[2], Dennis Sylvester[1], David Blaauw[1] [1]University of Michigan, Ann Arbor, [2]Sungkyunkwan University

This work presents a switched capacitor high voltage (HV) DC-DC converter with a single off-chip flying capacitor (SOF) for uW current draw applications. This converter is capable of up-conversion as well as down-conversion using the same ladder. It achieves efficiency of 62% in up-conversion mode (175V output) and 43% in down-conversion mode (184V input). Up-conversion efficiency is 16× higher than state-of-the-art converters with >100V output and nA output load.

4:10 PM

C17.3 A 6.78 MHz Wireless Power and Data Transfer System Achieving Simultaneous 52.6% End-to-End Efficiency and 4.0 Mb/s Forward Data Delivery with Interference-Free Rectifier, Quanrong Zhuang[1], Junyi Sun[1], Xusheng Zhang[1], Bo Li[1], Yi Shi[1], Hao Qiu[1] [1]School of Electronic Science and Engineering, Nanjing University, China

In this work, we presented a wireless power and data transfer (WPDT) system utilizing the fundamental and harmonic components of the bridge inverter to transfer power and data, respectively. The conventional full bridge rectifier (FBR) introduces the interference voltage and could cause the problem of data flipping, which is solved by the proposed interference-free rectifier (IFR). Additionally, a tapped coil three capacitor (TL3C) topology was proposed to maximize the data channel gain without affecting the power channel gain. A 6.78 MHz system was implemented with the IFR fabricated in 180 nm CMOS process. It supported simultaneous 82 mW load power (P_{Load}) and 4.0 Mb/s forward data rate (DR) at 52.6 % end-to-end efficiency (η_{E2E}).

4:35 PM

C17.4 A 0.6-1 V VIN Soft-Switching Low Dropout Regulator With 31.3 A/mm2 Current Density, 99.99% Current Efficiency, and 2.04 fs FoM, Jeongmyeong Kim[1], Changjoo Park[1], Wanyeong Jung[1] [1]KAIST

This paper presents a soft-switching LDO, which takes advantages of analog and digital LDOs. A soft quantizer enables smooth switching of power FETs like an analog LDO. Inverter-based buffers provide rail-to-rail output voltages to power FETs like a digital LDO and offer fast transient response using a push-pull structure even with a small dropout voltage (VDO) of 50 mV. A test chip fabricated in a 65 nm CMOS process achieves a high current density of 31.3 A/mm2 at 1 V VIN, a current efficiency of 99.99% at 0.6 V VIN, and a fast transient response of a 102 mV voltage droop at a 90 mA/4 ns load condition with a 0.6 V VIN.

5:00 PM

C17.5 A 400-ns-Settling-Time Hybrid Dynamic Voltage Frequency Scaling Architecture and Its Application in a 22-Core Network-on-Chip SoC in 12-nm FinFET Technology, Erik Loscalzo[1], Martin Cochet[2], Joseph Zuckerman[1], Samira Zaliasl[3], Michael Lekas[3], Stephen Cahill[3], Tianyu Jia[4], Karthik Swaminathan[2], Maico Cassel dos Santos[1], Davide Giri[1], Hesam Sadeghi[3], Joseph Meyer[3], Noah Sturcken[3], David Brooks[4], Gu-Yeon Wei[4], Luca Carloni[1], Pradip Bose[2], Kenneth Shepard[1] [1]Columbia University, [2]IBM Reserach, [3]Ferric Inc., [4]Harvard University

We have developed a dynamic-voltage-and-frequency- scaling (DVFS) architecture that combines a package- integrated buck voltage regulator (PIVR) with fully standard- cell-based digital low-dropout regulators (LDO) to support fine-grained control at the scale of individual cores in a 22-core system-on-chip (SoC) with a settling time of 400ns. The PIVR has a power density of 309mW/mm2 and features full back-end integration of magnetic-core power inductors. During a workload study on the SoC consisting of four general-purpose RISC-V cores and 18 specialized accelerators, our hybrid voltage regulator (HVR) showed the highest power savings when compared with other power management techniques for workload durations above 1.3µs and peak power savings of 23% over the baseline without DVFS.

Session C18: Data Converter Techniques

3:20 PM, Honolulu 3

Co-Chairs: Nereo Markulic, imec
Yun-Shyiang Shu, MediaTek Inc.

3:20 PM

C18.1 A 100kHz-BW 99dB-DR Continuous-Time Tracking-Zoom Incremental ADC with Residue-Gain Switching and Digital NC-FF, Ye-Dam Kim[1], Jae-Hyun Chung[1], Kent Edrian Lozada[1], Chang-Un Park[1], Kun-Woo Park[1], Kwan-Hoon Song[1], Young-Hoon Moon[1], Min-Jae Seo[2], Seung-Tak Ryu[1] [1]KAIST, [2]University of Seoul

This paper proposes a continuous-time (CT) tracking-zoom (TZ) incremental ADC (I-ADC) that reuses a quantizer for both the coarse SAR and fine DSM stages. The TZ I-ADC addresses the input bandwidth (BW) limitation issue with simple DAC code update. A residue-gain (RG) switching technique is proposed to mitigate the inconsistent signal transfer function (STF) in the fine CT incremental DSM (I-DSM). A digital noise-coupling-feedforward (DNC-FF) architecture is proposed to reduce the out-of-band gain (OBG). Fabricated in a 180nm CMOS process, the prototype consumes 2.52mW under a 1.8V supply, achieving 99-dB DR, 93.8-dB SNDR, and 102.5-dB SFDR.

3:45 PM

C18.2 A Low-OSR 5th-Order Noise Shaping SAR ADC Using EF-EF-CIFF Structure with PVT-Robust Differential V-T-V Converter, Yu-Hsiang Huang[1], Bao-shu Liu[1], Chih-Cheng Hsieh[1] [1]National Tsing Hua University

This paper presents a low-OSR 5th-order noise-shaping (NS) SAR (NS-SAR) ADC featuring a differential-Voltage-Time-Voltage (dVTV) converter. It introduces an innovative EF-EF-CIFF structure that achieves 5th-order NS with only two amplifications using the proposed dVTV converter. The PVT-robust dVTV converter enables the optimization of the Noise Transfer Function (NTF) without the need for static-power consumption, gain calibration, and trimming banks, thereby reducing circuit complexity and power consumption. The ADC has been prototyped and verified in 40nm CMOS technology with an active area of 0.059mm^2. Operating at a supply voltage of 1.1V and a sampling rate of 5MS/s, it achieves an SNDR of 81.8dB over a 625kHz bandwidth. The resulting Schreier Figure of Merit (FoMs) and Walden FoM (FoMw) are 181.8dB and 7.2fJ/conversion-step, respectively.

4:10 PM

C18.3 Synthesizable 10-bit Stochastic TDC Using Common-Mode Time Dithering and Passive Approximate Adder With 0.012mm^2 Active Area in 12nm FinFET, Qiaochu Zhang[1,2], Shiyu Su[1,3], Baishakhi Biswas[1], Sandeep Gupta[1], Mike Shuo-Wei Chen[1] [1]University of Southern California, [2]University of Virginia, [3]University of Waterloo

This paper presents 10-bit synthesizable stochastic TDC (STDC) with common-mode time dithering and passive approximate adder for lowering implementation cost while maintaining high linearity. Two STDCs prototypes achieve energy efficiency of ~160dB, while the one using passive approximation adder achieves area efficiency of 19.1µm^2/step.

4:35 PM

C18.4 A 71.5-dB SNDR 475-MS/s Ringamp-Based Pipelined SAR ADC with On-Chip Bit-Weight Calibration, Chao Chen[1], Zhu Yuan[1], Peng Cao[1], Jiawei Xu[1], Zhiliang Hong[1] [1]State Key Laboratory of Integrated Chips and Systems, Fudan University, Shanghai, China

This paper presents a 13-bit 475-MS/s single-channel pipelined SAR ADC, which utilizes a ring amplifier (ringamp) for residue amplification through an improved bias scheme and common-mode feedback (CMFB). Moreover, the ADC exploits an on-chip bit-weight calibration with signal-dependent pseudo-random noise (PN) injection and a window detector to correct the interstage gain error and DAC mismatch, requiring only 4096 PN-injected samples to calibrate the gain error in the background. As a result, this work achieves a peak SNDR of 71.5dB and consumes 9.93mW from a 1V supply. This corresponds to a state-of-the-art FoMs of 175.3dB and FoMw of 6.8fJ/conv-step.

5:00 PM

C18.5 A Single-Channel, 1-GS/s, 10.91-ENOB, 81-dB SFDR, 9.2-fJ/conv.-step, Ringamp-Based Pipelined ADC with Background Calibration in 16nm CMOS, Jorge Lagos[1], Pratap Renukaswamy[1], Nereo Markulic[1], Ewout Martens[1], Jan Craninckx[1] [1]imec

We present a single-channel ADC that exploits muti-bit pipelined stages based on ring amplification to simultaneously achieve high linearity, bandwidth, and power efficiency. A very-wide tuning range comparator is introduced in the stage quantizers, which not only enables multi-bit quantization but is also leveraged for the injection of dither to calibrate DAC mismatch and inter-stage gain in the background. Implemented in a 16nm FinFET process, it achieves 10.91 ENOB and 81 dB SFDR at 1 GS/s, consuming 17.8 mW from a 0.9 V supply, resulting in a Walden FoM of 9.2 fJ/conv.-step.

Thursday, June 20
Session JFS4: Biomedical Technologies
8:00 AM, Tapa 1

Co-Chairs: Emmanuel Quevy, Probius
Yuta Shiratori, NTT Corporation

8:00 AM

JFS4.1 Highly Sensitive Multimodal CMOS Antifouling Sensor Array with Multi-Use Electrodes for Single-Cell-Level Profiling of Biophysical and Biochemical Parameters, Hangxing Liu[1], Fuze Jiang[1], Adam Wang[1], Zhikai Huang[1], Ying Kong[1], Marco Saif[1], Dongwon Lee[1], Thomas Burger[1], Jing Wang[1], Hua Wang[1] [1]ETH Zürich

Monitoring cell bio-responses in organ-on-chip platforms is crucial for accurately predicting organ reactions to medications over time. This work presents an antifouling CMOS sensor platform for *in-vitro*, single-cell-level and multimodal sensing of biophysical and biochemical parameters in cell proliferation and inflammation. The chip features 4,096 sensing pixels at 45-µm spatial resolution. Each pixel node offers four sensing modalities (impedance tomography, electrochemistry, shadow imaging, and pH sensing) and three actuation functions (dielectrophoresis (DEP) as well as voltage and current stimulations).

8:25 AM

JFS4.2 A 65nm Neuromorphic Bio-signal Encoder with Compute-in-Entropy Architecture 7.13nJ Privacy-preserving Encoding and 2.38Mb/mm^2 Encoding Memory Density , Boyang Cheng[1], Jianbo Liu[1], Steven Davis[1], Zephan M. Enciso[1], Likai Pei[1], Muya Chang[1], Ningyuan Cao[1] [1]University of Notre Dame

This paper presents a neuromorphic bio-signal encoder for privacy-critical smart health applications featuring a novel compute-in-entropy architecture for hardware-efficient, physically-unclonable hyperdimensional encoding. The test chip achieved privacy-preserving bio-signal encoding with 7.13 nJ efficiency, 2.38 Mb/mm^2 item memory density, and in-situ decision-making and learning capabilities.

8:50 AM

JFS4.3 A Subcellular-Resolution Multimodal CMOS Biosensor Array with 16K Ion-Selective Pixels for Real-Time Monitoring Potassium Dynamics, Hangxing Liu[1], Fuze Jiang[1], Ying Kong[1], Dongwon Lee[1], Yuguo Sheng[1], Adam Wang[1], Zhikai Huang[1], Marco Saif[1], Thomas Burger[1], Jing Wang[1], Hua Wang[1] [1]ETH Zürich

Ion sensing offers an efficient tool for deep understanding of ion channel-related diseases such as K^+ for hyperproliferative tumors. In this work, we present the first biocompatible ion-selective bioimaging array for cellular characterization and modulation, fully integrated in a CMOS chip with 16K multi-modal pixels at a subcellular 5.4-µm-pitch resolution. This multimodal CMOS cell interfacing array consists of in-pixel

biosensing/actuation circuits for cell localization, ion-selective concentration monitoring, and plasma membrane stimulation.

9:15 AM

JFS4.4 A Pulsed Electrochemistry Readout IC with Slew-rate Booting Technique and Phase-domain ΔΣ ADC for Si-Nanowire Electrical Double-layer Capacitance Measurement, Po-Hsun Chu[1], Cheng-Tse Tsai[1], Yu-Siang Chou[1], Nitish Kumar[2], Shu-Ping Lin[2], Yu-Te Liao[1] [1]National Yang Ming Chiao Tung University, [2]National Chung Hsing University

This paper presents a pulse-driven method for detecting cardiac Troponin I using an electrical double-layer (EDL) capacitance sensing readout circuit and an on-chip pattern generator. The pattern generator is equipped with a slew rate-boosting driver circuit capable of handling EDL capacitance ranging up to 100 nF with a slew rate greater than 6.6 V/µs while consuming only 13.5 µW. Additionally, the design achieves a dynamic range (DR) of 77.4 dB by implementing an oscillator-based readout circuit and a limit of detection (LoD) of 200 fg/mL in an undiluted PBS solution with a total power consumption of 120 µW.

Session JFS5: Image Sensors

8:00 AM, Tapa 2

Co-Chairs: Bruce Rae, STMicroelectronics
Yoshiaki Kikuchi, Sony Semiconductor Solutions

8:00 AM

JFS5.1 A 336 x 240 backside-illuminated 3D-stacked 7&[mu]m SPAD for LiDAR sensor with PDE 28% at 940nm and under 0.4% depth accuracy up to 10m, Jaehyung Jang[1], Jongchae Kim[1], Sunho Oh[1], Kyungsu Byun[1], Dahwan Park[1], Jihee Han[1], Hanseung Lee[1], Suhyun Yi[1], Hoonmoo Choi[1], Jongeun Kim[1], Namil Kim[1], Yongtae Gim[1], Minkyu Kim[1], Sangyoung Lee[1], Hansang Kim[1], Eunchang Lee[1], Minsang Yu[1], Jeongjoon Hwang[1], Seunghyun Yoon[1], Kwang Hwangbo[1], Heesang Kim[1], Ahyoung Cho[1], Taejun Baek[1], Sooyoung Park[1], Kwangjun Cho[1], Wonje Park[1], Kyung-do Kim[1], Hoesam Jeong[1], Hoon-sang Oh[1], Chang-rock Song[1] [1]SK hynix Inc., CIS Development

Single photon avalanche diode (SPAD) is a key technology in light detection and ranging (LiDAR) sensors, which are gaining prominence as next-generation image sensors. We designed SPAD with high photon detection efficiency (PDE) using a backside-illuminated hybrid bonding 3D-stacked technology. This is aimed at developing a LiDAR sensor with good depth accuracy. We achieved a PDE of 28% at λ = 940nm and a low-level dark count rate (DCR) by applying the trench guide (TG) and the small lens array (SLA) structure and optimizing pixel design. As a result, we achieved a depth accuracy of less than 0.4% up to 10m.

8:25 AM

JFS5.2 A Temporal Noise Reduction via 40% Enhanced Conversion Gain in Dual-Pixel CMOS Image Sensor with Full-Depth Deep-Trench Isolation and Locally Lowered-Stack Technology, Seunghwan Lee[1], Jeongjin Cho[1], Shinyoung Choi[1], Sung Yoon Min[1], Eunjung Lee[1], Minji Jung[1], Kyoungmok Son[1], Hyunchaul Jeong[1], Heetak Han[1], Sachoun Park[1], Sanghyuck Moon[1], Seungki Jung[1], Junseok Yang[1], Taesub Jung[1], Howoo Park[1], Bumsuk Kim[1], Kyungho Lee[1], Jesuk Lee[1] [1]Samsung Electronics

We demonstrate a dual-pixel CMOS image sensor (CIS) with full-depth deep-trench isolation (FDTI) and locally lowered-stack (LLS) structure. When the LLS structure is adopted, the floating diffusion (FD) metal capacitance is dramatically reduced, resulting in a 40% increase in conversion gain (CG) and a 25% improvement in temporal noise (TN). We also present TN analysis from the perspective of the feedback circuit scheme.

8:50 AM

JFS5.3 High-Resolution and Compact Integrated FMCW-LiDAR Chip with 128 Channels of Slow Light Grating Antennas, Yuya Maeda[1], Yoshiki Ebiko[1], Haruhiko Terada[1], Ryo Tetsuya[1], Shunji Maeda[1], Yotaro Yasu[1], Takemasa Tamanuki[2], Mikiya Kamata[2], Keisuke Hirotani[2], Saneyuki Suyama[2], Kohei Yamamoto[2], Shota Nawa[2], Riku Kubota[2], Toshihiko Baba[2] [1]Sony Semiconductor Solutions Corporation, [2]Yokohama National University

This paper introduces compact solid-state optical beam scanning technology, slow light grating (SLG) based on photonic crystal waveguide. We implemented the successful implementation of a frequency modulated continuous wave (FMCW) LiDAR chip, featuring 128 channels equipped with the developed SLG antennas. Our design incorporates an upward radiating structure in an antenna array with a fine pitch of 40 µm and a total footprint of 5.14 mm × 1.20 mm, respectively. Using this chip, we successfully performed a FMCW measurements and point cloud mapping.

9:15 AM

JFS5.4 A 30fps 64 X 64 CMOS Flash LiDAR Sensor with Push-Pull Analog Counter Achieving 0.1% Depth Uncertainty at 70m Detection Range, Dongseok Cho[1,2], Byungchoul Park[1], Hyun-Seung Choi[3], Myung-Jae Lee[3], Youngcheol Chae[1] [1]Yonsei University, [2]Samsung Electronics, [3]KIST

This paper presents a CMOS flash LiDAR sensor based on a time-gated single-photon counting method. The proposed 64×64 sensor is implemented in a 110nm BSI process and achieves a small pixel pitch of 32mm with a fill factor of 33%. It consumes 29.1mW, while operating at 30fps. It achieves a high PDP of 14.3% at 850nm and a depth uncertainty of 7cm at a depth range of 70m, corresponding to the worst-case depth uncertainty of 0.1%. These results are achieved by the use of a compact SPAD front-end, a push-pull analog counter, and an optimized PDP. The gain mismatch errors in the analog counter are mitigated by the use of a push-pull gain averaging scheme.

Session T10: Emerging Non-Volatile Memories - RRAM, FeRAM, PCM, MRAM-2

8:00 AM, Tapa 3

Co-Chairs: Gary Bronner, Rambus
Byoung Hun Lee, Pohang University of Science and Technology

8:00 AM

T10.1 A Novel Phase Change Material RF Switch with 16nm Technology to Achieve Low Voltage and Low Ron*Coff for mmWave, Hung-Ju Li[1], K.P. Chang[1], C.E. Chen[1], W.T. Hsieh[1], H.H. Kuo[1], C.C. Huang[1], H.C. Chen[1], Z.H. Ya[1], H.Y. Chen[1], J.D. Jin[1], S.H. Yang[1], Y.W. Ting[1], K.C. Tseng[1], K.C. Huang[1], Harry Chuang[1] [1]TSMC, Taiwan

We present an enhanced phase change material (PCMe) RF switch (RFS) to achieve an impressive Ron*Coff of 11.6fs and operates below 1.8V. The PCMe material has low-resistivity that exhibits 40% insertion loss (IL) improvement compared to Ge50Te50, which is greater than -0.5dB, and isolation (ISO) less than -28dB at 30GHz. The switch operates 100 million cycles at -40C and 125C with stable Ron, and the transistor underneath is unaffected after RESET/SET 10Mc operations.

8:25 AM

T10.2 14nm FinFET node embedded MRAM technology for automotive non-volatile RAM applications with endurance over 1E12-cycles, Joosung Oh[1], Jaehyeon Park[1], Kiseok Suh[1], Kangmoon Lee[1], Sohee Hwang[1], Myeongjun Bak[1], Honghyun Kim[1], Baeseong Kwon[1], DongKyu Lee[1], Minkwan Kim[1], Seungmo Noh[1], Jongmin Lee[1], Soomin Cho[1], Gyuseong Kang[1], Hyun-Jin Shin[1], Yongsung Ji[1], Atsushi Okada[2], Ung-Hwan Pi[1], Kwangseok Kim[2], Younghyun Kim[1], Jeong-Heon Park[1], Seungpil Ko[1], Tae-Young Lee[1], Kyung-Tae

Nam[1], Minkwon Cho[1], Boyoung Seo[1], Shinhee Han[1], Yoonjong Song[1], Kangho Lee[1], Ja-Hum Ku[1] [1]Samsung Electronics Co., Ltd., [2]Samsung Advanced Institute of Technology
We present a 14nm FinFET embedded MRAM (eMRAM) technology for non-volatile RAM (nvRAM) applications, featuring endurance of 1E12 cycles, 100ns write speed, 150°C retention for 10 years, and macro density of 18Mb/mm^2. With SRAM interface, this macro provides write speed 24 times faster than flash-type eMRAM and ~50% area saving compared to SRAM. Compared to 28nm nvRAM-type eMRAM, we have improved retention temperature from 89°C to 150°C at the same endurance characteristics, which is suitable for automotive-grade products.

8:50 AM
T10.3 Extremely scaled perpendicular SOT-MRAM array integration on 300mm wafer, Farrukh Qayyum Yasin[1], Alvaro Palomino[1], Ankit Kumar[1], Valerio Pica[1], Simon Van Beek[1], Giacomo Talmelli[1], Van Dai Nguyen[1], Stefan Cosemans[1], Davide Crotti[1], Kurt Wostyn[1], Gouri Sankar Kar[1], Sebastien Couet[1] [1]imec
We present a novel integration solution to prevent MTJ pillar damage due to patterning of SOT- MRAM devices, particularly when targeting the ultimate SOT track scaling. Substantial reduction of switching current with pulse widths down to 0.3ns is shown in single cell extremely scaled devices versus our baseline. We demonstrate, for the first time, the functionality of a perpendicular SOT-MRAM array on 300mm CMOS wafer, comprising of multiple 4kb sub-banks with variations in SOT track size and pitch at our baseline 63nm MTJ CD. Study of the 4kb sub-banks indicates the feasibility of device pitch scaling from a device-to-device gap of 216nm down to 99nm, leading to a 50% increase in the MTJ read window (median Rp to Rap) while obtaining remarkable tailing bits as low as 0.3% for W/CoFeB stack (Wβ SOT track with CoFeB free layer MTJ).

9:15 AM
T10.4 First demonstration of high retention energy barriers and 2 ns switching, using magnetic ordered-alloy-based STT MRAM devices, Matthias Gottwald[1], Guohan Hu[1], Philip Trouilloud[1], Laura Rehm[1], Christopher Safranski[1], Gukcheon Kim[1], Stephen Brown[1], John Bruley[1], Christopher D'Emic[1], Oki Gunawan[1], Hyunsung Jung[2], Christian Lavoie[1], Joonmyoung Lee[2], Jim Liang[1], Michael Robbins[1], Jonathan Sun[1], Pouya Hashemi[1], Daniel Worledge[1] [1]IBM, [2]Samsung
Magnetic ordered alloys with low moment and strong bulk perpendicular magnetic anisotropy (PMA) were successfully developed and integrated on CMOS substrates as a free layer material. Superior device properties including high H_c (> 8 kOe), high E_b (> 80 k_BT) and sub-5 ns switching were achieved simultaneously, overcoming the fundamental tradeoff between high E_b and high-speed switching in conventional CoFeB-based devices using interface anisotropy. We further demonstrated improved switching performance at pulse widths down to 2 ns and improved magnetic field sensitivity in these ordered alloy-based devices, compared to the best published results to date.

Session C19: 2.5/3D Die-to-Die Interfaces
8:00 AM, Honolulu 1

Co-Chairs: John Wuu, AMD
Koji Nii, TSMC Design Technology Japan, Inc.

8:00 AM
C19.1 An On-Chip Current-Sink-Free Adaptive-Timing Power Impedance Measurement (PIM) Unit for 3D-IC in 5nm FinFET Technology, Tsung-Che Lu[1], Chin-Ming Fu[1], Wei-Hsiang Wang[1], Fred Kuo[1], Chih-Hsien Chang[1], Kenny Hsieh[1], King-Ho Tam[1], Tze-Chiang Huang[1], Tom Chen[1], Mei Wong[1], Wei-Pin Changchien[1], Frank Lee[1] [1]TSMC

This work presents a power impedance measurement (PIM) architecture for the 3D-IC platform with high-performance computing (HPC) applications. Proposed current-sink-free architecture improves stimulus current capacity without area overhead. Another adaptive-timing scheme saves 50% testing time. The PIM IP has been fabricated in 5nm FinFET process with TSMC-SoIC® technology for characterization of an embedded ARM® core. Compared to state-of-the-art works, the 3.6-A stimulus current yields 116x improvement while the 0.006 mm^2 core area achieves 79% reduction.

8:25 AM

C19.2 Scalable Embedded Multi-Die Active Bridge (S-EMAB) Chips with Integrated LDOs for Low-Cost Programmable 2.5D/3.5D Packaging Technology, Wei Lu[1], Jie Zhang[2,2], Yi-Hui Wei[2], Hsu-Ming Hsiao[2], Sih-Han Li[2], Chao-Kai Hsu[2], Chih-Cheng Hsiao[2], Feng-Hsiang Lo[2], Shyh-Shyuan Sheu[2], Chin-Hung Wang[2], Wei-Chung Lo[2], Shih-Chieh Chang[2], Hung-Ming Chen[1], Kuan-Neng Chen[1], Po-Tsang Huang[1] [1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan, [2]Electronic and Optoelectronic System Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan

For realizing low-cost miniaturized 2.5D/3.5D integration, this paper presents scalable embedded multi-die active bridge (S-EMAB) chips with integrated LDOs to provide on-demand I/O routing capability and in-package voltage regulation among multiple dies or chiplets. Each S-EMAB chip is a programmable bridge and implemented by an I/O array and MUX I/Os to support various transmission interfaces. The data rate of I/O array are from 50Mbps to 1Gbps, and MUX I/Os can reach to 8Gbps. Moreover, the number of programmable I/O links can be scaled up by connecting multiple S-EMAB chips in a daisy chain without extra control pins. In addition to miniaturization, LDOs are further integrated in S-EMAB chips to eliminate external LDOs. The proposed work is a fast time-to-market, low-cost, flexible, and miniaturized 3.5D integration solution for various IoT applications.

8:50 AM

C19.3 A 32Gb/s 0.36pJ/bit 3nm Chiplet IO using 2.5D CoWoS Package with Real-Time and Per-Lane CDR and Bathtub Monitoring, John Ma[1], Junhui Gu[1], Jianmin Guo[1], Dongliang Liang[1], Michael Sorna[1], Hui Wang[1], Ken Chang[1] [1]Marvell Technology Group

This work presents a high density single-ended NRZ Chiplet IO in 3nm CMOS technology over 2.5D CoWoS interposer of up to 2mm trace length, with a total of 216 data lanes running simultaneously at 32Gb/s/wire. The 2mm channel insertion loss and crosstalk at Nyquist frequency are -2.4dB and -18.1dB respectively. The RX features a real-time per-lane CDR and bathtub monitor, enabling optimal sampling point adaptation as well as tracking of phase drift over voltage and temperature. With all lanes toggling, the PHY achieves 3.84T/mm beach front density while consuming 0.36pJ/bit. The worst lane measures 0.342UI opening at BER of 1e-12 and interpolated 0.331UI opening at BER of 1e-15 when running at 32Gb/s. 25Gb/s results are also presented as a low power option.

9:15 AM

C19.4 WITHDRAWN - **A Customizable Killo-core Processor Architecture by Reusable Chiplets with Low-latency High-flexibility Die-to-Die Interconnection**

Session C20: Processing for AI

8:00 AM, Honolulu 2

Co-Chairs: Sophia Shao, UC Berkeley
Vinayak Honkote, Intel Corp.

8:00 AM

C20.1 Dyamond: A 1T1C DRAM In-memory Computing Accelerator with Compact MAC-SIMD and Adaptive Column Addition Dataflow, Seongyon Hong[1], Wooyoung Jo[1], Sangjin Kim[1], Sangyeob Kim[1], Kyomin Sohn[2], Hoi-Jun Yoo[1] [1]KAIST, [2]Samsung Electronics
This paper proposes Dyamond, a 1T1C DRAM in-memory computing accelerator with column addition (CA) dataflow, for high density and energy efficiency. LSB-CA minimizes ADC readouts to increase energy efficiency. MSB-CA with signal-enhanced MAC and signal-shifted ADC enhances SQNR, improving energy efficiency. A switchable sense amplifier reduces read energy for low-power in-memory arithmetic SIMD. Dyamond is fabricated in 28nm CMOS technology, integrating 27Mb eDRAM memory within a 6.48mm2 die area. It achieves 27.2 TOP/W peak energy efficiency and outstanding performance in advanced models (ResNet, BERT, GPT2).

8:25 AM
C20.2 A PVT Robust Signed 8-Bit Analog Compute-In-Memory Accelerator with Integrated Activation Functions for AI Applications, Hechen Wang[1], Renzhi Liu[1], Richard Dorrance[1], Deepak Dasalukunte[2], Niranjan Gowda[1], Brent Carlton[1] [1]Intel Labs, [2]Intel
The frequent data conversion in analog CiM reduces the benefits obtained by analog computing. This paper proposes a signed 8b MAC with hybrid differential capacitor ladders. Then a sparsity-aware DAC and an embedded SAR-ADC are introduced to lower the data conversion overhead. Finally, two activation functions (AFs) are included to further improve efficiency: 1) ReLU is realized by SAR-ADC LSB skipping; 2) tanh is built with analog buffers to bypass data converters.

8:50 AM
C20.3 A 22nm Nonvolatile AI-Edge Processor with 21.4TFLOPS/W using 47.25Mb Lossless-Compressed-Computing STT-MRAM Near-Memory-Compute Macro, De-Qi You[1], Win-San Khwa[2], Jui-Jen Wu[2], Chuan-Jia Chang[1], Guan-Yi Lin[1], Po-Jung Chen[1], Ting-Chien Chiu[1], Fang-Yi Chen[1], Andrew Lee[1], Yu-Cheng Hung[1], Chung-Chuan Lo[1], Ren-Shuo Liu[1], Chih-Cheng Hsieh[1], Kea-Tiong Tang[1], Yu-Der Chih[2], Tsung-Yung Chang[2], Meng-Fan Chang[2] [1]National Tsing Hua University, [2]TSMC
Battery-powered AI-edge processors require short wakeup-to-response latency (T_{WR}) and high energy efficiency (EF) for accurate real-time inference. This necessitates high-capacity nvCIM macros to store floating-point (FP) neural network (NN) data (e.g., BF16) and perform MAC operations with short latency (T_{CD}) and high EF. This paper presents an STT-MRAM nvCIM macro with lossless compression computation, a near-far aware readout scheme, and system-level CIM-friendly hybrid weight mapping. The proposed 22nm nonvolatile processor (nvProcessor) with 47.25-Mb STT-MRAM nvCIM achieved high EF (21.4TFLOPS/W), short T_{WR} (428.58μs), and high macro-level EF (27.6TFLOPS/W).

9:15 AM
C20.4 A Δ Based Spike Sorting SoC with End-to-End Implementation of Event-Driven Binary Autoencoder Neural Network in Analog CIM Achieving 94.54% Accuracy and 3.11μW/Ch, Edward Jongyoon Choi*[1], Vincent Lukito*[1], Injun Choi[1], Seoyoung Lee[1], Ik-Joon Chang[2], Sohmyung Ha[3] Minkyu Je[1]
[1]Korea Advanced Institute of Science and Technology, [2]Kyung Hee University, [3]New York University
This work presents a Δ-based spike sorting SoC with 3 main key features. 1) Incorporate the first CIM implementation in spike sorting using an autoencoder neural network feature extraction to increase clustering accuracy but with low power and latency. 2) Utilize Δ-spikes to suppress the low-frequency noise of neural signals avoiding false detection and increase overall system accuracy. 3) Reduce digital data transmission rate by relocating the spike detection and feature extraction to the analog domain using analog Δ detection and analog CIM. The proposed system achieves the highest measured on-chip spike sorting classification accuracy of 94.54% and reduced digital data transmission rate by 48.8× on average compare to prior spike sorting systems.

Thursday Luncheon Presentation
12:15 PM – 1:15 p.m., Coral 4-5

"The CHIPS Program and you: An R&D update for the VLSI Symposia", Greg Yeric, Director of Research, CHIPS National Semiconductor Technology Center Program, US Department of Commerce

The U.S. CHIPS and Science act allocated $50B for the advancement of semiconductor technology, which includes manufacturing incentives, R&D programs, and workforce development. Initial announcements have primarily involved the $39B directed toward manufacturing incentives. But now, just in time for the VLSI Symposia, R&D programs that align with the Symposia's membership are rolling out: the National Advanced Packaging Manufacturing Program (NAPMP) and the National Semiconductor Technology Center (NSTC), related workforce development initiatives, and additional programs. Dr. Yeric will describe the organization, strategy, and vision of the CHIPS R&D programs and discuss how the Symposia membership, including non-U.S. entities, can expect to participate as these R&D programs fully ramp up.

Session C21: Power Converters
8:00 AM, Honolulu 3

Co-Chairs: Zeynep Toprak Deniz, IBM
Kouichi Kanda, Fujitsu Research

8:00 AM
C21.1 A 96.4%-Efficiency Single-Duty-Cycled Buck-Boost Converter Achieving 1.9mV Ripple and 2.1mV Mode-Change Fluctuation for Mobile OLED Displays, Jae-Hyun Kim[1], Yousung Park[1], Doyoung Kwon[1], Dong-Kyu Kim[2], Sung-Chun Park[2], Yongjae Lee[2], Jung-Bong Lee[2], Hyun-Sik Kim[1] [1]KAIST, [2]Samsung Display
This paper presents a single-duty-cycled buck-boost (SDC-BB) DC-DC converter for powering mobile OLEDs. Its features include a low output ripple and the ability to seamlessly cover all conversion ratios using a single duty-cycle (*D*), effectively suppressing output fluctuations during transitions between boost and buck modes. In its implementation, the flying capacitor is reused for the gate drives, thereby eliminating bootstrap overhead, and an adaptive ramp generator is incorporated to enhance immunity to TDMA noise. The chip fabricated in 0.18µm achieves output ripples of ≤1.9mV and a peak efficiency of 96.4%. It maintains output fluctuations within 2.1mV during transitions between buck and boost modes, ensuring flicker-free displays.

8:25 AM
C21.2 A 1.8V-Input 0.2-to-1.5V-Output 2.5A 930mA/mm^3 Always-Balanced Dual-Path Hybrid Buck Converter with Seamlessly All-VCR-Coverable Tri-Mode Operation, Dae-Hyeon Kim[1], Jeong-Hyun Cho[1], Hyunki Han[1], Hyun-Sik Kim[1] [1]KAIST
This paper presents an always-balanced dual-path hybrid buck converter capable of covering all conversion ratios with high efficiency. The proposed tri-mode operations ensure seamless, defect-free dynamic voltage scaling (DVS). Fabricated in 180nm, the chip outputs voltages ranging from 0.2 to 1.5V with a 1.8V input. It achieves a peak efficiency of 94.2%, even with compact-volume LC parts. Its current density was measured to be 930mA/mm^3 at 2.5A load current.

8:50 AM
C21.3 A 5.4V-Vin, 9.3A/mm^2 10MHz Buck IVR Chiplet in 55nm BCD Featuring Self-Timed Bootstrap and Same-Cycle ZVS Control, Harish Kumar Krishnamurthy[1], Sally Amin[1], Huong Do[1], Claudio Alvarez[1], Michael

J Hill[1], Kaladhar Radhakrishnan[1], Vivek De[1], Sheldon Weng[1], Krishnan Ravichandran[1], Jim Tschanz[1], Wilfred Gomes[1], Jonathan Douglas[1] [1]Intel Corporation
This paper presents a 5.4V-V_{in}, 0.6-1.8V V_{out}, 10MHz LDMOS-based buck IVR chiplet implemented in a 55nm BCD process featuring a self-timed bootstrap technique and same-cycle all-digital ZVS control to achieve 9.3A/mm^2 current density and 93.6% peak conversion efficiency, while meeting all reliability constraints. The IVR chip supports a maximum load current of 80A and occupies 8.6mm^2 die area.

9:15 AM
C21.4 730-790mA/mm^2 48V-to-1V Integrated Hybrid DC-DC Converters based on a Star-Delta Switching Network with 5x/8x Duty Expansion, Chen Kong Teh[1], Te Bi[1], Shuichi Ito[1], Takashi Kurihara[1]
[1]Toshiba Electronic Devices & Storage Corporation
We present two 48V-to-1V non-isolated dc-dc converters with up to 790mA/mm^2 current density and 88% peak efficiency, realized by a star-delta topology providing 5x and 8x duty expansion with only 3 and 4 Cfly, respectively.

Session T11: Advanced CMOS Devices and Technology-2
9:55 AM, Tapa 1

Co-Chairs: Yue Liang, nVidia
Kazuyuki Tomida, Rapidus Corp.

9:55 AM
T11.1 V_t Fine-Tuning in Multi-V_t Gate-All-Around Nanosheet nFETs using Rare-Earth Oxide-based Dipole-First Gate Stack Compatible with CFET Integration, Hiroaki Arimura[1], Hans Mertens[1], Jacopo Franco[1], Leo Lukose[1], Waleed Maqsood[1], Stephan Brus[1], Thomas Chiarella[1], Andrea Impagnatiello[1], Suvidyakumar Homkar[2], Vivek Koladi Mootheri[2], Chunhai Yin[2], Giuseppe Alessio Verni[2], Michael Givens[2], Lucas Petersen Barbosa Lima[1], Serge Biesemans[1], Naoto Horiguchi[1] [1]imec, [2]ASM
This work demonstrates a dipole-induced V_t fine-tuning on scaled Gate-All-Around (GAA) nanosheet (NS) nFETs (48 nm CPP, 16 nm L_g). Thanks to a novel Rare-Earth-Oxide (REO) as a moderate n-type dipole former, ~50 mV-step V_t modulation is demonstrated even in a drive-in-free dipole-first integration scheme. V_t shift-dependent slight mobility degradation is seen on long-channel planar RMG nFETs, however, improved D_{it} and PBTI max. V_{ov} confirmed the high-quality gate stack. On the scaled NS nFETs, REO dipole-first demonstrates a gradual V_t modulation with maintained V_t variability and device performance while outperforming LaO dipole-first and dipole-last multi-V_t options.

10:20 AM
T11.2 Replacement Metal Gate Process Extendible Beyond 2 nm Node with Superior Gate Conductivity, Naomi Yoshida[1], Ilanit Fisher[1], He Ren[1], Chi-Chou Lin[1], Chenfei Shen[1], Yongjing Lin[1], Yi Xu[1], Michael S-.C. Chen[1], Mehul Naik[1] [1]Applied Materials
This paper describes a selective metal cap process on replacement-metal-gate (RMG) for gate scaling with high conductivity. Thin highly conductive metal cap on top of RMG is an effective way to maintain high gate conductivity with extremely scaled gate trench. The technology is extendible to 2 nm node GAA-FET and beyond.

10:45 AM
T11.3 Breakthrough processes for Si CMOS devices with BEOL compatibility for 3D sequential integrated More than Moore analog applications, Daphnée Bosch[1], Abygael Viey[1], Tadeu MOTA FRUCTUOSO[1], Pierre LHERITIER[1], Christophe LICITRA[1], Nada Zerhouni ABDOU[1], Antoine ALBOUY[1], Laurent

BRUNET[1], Alexandre MAGALHAES-LUCAS[1], Lucas MOTA BARBOSA DA SILVA[2], Hervé BOUTRY[1], Mohamed Husien Fahmy Taha Abdelrahman[1,3], Fuccio CRISTIANO[3], Remy GASSILLOUD[1], Michael RIBOTTA[1], Giovanni ROMANO[1], William VANDENDAELE[1], veronique BENEVENT[1], Mathieu OPPRECHT[1], Sebastien KERDILES[1], Frederic MILESI[1], Frederic MAZEN[1], Benoit SKLENARD[1], Catherine EUVRAT-COLNAT[1], Julien STURM[1], Amelie LAMBERT[1], cecile CANDEGABE[1], Lucie LARAIGNOU[1], Francois BOULARD[1], Aurelien SARRAZIN[1], Michelly DE SOUZA[2], Christoforos THEODOROU[4], Xavier GARROS[1], Perrine BATUDE[1] [1]Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France, [2]FEI, São Bernardo do Campo, Brazil, [3]LAAS, CNRS and University Toulouse, France, [4]Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, CNRS, Grenoble INP, CROMA, Grenoble

This work unlocks Low Temperature (LT) technological showstoppers in view of versatile analog high voltage (>2.5V) BEOL (400°C) devices. We demonstrated Silicon (Si) devices with CMOS-compatible poly gate thanks to ns laser annealing (NLA) in melt regime and junction dopants activation without diffusion at 400°C to preserve the engineered junction profile. HPD_2 final anneal cures LT gate stack, achieving performances in line with planar analog CMOS technology: D_{it} <1e11 $cm^2.eV^{-1}$, N_t <1e17 $eV^{-1}.cm^{-3}$ μ_{pMOS} >100$cm^2.V^{-1}.s^{-1}$ μ_{nMOS} >300$cm^2.V^{-1}.s^{-1}$.

11:10 AM

T11.4 First Experimental Demonstration of Self-aligned Flip FET (FFET): a Breakthrough Stacked Transistor Technology with 2.5T Design, Dual-side Active and Interconnects, Haoran Lu[1], Yandong Ge[1], Xun Jiang[1], Jiacheng Sun[1], Wanyue Peng[1], Rui Guo[1], Ming Li[1], Yibo Lin[1], Runsheng Wang[1], Heng Wu*[1], Ru Huang[1] [1]School of Integrated Circuits, Peking University, Beijing, China

For the first time, the Flip FET (FFET), a novel stacked transistor technology with self-aligned active and interconnects on both sides of wafer, is proposed and experimentally demonstrated. Two layers of transistors are formed on the same active and back-to-back stacked, featuring a much more manufacturing-friendly process flow. Standard cell libraries with minimum 2.5T design are established. FFET has better design flexibility with no restriction on N/P polarity for each transistor layer, enabling a bipolar SRAM with at least 35.9% over FinFET SRAM. Based on fins, FFET outperforms CFET with 21.5% higher frequency at iso-power and 45.0% lower power at iso-frequency. For nanosheet-based ones, FFET shows extra benefits over CFET with larger nanosheet width, with 14.5% higher frequency at iso-power. New concepts of dual-side interconnects are introduced and the P&R result of a RISCV32I core further validates the superiority of FFET with more than 31.3% area reduction compared with CFET.

11:35 AM

T11.5 3DIC with Stacked FinFET, Inter-level Metal, and Field-Size (25x33mm^2) Single-Crystalline Si on SiO_2 by Elevated-Epi, Bo-Jheng Shih[1,2], Yu-Ming Pan[1], Hao-Tung Chung[1], Chieh-Ling Lee[1], I-Chun Hsieh[1], Nein-Chih Lin[2], Chih-Chao Yang[2], Po-Tsang Huang[1], Hung-Ming Chen[1], Chiao-Yen Wang[1], Huan-Yu Chiu[1], Huang-Chung Cheng[1], Chang-Hong Shen[2], Wen-Fa Wu[2], Tuo-Hung Hou[2], Kuan-Neng Chen[1], Chenming Hu[1,3] [1]National Yang Ming Chiao Tung University, [2]Taiwan Semiconductor Research Institute, [3]Department of Electrical and Computer Science, University of California, Berkeley

The Elevated Epi technique is presented for the fabrication of single-crystal (100) silicon of wafer field size (25mmx33mm) for monolithic three-dimensional integrated circuits (3DICs). Elevated Epi uses a low substrate temperature, pulse laser technique to fabricate single-crystal Si on dielectric. We also demonstrate 3D inverters, with an inter-layer metal M0 positioned between two layers of FinFETs. A hybrid-3D cell library is presented for improving performance, power, and area of 3DICs.

Session T12: Oxide Channel FET for Logic and Memory Applications-2

9:55 AM, Tapa 2

Co-Chairs: Vamsi Paruchuri, ASM
Hiroshi Morioka, Socionext Inc.

9:55 AM

T12.1 Overcoming Performance Limitation of IGZO FET by iCVD Fluorine Doping, SEUNG HYUN OH[1], CHANG HYEON LEE[1], HEE TAE KIM[1], JEONG IK PARK[1], MIN JU KIM[2], SE JUN PARK[3], SUNG GAP IM[1], SUNG HAENG CHO[4], BYUNG JIN CHO[1] [1]KAIST, [2]Dankook University, [3]Samsung Electronics, [4]ETRI

It has been reported that fluorine (F) doping using initiated chemical vapor deposition (iCVD) doping technique can significantly improve electrical performance and reliability of IGZO channel FET. This new process can overcome the trade-off relationship between μ_{FE} and threshold voltage (V_{TH}), as IGZO FET with iCVD doping provides 2.5 times higher mobility than that without doping, yet maintains enhancement-mode (V_{TH}>0) operation. iCVD doping can achieve uniform distribution of F across the entire IGZO channel thickness, thereby successfully passivating interfaces, achieving excellent stability under electrical and illumination stresses.

10:20 AM

T12.2 Ge-doped In_2O_3: First Demonstration of Utilizing Ge as Oxygen Vacancy Consumer to Break the Mobility/Reliability Tradeoff for High Performance Oxide TFTs, Jiayi Wang[1,2], Ziheng Bai[2], Kuo Zhang[1,3], Zhicheng Wu[2], Di Geng[2], Yang Xu[1,2], Nannan You[1,2], Yuxuan Li[1,3], Guanhua Yang[2], Ling Li[2,3], Shengkai Wang[1,3], Ming Liu[2] [1]High-Frequency High-Voltage Device and Integrated Circuits R&D Center, Institute of Microelectronics, Chinese Academy of Sciences, [2]State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, [3]University of Chinese Academy of Sciences

For the first time, we demonstrated high-performance Ge-doped In_2O_3 (IGeO) thin film transistors (TFTs). Through comprehensive understanding of Ge-induced oxygen vacancy (V_O) consumption and crystallization mechanisms, the V_O generation is actively suppressed while increased the crystallinity. The proposed IGeO TFT with fractional Ge doping (atomic concentration ~0.4% by SIMS) presents an enhanced reliability (ΔV_{th} = 10 m V, +4 V for 3600 s) with high mobility (μ_{FE} = 62.7 $cm^2 V^{-1} s^{-1}$), which makes it a promising way to overcome the mobility/reliability tradeoff in In_2O_3-based TFTs.

10:45 AM

T12.3 First Demonstration of Monolithic Three-dimensional Integration of Ultra-high Density Hybrid IGZO/Si SRAM and IGZO 2T0C DRAM Achieving Record-low Latency (<10ns), Record-low Energy (<10fJ) of Data Transfer and Ultra-long data retention (>5000s), Menggan Liu[1,2], Zhi Li[1,2], Wendong Lu[1,2], Kaifei Chen[1,2], Jiebin Niu[1,2], Fuxi Liao[1,2], Zijing Wu[1,2], Congyan Lu[1], Weizeng Li[1], Di Geng[1], Nianduan Lu[1], Chunmeng Dou[1], Guanhua Yang[1], Ling Li[1], Ming Liu[1] [1]Laboratory of Microelectronic Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences(CAS), [2]University of Chinese Academy of Sciences

This work firstly demonstrates a monolithic 3D architecture with ultra-high density IGZO/Si SRAM and IGZO 2T0C DRAM (M3D-SD) integrated in 3-tiers. By incorporating ultra-low leakage IGZO transistor in tier 2 as pass gate and BEOL integration on Si-CMOS cross-coupled inverters (Tier 1), a hybrid IGZO/Si SRAM is demonstrated with ultra-high density of 4T footprint and 51% reduced static power. In addition, IGZO 2T0C DRAM is integrated in tier 3, which achieves SRAM-DRAM data transfer with record-low latency (<10ns) and energy (2.26fJ). The M3D-SD (with a minimum VDD of 0.35V) can successfully store the data to IGZO 2T0C DRAM and restore to the hybrid IGZO/Si SRAM after 5000s power off. This work provides a novel M3D platform to boost the memory hierarchy performance.

11:10 AM

T12.4 A Dual-Gate Vertical Channel IGZO Transistor for BEOL Stackable 3D Parallel Integration for Memory and Computing Applications, Ziyi Liu[1], Yiwei Du[1], Renrong Liang[1], Zhigang Zhang[1], Liyang Pan[1], Jianshi Tang[1], Bin Gao[1], Qi Hu[2], Jun Xu[1], He Qian[1], Huaqiang Wu[1], Yuegang Zhang[3,4] [1]School of Integrated Circuits, ICFC, BNRist, Tsinghua University, Beijing, China., [2]Beijing Superstring Academy of Memory Technology, Beijing, China, [3]State Key Laboratory of Low Dimensional Quantum Physics and Department of Physics, Tsinghua University, Beijing, China., [4]Frontier Science Center for Quantum Information, Beijing, China.

In this work, we demonstrate a stackable vertical single/dual-gate(SG/DG) C-shaped-channel field-effect transistor (VCCFET) based on atomic layer deposition (ALD) In-Ga-Zn-O thin film. with an Ion/Ioff ratio over1.4×10^{11} and an on current of 21 μA/μm. And we firstly fabricate vertical dual-gate IGZO transistors, featuring Gate-All-Around Lateral Gate(LG) and Channel-All-Around Vertical Gate(VG). The dual gates can be biased simultaneously to enhance gate control ability, Or bias independently to random access and linearly adjustment threshold voltage(Vth). This makes the transistor broadly applicable of memory and computing. Also, this device has future prospect for BEOL(≤300°C) parallel 3D integration, where different layers of transistors can be formed concurrently with independent source/drain contacts. And the one-step channel formation approach, akin to 3DNAND, reduces lithography costs and eliminates device performance degradation induced by sequential integration. Keywords: Atomic layer deposition, IGZO, dual-gate, vertical channel, monolithic 3D integration.

11:35 AM

T12.5 Bit-cost-scalable 3D DRAM Architecture and Unit Cell First Demonstrated with Integrated Gate-around and Channel-around IGZO FETs, Feng-Min Lee[1], Po-Hao Tseng[1], Yu-Yu Lin[1], Yu-Hsuan Lin[1], Wei-Lung Weng[1], Nei-Chih Lin[2], Po-Jung Sung[2], Chien-Ting Wu[2], Chih-Chao Yang[2], Wen-Fa Wu[2], Chang-Hong Shen[2], Tuo-Hung Hou[2], Ming-Hsiu Lee[1], Kuang-Yeu Hsieh[1], Keh-Chung Wang[1], Chih-Yuan Lu[1] [1]Macronix International Co., Ltd., [2]Taiwan Semiconductor Research Inst.

Novel 3D DRAM architectures with 2T0C IGZO gain cell and bit-cost-scalable 3D array are proposed and demonstrated for the first time. The unit cell is composed of one gate-around (GA) FET and one channel-around (CA) FET to form 2T0C DRAM device, where the GA FET and CA FET serve as the write transistor and the read transistor, respectively. To verify 3D stacking architecture, we demonstrate the GA IGZO FET by top metal gate with IGZO channel structure, and the CA IGZO FET by bottom IGZO gate with IGZO channel. The integrated 3D DRAM memory cell shows excellent device characteristics with >180 second data retention time and endures >1000 second DC stress on the write and read transistors w/o memory window closure. The proposed BEoL 2T0C DRAM cell features small footprint, bit-cost scalable 3D array, fast write/read, and good reliability, which is promising for future high density DRAM applications.

Session JFS6: Memory-Centric Computing for LLM

9:55 AM, Tapa 3

Co-Chairs: Hsinyu Tsai, IBM
Kyomin Sohn, Samsung Electronics Co., Ltd.

9:55 AM

JFS6.1 State-Independent Low Resistance Drift SiSbTe Phase Change Memory for Analog In-Memory Computing Applications (Invited), HUAI-YU CHENG[1], Zhi-Lun Liu[1], Amlan Majumdar[2], Alexander Grun[1], Asit Ray[2], Jeff Su[1], Malte J. Rasch[2], Fabio Carta[2], Lynne Gignac[2], Christian Lavoie[2], Cheng-Wei Cheng[2], Matt BrightSky[2], Hsiang-Lan Lung[1] [1]Macronix International Co., Ltd., [2]IBM T. J. Watson Research Center

We developed a phase-change memory (PCM), with SiSbTe material, that showed state-independent resistance drift (v~0.04) at 65 °C over the entire analog conductance range. We evaluated this PCM for In

Memory Compute (IMC) applications simulating the performance of BERT model with the IBM Analog Hardware Acceleration Kit (AIHWKit). Drift and data retention are dependent on the amount of A-type dopant into SiSbTe materials. Finding a trade-off between the two is important to deliver a balanced material that can tackle IMC workload without losing in performance. The fabricated SiSbTe PCM devices maintain the BERT accuracy (<2% loss) for more than 7 days at 65 °C and pass the data retention at 85 °C/48hrs demonstrating a great balance between the two metrics.

10:20 AM

JFS6.2 Cost-effective LLM Accelerator Using Processing in Memory Technology (Invited), hyungdeok Lee[1], guhyun kim[1], dayeon yun[1], ilkon kim[1], yongkee kwon[1], Euicheol Lim[1] [1]SK Hynix

Large language model (LLM)-based services continue to improve their performance requires the system with both large memory capacity and high memory bandwidth. For the GPT-3 175 billion model to operate at a minimum, it requires 800GB of storage. In addition, from frequent memory access and limited data reuse also affects memory bandwidth. More powerful memory performance requirements, however, comes with significant costs increase. The expenses associated with operating the necessary equipment and services to handle these memory and bandwidth requirements are considerable.

SK hynix aims to solve this issue by introducing a Processing in memory (PIM) device and PIM based accelerator called AiM and AiMX, respectively. By exploiting true bank-level parallelism, AiM and AiMX is expected to enhance the performance of LLM-based services as a core component of disaggregated system and multi-head attention acceleration. Additionally, AiM also has a potential in on-device AI, in direction of both performance and energy consumption with low batch size and reducing off-chip data movement.

10:45 AM

JFS6.3 An Ultra-low Voltage Auger-Recombination Enhanced Hot Hole Injection Scheme in Implementing a 3 Bits per Cell e-DRAM CIM Macro for Inference Accelerator, T. C. Kao[1], M. J. Huang[1], Y. R. Liu[1], Y. K. Wang[1], J. C. Guo[1], Steve Chung[1] [1]National Yang Ming Chiao Tung University

This work proposed a 3 bits per cell e-DRAM Compute-In-Memory (CIM) macro. The programming mechanism is based on Auger-recombination enhanced hot hole injection (AREHHI). Unlike conventional SRAM and DRAM architectures, it was designed on the high-performance Logic FinFET platform without an extra mask. The unit cell was based on three identical transistors, two serving as 1T1C DRAM and the other as computing component. Taking advantage of high linearity and low variability, a 2kb CIM Macro with untra-small cell size (0.192 μm^2) demonstrated high-speed operation (110MHz), significantly lower programming voltage (0.8V-1.4V), and high endurance, supporting multi-bit operation. Furthermore, we successfully employed AI inference algorithms to validate the CIM architecture, achieving a test accuracy of 90.07% and an energy efficiency of 56.9 TOPS/W. Overall, this CIM architecture provides an ideal and reliable solution for AI inference in IoT applications.

11:10 AM

JFS6.4 A 41.7TOPS/W@INT8 Computing-in-Memory Processor with Zig-Zag Backbone-Systolic CIM and Block/Self-Gating CAM for NN/Recommendation Applications, Zhuoyu Dai[1], Shengzhe Yan[1], Zhaori Cong[1], Zeyu Guo[1], Yifan He[2], Wenyu Sun[2], Chunmeng Dou[1], Feng Zhang[1], Jinshan Yue[1], Yongpan Liu[2], Ming Liu[1] [1]Institute of Microelectronics of the Chinese Academy of Sciences, [2]Tsinghua University

This work presents an energy-efficient CIM-CAM processor for both neural network (NN) and recommendation system (RecSys) applications. The main contributions include: **1)** A reconfigurable Zig-Zag memory access architecture for diverse convolution/MVM to minimize SRAM access; **2)** A backbone-

systolic CIM array towards a higher system/macro efficiency ratio; **3)** A distribution-aware block/self-gating (DABG) CAM to reduce both off-chip access and on-chip search power for the memory-dominate embedding layer. The fabricated 28nm chip demonstrates 37.9-81.5TOPS/W system energy efficiency for NN and 12.3-56.1nJ/request for RecSys. This work achieves 2.4×/3.6× energy/area efficiency for NN and 370× energy reduction for RecSys compared with the state-of-the-art.

11:35 AM

JFS6.5 Monolithic 3D Integration of Analog RRAM-based Fully Weight Stationary and Novel CFET 2T0C-based Partially Weight Stationary for Accelerating Transformer, H. Yang[1], Y. Li[1], J. Tang[1], R. An[1], Y. Zhang[1], L. Gao[2], N. Gao[2], H. Xu[2,3], Y. Du[1], Z. Liu[1], X. Ma[4], G. Wang[4], C. Zhao[4], J. Xiang[4], J. Zhao[5], W. Bu[6], K. Zheng[6], J. Kang[6], B. Gao[1], H. Qian[1], H. Wu[1] [1]School of Integrated Circuits, Tsinghua University, [2]BICIC, Beijing, China, [3]ICTFE, PKU, Taiyuan, China, [4]SAMT, Beijing, China, [5]DPI, Tsinghua University, [6]STIC, Beijing, China
To accelerate transformer with the crucial operation of linear projection and matrix multiplication, we present the M3D-SFP chip, a **m**onolithic **3D** integration of **S**i-CMOS logic with an analog resistive random-access memory (RRAM)-based fully weight stationary (**F**WS) for linear projections with a weight matrix fixed to capitalize on its highly efficient matrix-vector multiplication (MVM), complementary FET (CFET) 2T0C-based partially weight stationary (**P**WS) for data buffer and attention mechanisms with dynamic matrixes to utilize its easy writing. The novel CFET 2T0C is designed to output a digital voltage, instead of current, enabling CMOS logic compatibility for CIM, without increasing area due to the stacked nature of CFET N/P. Futhermore, the functional integrity of the M3D-SFP chip is corroborated by electrical tests with fabricated 128 k-bit RRAM array and CFET 2T0C macro with 164 transistors, while performance benchmark reveals a 12.9× speed-up over its 2D counterparts.

Session C22: Wireline Circuits II

9:55 AM, Honolulu 1

Co-Chairs: Trevor Caldwell, Alphawave Semi
Hisakatsu Yamaguchi, Fujitsu Ltd.

9:55 AM

C22.1 A 256Gbps Microring-based WDM Transceiver with Error-free Wide Temperature Operation for Co-packaged Optical I/O Chiplets, Pavan Bhargava[1], Daniel Jeong[1], Eric Jan[1], Derek Van Orden[1], Derek Kita[1], Hayk Gevorgyan[1], Sidney Buchbinder[1], Anatoly Khilo[1], Woorham Bae[1], Sung-Jin Kim[1], John Fini[1], Norman Chan[1], Chen Sun[1] [1]Ayar Labs
We present a 256Gbps WDM transceiver macro for use in co-packaged AI scale-out interconnects. The macro adopts a 8λ×32Gbps configuration to achieve 256Gbps per fiber. The transceiver macro operates error-free across a dynamic temperature ramp of 50-110°C, has >4dB optical link margin with 4dBm/λ input laser power, and consumes 3.45pJ/b (TX+RX). All transmit, receive, thermal control, and optical components are monolithically integrated in a 45nm SOI process. An optical I/O chiplet with 8 WDM transceiver macros achieves <1e-15 BER without FEC across 90 hours of operation in a 4Tbps duplex link configuration.

10:20 AM

C22.2 A 48-Gb/s Half-Rate PAM4 Optical Receiver with 0.27-pJ/bit TIA Efficiency, 1.28-pJ/bit RX Efficiency, and 0.06-mm^2 area in 28-nm CMOS, Chongyun Zhang[1], Li Wang[1], Zilu Liiu[1], Fuzhan Chen[1,2], Quan Pan[2], Xianbo Li[3], C. Patrick Yue[1] [1]ECE Department, The Hong Kong University of Science and Technology, [2]School of Microelectronics, Southern University of Science and Technology, [3]School of Electronics and Information Technology, Sun Yat-sen University

This work presents a 48 Gb/s PAM4 optical receiver with TIA and sampler integrated. The proposed TIA employs transadmittance transimpedance (TAS-TIS) structure to replace conventional CML-based VGA and post-amplifier, eliminating CTLE and inductive peaking while preserving the linearity and the gain-bandwidth product for PAM4 operation. The sampler includes a 2-tap FFE and a 2-tap DFE to compensate for ISI of the TIA and to recover data. Timing criteria of DFE loop is achieved up to 30 GBaud by optimizing the clock-to-Q delay of slicers. The RX is implemented in 28 nm CMOS process and wirebonded to a commercial photodiode. Optical measurement results at 48 Gb/s PAM4 show the RX consumes 61.4 mW with -5.1 dBm sensitivity at 2.4e-4 BER, and the TIA only contributes 13.1 mW, resulting in 1.28 pJ/bit (0.27 pJ/bit for TIA only) efficiency.

10:45 AM

C22.3 A 20Gb/s/pin Single-Ended PAM-4 Transceiver with Pre/Post-Channel Switching Jitter Compensation and DQS-Driven Biasing for Low-Power Memory Interfaces, Kyunghwan Min[1], Jahoon Jin[1], Soo-Min Lee[1], Sodam Ju[1], Jisu Yook[1], Jihoon Lee[1], Yunji Hong[1], Sung-Sik Park[1], Sang-Ho Kim[1], Jongwoo Lee[1], Hyungjong Ko[1] [1]Samsung Electronics

This paper presents a 20Gb/s/pin single-ended PAM-4 transceiver with advanced switching jitter compensation (SWJC) technique. The SWJC operates independently of equalization, hence further improving timing margin from 0.26UI to 0.39UI at a 1e-12 BER. The proposed pre-channel SWJC at a transmitter side minimizes switching jitter (SWJ) of middle eye, modulating the transitions of top and bottom eyes in a beneficial way for SWJC at a receiver side. Ultimately, along with the proposed SWJC technique, the timing margins improved by SWJC at a receiver side are further increased, having overheads only 1.6% in power and 0.22% in area.

11:10 AM

C22.4 A 2 X 112 Gb/s 0.34 pJ/b/lane Single-Ended PAM4 Receiver with Multi-Order Crosstalk Cancellation and Signal Reutilization Technique in 28-nm CMOS, Liping Zhong[1,2], Yangyi Zhang[1], Xiongshi Luo[1], Hongzhi Wu[1,2,2], Xuxu Cheng[1], Weitao Wu[1], Zhenghao Li[1], Quan Pan[1] [1]Southern University of Science and Technology, [2]southern university of science and technology

This paper presents a 2×112 Gb/s single-ended PAM4 receiver (RX) with multi-order crosstalk cancellation and signal reutilization (MO-XTCR) technique in 28-nm CMOS. An Nth-order far-end crosstalk (FEXT) model is proposed to accurately reveal the intricate FEXT behavior. Based on this model, the MO-XTCR technique is proposed to minimize the residual FEXT and boost signal reutilization ability. The proposed RX achieves the horizontal and vertical eye-openings of 53% and 40% for 56 Gb/s NRZ, and 24% and 18% for 112 Gb/s PAM4, respectively. This work achieves the best energy efficiency of 0.34 pJ/b/lane compared with state-of-the-art XTC schemes.

11:35 AM

C22.5 A 4.6pJ/b 64Gb/s Transceiver Enabling PCIe 6.0 and CXL 3.0 in Intel 3 CMOS Technology, Dong-Myung Choi[1], Yikui Dong[1,1], Roan Nicholson[1], Frank Liu[1], Wenyan Jia[1], Vadim Levin[1], Mike He[1], Sameer Pradhan[1], Jieqiong Du[1], Michael De Vita[1], Amanda Tran[1], Reza Navid[1], Sitaraman Iyer[1], Rui Song[1] [1]Intel Corporation

A voltage mode transmitter with 4-tap FIR filter and analog-mixed signal receiver employing 16-tap DFE are presented to enable PCI Express (PCIe) 6.0 and Compute Express Link (CXL) 3.0. The transceiver is implemented in Intel 3 CMOS technology and delivers full spec. compliance with 4.6pJ/b power efficiency.

Session C23: Neural Recording Interfaces

9:45 AM, Honolulu 2

Co-Chairs: Phillip Nadeau, Analog Devices
Chun-Huat Heng, National University of Singapore

9:45 AM

C23.1 SPIRIT: A Seizure Prediction SoC with a 17.2nJ/cls Unsupervised Online-Learning Classifier and Zoom Analog Frontends, Adelson Chua[1], Aviral Pandey[1], Ryan Kaveh[1], Sina Faraji Alamouti[1], Justin Doong[1], Rikky Muller[1] [1]University of California, Berkeley

This work presents SPIRIT, an SoC integrating an unsupervised online-learning seizure prediction classifier with eight 14.4µW, 0.057mm^2, 90.5dB dynamic range, Zoom Analog Frontends. SPIRIT achieves, on average, 97.5%/96.2% sensitivity/specificity, predicting seizures an average of 8.4 minutes before they occur. Its classifier consumes 17.2µW and occupies 0.14mm^2, the lowest reported for a prediction classifier by >134x in power and >5x in area.

10:10 AM

C23.2 A Highly-Integrated 1536-Channel Quad-Shank Monolithic Neural Probe in 55nm CMOS for Full-Band Raw-Signal Recording, Xiaolin Yang[1], Joan Aymerich[1], Philippe Coppejans[1], Wen-Yang Hsu[1], Chutham Sawigun[1], Jose Cisneros-Fernández[1], Andrea Lodi[1], Maribel Caceres Rivera[1], Bernardo Tacca[1], Matt McDonald[1], Hasan Mahmud-Ul[1], Barun Dutta[1], Jan Putzeys[1], Carolina Mora Lopez[1] [1]imec

We present a highly integrated neural probe for in vivo recordings, boasting a record of 1536 channels and 5120 TiN electrodes. The probe is optimally engineered with integrated capless LDOs and a low-power LVDS transmitter for energy-efficient data transfer, achieving a high level of integration and minimizing the number of external components. Innovative block-level optimization techniques result in a total area of 0.012mm2/ch, a total power of 19.34µW/ch, and the lowest total power-efficiency factor, while attaining excellent performance uniformity across channels. The probe is fabricated using a fab-compatible 300-mm post-CMOS process and fully validated in saline, demonstrating its ability to record full-band neural signals.

10:35 AM

C23.3 A 79.2dB-SNDR Slope-Adaptive Dynamic Zoom-and-Track Incremental ΔΣ Neural Recording Frontend with Resolution-Preservative 192mV/ms Transient Tracking, Sungjin Oh[1], Hyunsoo Song[1], Jose R. L. Ruiz[1], Wangbo Chen[1], Sung-Yun Park[1,2], Michael P. Flynn[1], Euisik Yoon[1] [1]University of Michigan, [2]Pusan National University

We present an incremental ΔΣ frontend that can resolve µV-level neural signals superimposed with large (>100mV) and fast (>100mV/ms) interferences without quality degradation. Unlike conventional approaches that stretch conversion range to accept the large input by sacrificing resolution, the proposed work tracks the large transient with constant high-resolution but variable tracking speed adaptive to its input slope. Thus, this frontend acquires neural information without quality loss even when exposed to large and fast artifacts that overwhelm small neural signals. With the proposed high-resolution tracking scheme, this work achieves the highest SNDR (79.2dB) and FoM_{SNDR} (165.7dB) among the state-of-the-art frontends using the conventional transient tracking techniques.

11:00 AM

C23.4 A 3072-Channel Neural Readout IC with Multiplexed Two-Step Incremental-SAR Conversion and Bulk-DAC-Based EDO Compensation in 22nm FDSOI, Xiaohua Huang[1,2], Xiaolin Yang[1], Andrea Lodi[1], Chris Van Hoof[1,2], Georges Gielen[1,2], Carolina Mora Lopez[1] [1]imec, [2]KU Leuven

We introduce a compact neural readout IC (ROIC) for high-resolution, large-scale µECoG arrays able to capture wideband brain-surface action potentials (APs). It efficiently records from 3072 electrodes via 96 time-multiplexed super-channels. The super-channels feature two-step incremental-SAR (I-SAR)

conversion and area-power-efficient bulk-DACs (BDACs) to handle multiplexed inputs and mitigate comparator and electrode DC offsets (EDOs). Fabricated in 22nm FDSOI, this prototype achieves the smallest effective per-channel area to date (0.0004mm2) and consumes 0.44μW, while maintaining a low full-band (1Hz-7.5kHz) input-referred noise (IRN) of 6.38μVrms. The ability to record multiplexed signals has been successfully demonstrated in saline.

11:25 AM

C23.5 A 16-Ch CMI-Tolerant Neural AFE with Inherent CM Detection and Shared CM Suppression Achieving 0.006mm^2/Ch and 3.1μW/Ch, Joan Aymerich[1], Chutham Sawigun[1], Jose Cisneros-Fernandez[1], Xiaolin Yang[1], Carolina Mora Lopez[1,2] [1]imec, [2]Imec

This work introduces a multichannel AFE for compact, low-power bidirectional neural interfaces, capable of tolerating common-mode interferences (CMIs) and capturing action potentials (APs) and local-field potentials (LFPs) with a 10kHz bandwidth (BW). By combining noiseless capacitive common-mode (CM) coupling and intrinsic OTA CM detection, our AFE achieves power- and area-efficient CM suppression (CMS) without input impedance (Zin) nor noise degradations. Our design allows sharing a single CMS loop across multiple channels, significantly reducing the total area and power. The fabricated proof-of-concept 16-ch AFE prototype tolerates 400mV$_{pp}$ CMIs, consumes 3.1μW/ch, and occupies 0.006mm^2/ch, thus achieving the best CMI-tolerance vs. area tradeoff. The CMS capability has been fully demonstrated in saline.

Session C24: High-Speed Data Converters

9:55 AM, Honolulu 3

Co-Chairs: Namik Kocaman, Broadcom
Hyunui Lee, Micron Technology

9:55 AM

C24.1 A 12-bit 16GS/s Single-channel RF-DAC with Hybrid Segmentation for Digital Back-off and Code-dependent Free Switch Driver achieving -85dBc IMD3 in 5nm FinFET, Byeongwoo Koo[1], Sunghan Do[1], Sangkyu Lee[1], Sangpil Nam[1], Heewook Shin[1], Saemin Im[1], Hyochul Shin[1], Sungno Lee[1], Junsang Park[1], Jungho Lee[1], Youngjae Cho[1], Michael Choi[1], Jongshin Shin[1] [1]Samsung Electronics

This work presents a single-channel 12-bit 16GS/s RF current steering DAC in a 5nm FinFET process. To achieve high dynamic performance without noise degradation, hybrid segmentation architecture is implemented with 0.0046mm2 small area. A novel pre-discharge switch drivers remove data dependency of switching without dynamic element matching (DEM) technique. The prototype DAC shows -85dBc IMD3 and -163dBFS/Hz noise spectral density. The power dissipation is 486mW at 16GS/s sampling with 7.1GHz output frequency.

10:20 AM

C24.2 A 16GS/s 10b Time-domain ADC using Pipelined-SAR TDC with Delay Variability Compensation and Background Calibration Achieving 153.8dB FoM in 4nm CMOS, Juzheng Liu[1], Ayman Shabra[2], Stacy Ho[2], Gabriele Manganaro[2], Mike Shuo-Wei Chen[1] [1]University of Southern California, [2]MediaTek

The paper presents a 16GS/s 10-bit direct-RF sampling time-domain ADC in 4nm. A background TDC delay variability calibration scheme and a bottom-plate sampling VTC are proposed. The ADC achieves a 44.48dB SNDR at Nyquist with 94.2mW power and 8000um^2 area, leading to a state-of-the-art 153.8dB FoM$_S$.

10:45 AM

C24.3 A 5nm 60GS/s 7b 64-way Time Interleaved Partial loop unrolled SAR ADC achieving 34dB SNDR up to 32GHz, Claudio Nani[1], Enrico Monaco[1], Nicola Ghittori[1], Alessandro Bosi[1], Domenico Albano[1], Claudio Asero[1], Nicola Codega[1], Alessio Di Pasquo[1], Ivan Fabiano[1], Marco Garampazzi[1], Fabio Giunco[1], Daniel Burgos[1], Gabriele Minoia[1], Paolo Rossi[1], Marco Sosio[1], Leonardo Vignoli[1], Enrico Temporiti[1], Shawn Scouten[2], Stephen Jantzi[3] [1]Marvell, Pavia, [2]Marvell, Ottawa, [3]Marvell, Irvine CA
We present a 60GS/s 7b 64-way Time Interleaved (TI) ADC with Analog Front End that features a non binary Partial Loop Unrolled (LU) SAR SubADC architecture which enables optimum comparator noise and power trade off. Comparator offsets among comparators of each SubADC are calibrated in background without analog hardware overhead by detecting patterns in the SAR output decisions. Fabricated in 5nm technology, the prototype AFE and ADC delivers 34.3dB SNDR till 32GHz and draws 109.3mW from 0.9V supply.

11:10 AM
C24.4 A 12-bit 10GS/s Time-Interleaved SAR ADC with Even/Odd Channel-Correlated Absolute Error-Based Over-Nyquist Timing-Skew Calibration in 5nm FinFET, Junsang Park[1], Jinwoo Park[1], Jaemin Hong[1], Sunjae Park[1], Dongsuk Lee[1], Sungno Lee[1], Hyochul Shin[1], Kyunghoon Lee[1], Byeongwoo Koo[1], Youngjae Cho[1], Michael Choi[1], Jongshin Shin[1] [1]Samsung Electronics
This paper presents an over-Nyquist 12-bit 10GS/s time-interleaved (TI) ADC with a background timing-skew calibration. An absolute error-based auto-correlation algorithm enables calibration of time skew for both the first and second Nyquist inputs, while an even and odd channel-based auto-correlation algorithm requires only three calibration steps. A prototype 10GS/s ADC in 5nm FinFET achieves a SNDR of 50.2dB and 46.2dB at input frequencies of 5GHz and 9GHz, respectively. The ADC consumes 386mW resulting in a FoMWalden and FoMSchreier of 146.0fJ/c-s. and 151.3dB, respectively.

11:35 AM
C24.5 A 10GS/s Hierarchical Time-Interleaved ADC for RF-sampling applications, Nereo Markulic[1], Johan Nguyen[1], Jorge Lagos Benites[1], Ewout Martens[1], Jan Craninckx[1] [1]imec
RF-sampling ADCs above 10GS/s enable modern instrumentation and wireless infrastructure applications. The key design challenge is to simultaneously guarantee high ENOB and high wide-band linearity, at moderate power. High ENOB requires large sampling capacitors for low kT/C noise, but they load the front-end buffer resulting in dynamic distortion at RF. Additionally, substantial power must be used for low-jitter clock distribution. The presented time-interleaved ADC addresses these challenges with innovation in (1) front-end and inter-level signal/clock distribution of a hierarchical converter, and (2) wideband-linear signal buffering, delivering higher ENOB than comparable systems [1-3], without the need for power consuming digital nonlinear distortion correction engines [1,3]. At only 350mW, the presented 10GS/s ADC delivers 9/8.2 ENOB at low/Nyquist frequencies with SFDR>60dB across 5-GHz BW.

Session T13: Technologies for Power & RF Applications
1:30 PM, Tapa 1

Co-Chairs: Srabanti Chowdhury, Stanford University
Mitsuru Takenaka, The University of Tokyo

1:30 PM
T13.1 71 GHz-fmax β-Ga2O3-on-SiC RF power MOSFETs with record Pout=3.1 W/mm and PAE=50.8% at 2 GHz, Pout= 2.3 W/mm at 4 GHz, and low microwave noise figure, Min Zhou[1], Hong Zhou[1], Mengwei Si[2], Guangjie Gao[1], Xiaojin Chen[1], Xiaoxiao Zhu[1], Kui Dang[1], Peijun Ma[1], Xiaohua Ma[1], Xuefeng Zheng[1], Zhihong Liu[1], Jincheng Zhang[1], Yuhao Zhang[3], Yue Hao[1] [1]Xidian University, [2]Shanghai Jiao Tong University, [3]Virginia Polytechnic Institute and State University

In this work, we demonstrate heavily-doped (8×10^{18} cm^{-3}) and gate-recessed β-Ga_2O_3 RF power MOSFETs integrated on a high thermal conductivity SiC substrate to minimize self-heating effect (SHE), high on-resistance (R_{on}) and short-channel effect (SCE). As a result, β-Ga_2O_3-on-SiC RF power FETs achieve a record maximum oscillation frequency (f_{max}) of 71 GHz, output power density (P_{out}) of 3.1 W/mm and power added efficiency (PAE) of 50.8% at frequency (f) of 2 GHz and P_{out}=2.3 W/mm at f=4 GHz. In addition, this work for the first time studies the microwave noise performance of the β-Ga_2O_3 RF MOSFET at f range of 2-18 GHz with low minimum-noise figure (NF_{min}) of 1.6 dB at f=4 GHz. Remarkably, we have provided an effective route of oxide RF transistors for future high-f, high-power and low-noise RF power applications.

1:55 PM

T13.2 Field Plate and Package Optimization for GaN Devices and Systems, Tz-Wun Wang[1], Sheng-Hsi Hung[1], Chien-Wei Cho[1], Po-Jui Chiu[1], Chi-Yu Chen[1], Ke-Horng Chen[1], Kuo-Lin Zheng[2], Chih-Chen Li[3] [1]EE, National Yang Ming Chiao Tung University, [2]Chip-GaN Power Semiconductor Corporation, [3]MediaTek, Hsinchu, Taiwan

This work demonstrates the 650V GaN field plate design and the optimized integrated circuit (IC) package. The source FP length is suggested to be longer but less than three times the split high FP. Longer 1ST FP and shorter Gap design enhance the Miller ratio and suppress ringing effect.

2:20 PM

T13.3 Hybrid Integration of 3D-RF Interconnects on AlGaN/GaN/Si HEMT RF Transistor featuring 2.2W/mm P_{sat} & 41% PAE @28GHz using a Robust and Cost-Effective Chiplet Heterogeneous Bonding Technique, Alexis Divay[1], Olivier Valorge[1], Christophe Dubarry[1], Mohammed Medbouhi[1,1], Rémi Franiatte[1], Daniel Mermin[1], Rémi Velard[1], Yveline Gobil[1], Fanny Morisot[1], Erwan Morvan[1], Ismaël Charlet[1], Luca Lucci[1], José Lugo[1], Xavier Garros[1] [1]CEA-Leti

This article presents electrical results of an effective heterogeneous 3D scenario for RF integrated systems: an AlGaN/GaN/Si HEMT is stacked on Si CPW and interconnected with copper pillars using a high-yield chiplet heterogeneous integration process. DC and RF measurements confirm the relevance of this efficient and pragmatic approach regarding electrical performances: copper pillar interconnects exhibit less than 0.2dB of insertion loss at 28GHz. However, measurements also confirm that the thermal dissipation of such an integrated system requires special attention in order to maintain valuable system performance.

2:45 PM

T13.4 Novel Material, Process and Device Innovations for Next Generation Silicon Carbide (SiC) Trench MOSFET Technology, Pratik B Vyas[1], Ludovico Megalini[1], Ashish Pal[1], Joshua Holt[1], Archana Kumar[1], Stephen Weeks[1], Charisse Zhao[1], Lucien Date[1], Hansel Lo[1], Michel Khoury[1], Safdar Muhammad[1], Fabian Piallat[1], Ricky Fang[1], William Charles[1], Pratim Palit[1], Jinghe Yang[1], Qintao Zhang[1], Jang Seok Oh[1], Bryan Turner[1], Samphy Hong[1], Aswin Prathap Pitchiya[1], Benjamin Briggs[1], Jiao Yang[1], Dae Yang[1], Fengshou Wang[1], Joseph Lee[1], Gopal Prabhu[1], Dustin Ho[1], Carlos Caballero[1], Durga Chaturvedula[1], Zheng Yuan[1], Yi Zheng[1], David A. Britz[1], Stephen Krause[1], Raghav Sreenivasan[1], Michael Chudzik[1], Subi Kengeri[1], Siddarth Krishnan[1], El Mehdi Bazizi[1] [1]Applied Materials Inc.

New material, process and device design innovations are proposed for next generation SiC trench MOSFET. Advanced patterning films (APF) are proposed as novel implant hardmask and high temperature capping material. Novel gate oxide formation processes are demonstrated for improved pattern fidelity & carrier mobility. A novel SiC transistor device design integrating channel counter-implant and pocket implant is proposed for significant mobility improvement without threshold voltage (VT) loss.

Session T14: Novel Devices for Quantum Computing Applications

1:30 PM, Tapa 2

Co-Chairs: Thanh Viet Dinh, NXP Semiconductors
Ryuta Tsuchiya, Hitachi Ltd.,

1:30 PM

T14.1 Concatenated Continuous Driving for Extending Lifetime of Spin Qubits towards a Scalable Silicon Quantum Computer, Takuma Kuno[1], Takeru Utsugi[1], Noriyuki Lee[1], Toshiyuki Mine[1], Itaru Yanagi[1], Satoshi Muraoka[1], Raisei Mizokuchi[2], Jun Yoneda[2], Tetsuo Kodera[2], Takashi Nakajima[3], Andrew Ramsay[4], Normann Mertig[4], Shinichi Saito[1], Digh Hisamoto[1], Ryuta Tsuchiya[5], Hiroyuki Mizuno[1] [1]Hitachi, Ltd., [2]Tokyo Institute of Technology, [3]RIKEN Center for Emergent Matter Science, [4]Hitachi Cambridge Laboratory, [5]Hitachi Ltd.

We demonstrate a technique for manipulating silicon spin qubits that will facilitate large-scale integration of quantum computers. We confirm spin manipulation and evaluate the coherence time of a silicon spin qubit. The qubit device is fabricated using fully-depleted-silicon-on-insulator (FDSOI) technology. This promises scalability to large qubit numbers, using commercial semiconductor technology. Furthermore, we demonstrate concatenated continuous driving (CCD) for spin qubits. This contributes to extending their coherence time. Specifically, we extend the coherence time of Rabi oscillation from 1.2 µs to over 200 µs. This result shows that spin qubits can be protected against inherent noise in the chip environment, including fluctuations of magnetic moments of ^{29}Si isotopes in natural Si. This is essential for realizing quantum computers in silicon.

1:55 PM

T14.2 Single-power-supply compatible cryogenic $In_{0.8}Ga_{0.2}As$ quantum-well HEMTs with record combination of high-frequency and low-noise performance for quantum-computing applications, Ji-Hoon Yoo[1], Yong-Soo Jeon[1], Seung-Woo Son[1], In-Geun Lee[1], Hyeon-Bhin Jo[1], Su-Min Choi[1], Min-Seo Yu[1], Wan-Soo Park[1], Hyo-Jin Kim[1], Hyeok-Jun Lee[1], Sang-Pyeong Son[1], Sang-Kuk Kim[2], Jacob Yun[2], Jae-phil Shim[3], Hyunchul Jang[3], Kiwon Lee[4], Yongsik Jeong[5], Ted Kim[2], Chan-Soo Shin[3], Tae-Woo Kim[6], Jae-Hak Lee[1], Kyunghoon Yang[5], Dae-Hyun Kim[1] [1]Kyungpook National University, [2]QSI, [3]KANC, [4]Wonkwang University, [5]KAIST, [6]Texax Tech University

We present L_g = 45 nm E-mode cryogenic $In_{0.8}Ga_{0.2}As$ quantum-well (QW) HEMTs with the record combination of high-frequency and low-noise characteristics. The fabricated devices exhibited a true E-mode operation, the best balance between f_T = 662 GHz and f_{max} = 653 GHz, and the lowest $\sqrt{I_D}/g_m$ = 0.176 at 4 K. Besides, we investigated the temperature-dependent behavior. Three-layer model indicated that the reduction of $\rho_{barrier}$ was critical to lower R_s at 4 K. According to the delay time analysis, the improvement of f_T was mainly due to the mitigation of the extrinsic channel charging delay, arising from the enhanced carrier transport at 4 K.

2:20 PM

T14.3 First Demonstration of Superconducting Nb Contact on Heavily-Doped Group IV Semiconductor, Gerui Zheng[1], Enze Zhang[1], Rami Khazaka[2], Kaizhen Han[1], Haiwen Xu[1], Yuxuan Wang[1], Hyunsoo Yang[1], Xiao Gong[1] [1]National University of Singapore, [2]ASM

We report the first demonstration of superconducting Nb contact on highly boron-doped $Si_{0.35}Ge_{0.65}$, achieving an ultra-low contact resistivity (ρ_c) of 5.22×10^{-10} Ω-cm^2 at 295 K on $Si_{0.35}Ge_{0.65}$ with active doping concentration (N_A) of 2.80×10^{21} cm^{-3}. We discover that the contact resistance (R_c) remains low from 295 K to 6 K, with only slight increase from 1.80×10^{-4} to 2.47×10^{-4} Ω-cm. However, the superconducting nature of the Nb film at 6 K enables the realization of 28% reduction in total resistance compared with the $Ti/Si_{0.35}Ge_{0.65}$ contact. Such property can be obtained with a process thermal budget up to 180 °C, demonstrating its quantum compatibility.

2:45 PM

T14.4 Photon-mediated charge transport and stability of physically-defined and self-organized germanium quantum dots/SON barriers in few-hole regime at T > 10 K, Chi-Cheng Lai[1], Yu-Wen Chiu[1], I-Hsiang Wang[1], Ting Tsai[1], Jhih-Wei Chen[2], Yen-Hsiang Wang[2], Mau-Chung Frank Chang[2], Horng-Chih Lin[1], Pei-Wen Li[1] [1]National Yang Ming Chiao Tung University, [2]University of California, Los Angeles, CA

We report for the first photon-mediated charge transport through physically-defined Ge double quantum-dots (DQDs)/Si barrier and QD/Si3N4 single-hole transistor in few-hole regime for high-fidelity qubit operation at T > 10 K. Engineering strengths of size-tunable QDs, self-organized barriers, and self-aligned reservoirs enable controllable tunability of charging energy, level spacing and coupling energy of Ge DQDs by adjusting QD size and barrier width/potential. Hard-wall confinement and photon enhanced carrier transport are facilitated to resolve charge states of DQDs, improve tunneling current properties of SHTs with high peak-to-valley ratio (~2000), low leakage (~5 fA), large addition energy (~50 meV), low 1/f noise (~10E-26 A2 /Hz), and achieve DQDSHT readout fidelity of 99.92% at T > 10 K.

Session C25: Digital Circuits

1:30 PM, Honolulu 1

Co-Chairs: Carlos Tokunaga, Intel Corporation
Makoto Miyamura, Toshiba Electronic Devices & Storage Corp.

1:30 PM

C25.1 A 5.6µW10-Keyword End-to-End Keyword Spotting System Using Passive-Averaging SAR ADC and Sign-Exponent-Only Layer Fusion with 92.7% Accuracy, Sungjin Park[1], Kwanghyun Shin[1], Dongkwon Lee[1], Minyoung Kang[1], Sunwoo Lee[1], Youngmin Park[1], Mingoo Seok[2], Dongsuk Jeon[1] [1]Seoul National University, [2]Colombia University

This paper presents a 10-keyword end-to-end keyword spotting system. Passive averaging effectively improves the analog front-end SNR with a small power overhead of 20nW. A sign-exponent-only layer fusion scheme reduces the model size and multiplication power overhead by 63.5% and 29.8%, respectively, maintaining the keyword spotting accuracy. Fabricated in 65nm CMOS, the design provides the highest accuracy of 92.7% and the lowest power consumption of 5.6µW compared to prior arts aimed at 10 keywords.

1:55 PM

C25.2 An Area-Efficient True Single-Phase Clocked and Conditional Capture Flip-Flop for Ultra-Low-Power Operations in 7nm Fin-FET Process, Hyunchul Hwang[1], Minsu Kim[1], Daeseong Lee[1], Yonggeol Kim[1], Byungsu Kim[1], Kunhyuk Kang[1] [1]Samsung Electronics

In this paper, we propose a new ultra low-power flip-flop circuit structure that supports true single phase clock operation and conditional capture characteristics. Simulation results based on 7nm Fin-FET process shows 63% power reduction while reducing cell area by 7%, compared to the conventional transmission-gate flip-flop. Silicon measure based on a test chip shows successful operation even at 0.33V, proving its structural robustness near sub-threshold region.

2:20 PM

C25.3 A Mixed-signal 3D Footstep Planning SoC for Motion Control of Humanoid Robots with Embedded Zero-Moment-Point based Gait Scheduler and Neural Inverse Kinematics, Qiankai Cao[1], Juin Chuen Oh[1], Jie Gu[1] [1]Northwestern University

This work presents a footstep planning SoC chip for humanoid robot. A time-domain graph search engine for 3D footstep planning and mixed-signal zero moment point (ZMP) gait scheduler with neural inverse

kinematics is developed for efficient robot motion control. A 65nm SoC chip is fabricated and demonstrated in-situ on a humanoid robot with the state-of-the-art search rate and energy efficiency for humanoid robot control and footstep planning.

2:45 PM

C25.4 A Jammer-Mitigating 267Mb/s 3.78mm² 583mW 32x8 Multi-User MIMO Receiver in 22FDX, Florian Bucheli[1], Oscar Castañeda[1], Gian Marti[1], Christoph Studer[1] [1]ETH Zurich

We present the first multi-user (MU) multiple-input multiple-output (MIMO) receiver ASIC that mitigates jamming attacks. The ASIC implements a recent nonlinear algorithm that performs joint jammer mitigation (via spatial filtering) and data detection (using a box prior on the data symbols). Our design supports 8 user equipments (UEs) and 32 basestation (BS) antennas, QPSK and 16-QAM with soft-outputs, and enables the mitigation of single-antenna barrage jammers *and* smart jammers. The fabricated 22nm FD-SOI ASIC includes preprocessing, has a core area of 3.78mm², achieves a throughput of 267Mb/s while consuming 583mW, and is the only existing design that enables reliable data detection under jamming attacks.

Session C26: Analog Techniques II

1:30 PM, Honolulu 2

Co-Chairs: Qinwen Fan, TU Delft
Tomohiro Nezuka, MIRISE Technologies Corp.

1:30 PM

C26.1 A Scalable mK Cryo-CMOS Demultiplexer Chip for Voltage Biasing and High-Speed Control of Silicon Qubit Gates, Sushil Subramanian[1], Todor M Mladenov[1], Simon Schaal[1], Bishnu Patra[1], Lester Lampert[1], Nancy K Robinson[1], Jeanette Roberts[1], Stefano Pellerano[1] [1]Intel Corporation

Large-scale silicon qubit control requires closer integration of control electronics to qubits at the mK stage of the dilution refrigerator to address the wiring bottleneck. We present a mK demultiplexer chip that uses only two input analog voltages and digital control signals, to provide both DC bias and high-speed voltage pulsing for up to 64 qubit terminals. Integrated with a foundry qubit chip on the same PCB and controlled by a 4 K cryo-CMOS controller, mK cryogenic measurements show multi-terminal characterization of a qubit device.

1:55 PM

C26.2 A 0.8V Capacitively-Biased BJT-Based Temperature Sensor with an Inaccuracy of ± 0.4°C (3σ) from -40°C to 125°C in 22nm CMOS, Zhong Tang[1], Haining Wang[1], Xiaopeng Yu[2], Kofi Makinwa[3], Nick Nianxiong Tan[1] [1]Vango Technologies, Inc, [2]Zhejiang University, [3]Delft University of Technology

The paper presents a compact sub-1V BJT-based temperature sensor for thermal management applications. Capacitively-biased PNPs driven by a regulated charge-pump generate PTAT and CTAT voltages that are readout by an energy and area efficient inverter-based ΣΔ ADC. Fabricated in 22nm CMOS, the sensor occupies 0.01mm² and consumes 2.9µW from a 0.8V supply. After a 1-point trim, it achieves an inaccuracy of ± 0.4 ˚C (3σ) from -40 ˚C to 125˚C, which is the best reported in sub-65nm CMOS, as well as high energy efficiency, resulting in a resolution FoM of 0.41pJ·K².

2:20 PM

C26.3 A 0.29pJ/step Fully Discrete-Time Charge Domain Bridge-to-Digital Converter for Force Sensing in Spinal Implants Using RC Bridge, Tim Keller[1], Rosario Incandela[1], Xi Chen[1], Hesam Ghiasi[1], Mohsen Khodaee[1], Sina Arjmandpour[1], Jiawei Liao[1], Long He[1], Tobias Goetschi[2], Jonas Widmer[2], Taekwang Jang[1]

[1]ETH Zurich, [2]Spine Biomechanics, Department of Orthopedic Surgery, Balgrist University Hospital, University of Zurich

This paper proposes a fully discrete-time charge domain bridge-todigital converter for implantable force sensing after a spinal fusion surgery. We propose an energy-efficient RC bridge to replace the quarter bridge, reducing power consumption. Further, the sampling capacitor in the bridge is reused in a series-parallel amplifier (SPA) and charge-injection successive approximation (CI-SAR) analog to digital converter, thus saving power consumption and reducing the noise. Implemented in 22nm CMOS, the proposed design achieved an SNR of 55.3dB while consuming 1.38 µW at 10ksps with the lowest reported FoM of 0.29pF/step and the smallest area of 0.07mm2.

2:45 PM

C26.4 A 0.72nW, 0.006mm^2 32kHz Crystal Oscillator with Adaptive Sub-Harmonic Pulse Injection from -40°C to 125°C in 22nm FDSOI, Yingjie Zhu[1], Yiqing Lan[1], Humiao Li[1], Haoran Lyu[1], Zhen Kong[1], Jian Zhao[2], Yida Li[1], Guoxing Wang[2], Jiamin Li[1], Longyang Lin[1] [1]Southern University of Science and Technology, [2]Shanghai jiao Tong University

A sub-nW, single-supply pulse-injection-based crystal oscillator(XO) that operates across a wide temperature range is presented. The valley-injection timing adaptation circuit achieves <±7% inaccuracy against PVT variations at 58.8pW. Moreover, the injection distortion compensation and oscillation DC stabilizing techniques achieve 7× lower peak-injection timing deviation. The IC in 22nm FDSOI achieves a 11ppb Allan deviation floor at 0.72nW and 0.006mm2, and enables the widest reported temperature range of -40°C to 125°C.

Session C27: Sensors and Displays

1:30 PM, Honolulu 3

Co-Chairs: Inhee Lee, University of Pittsburgh
Wangyeong Jung, KAIST

1:30 PM

C27.1 An OLED Display Driver IC Embedding -63dB CMR, 80mV/nA Sensitivity, 390pA Detectable, and Column-Parallel Pixel Current Readout for Real-Time Non-Uniformity Compensation, Gyu-Wan Lim[1], Gyeong-Gu Kang[1], Seunghwa Shin[1], Kihyun Kim[1], Yousung Park[1], Won Kim[2], Young-Bok Kim[2], Hyun-Kyu Jeon[2], Hyun-Sik Kim[1] [1]KAIST, [2]LX Semicon

This paper presents a display driver IC that embeds column-parallel 11b pixel-current readouts to compensate for display non-uniformity. Leveraging the source-driven TFT pixel, the proposed techniques facilitate real-time current sensing, even while the display is active. Fabricated in 180nm, the chip achieves a -63dB rejection to common noise, a 390pA/LSB resolution, and an 80mV/nA sensitivity. Demonstrations with real LEDs effectively validated the pixel current sensing.

1:55 PM

C27.2 A 92.8% Power Reduction Event-Driven Dual-Mode Touch Analog Front-End IC Featuring 620&[mu]W Self-Capacitance Sensing and 500fps Mutual-Capacitance Sensing, Jonghang Choi[1], Ingu Jeong[1], Seok-Won Jung[1], Jun-Eun Park[1] [1]Sungkyunkwan University

This paper presents an energy-efficient dual-mode touch- sensor analog front-end (AFE) IC that supports an event-driven operation. The proposed AFE consists of 1) an ultralow-power self-capacitance sensing (LP-SCS) and 2) a high-performance mutual-capacitance sensing (HP-MCS). Once the LP-SCS detects a touch input during a standby mode, the HP-MCS is triggered to start the mutual capacitance sensing with high SNR and high frame rate. The event-driven dual-mode sensing can reduce the AFE power

consumption up to 92.8%. The proposed AFE IC was fabricated in an 80nm CMOS process. The measured power consumptions are 0.62mW and 8.65mW for the LP-SCS and the HP-MCS, respectively. The measured SNRs of the LP-SCS and the HP-MCS are 52.6dB and 40.2dB with frame rate of 60Hz and 500Hz, respectively.

2:20 PM

C27.3 A 0.9-2.6pW 0.1-0.25V 22nm 2-bit Supply-to-Digital Converter Using Always-Activated Supply-Controlled Oscillator and Supply-Dependent-Activation Buffers for Bio-Fuel-Cell-Powered-and-Sensed Time-Stamped Bio-Recording, Hiroaki Kitaike[1], Masaharu Inada[1], Mitsuru Terauchi[1], Hironori Tagawa[1], Ryosuke Nagai[1], Shufan Xu[1], Ruilin Zhang[1], Kunyang Liu[1], Kiichi Niitsu[1] [1]Kyoto University

This paper presents a low-power supply-to-digital converter for bio-recording system where bio fuel cell provides both power and sensing data. It is achieved by supply-controlled oscillator, supply-dependent activation buffers (SDAB), and encoders. A 22-nm prototype chip exhibits its feasibility with a power of 0.9-2.6 pW under 0.1-0.25 V.

2:45 PM

C27.4 E-Textile Battery-Less Walking Step Counting System with <23 pW Power, Dual- Function Harvesting from Breathing, and No High-Voltage CMOS Process, Anil Kumar Gundu[1], Luigi Fassio[1], Massimo Alioto[1] [1]National University of Singapore

An e-textile walking step counting full system (smart Tshirt) is presented. Harvesting from co-designed low-voltage triboelectric nanogenerator (TENG) pushes over-voltage protection/rectification on chip. Conformability and minimal off-chip components are achieved via dual-function harvester/sensor reuse and battery/passive elimination. Always-on power reduction to pWs enables uninterrupted operation while solely powered by breathing harvesting.

Session T15: Non-Volatile Memory Technology - Hafnia Based Ferroelectrics-2

3:25 PM, Tapa 1

Co-Chairs: Karl Hofmann, Infineon Technologies
Kenji Tateiwa, TPSCo

3:25 PM

T15.1 Low-Damage Processed and High-Pressure Annealed High-κ Hafnium Zirconium Oxide Capacitors near Morphotropic Phase Boundary with Record-Low EOT of 2.4Å & high-κ of 70 for DRAM Technology, Venkateswarlu Gaddam[1], Junghyeon Hwang[1], Hunbeom Shin[1], Chaeheon Kim[1], Giuk Kim[1], Hyung-Jun Kim[2], Jooho Lee[2], Hyun-Cheol Kim[3], Bumsu Park[3], Suhwan Lim[3], Sang Yun Kim[3], Kwangsoo Kim[3], Sungho Lee[3], Daewon Ha[3], Jinho Ahn[4], Sanghun Jeon[1] [1]KAIST, [2]Samsung Advanced Institute of Technology, [3]Samsung Electronics, [4]Hanyang University

We present record-low equivalent oxide thickness (EOT) of 2.4 Å with a remarkable dielectric constant (κ) of 64 at 4.1nm-thick hafnium-based films with no wake-up characteristics. In comparison to conventional HZO films, our remarkable achievement stems from the high-quality crystalline structure with less oxygen vacancies formed by a low-damage process, as evidenced by high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) images and electron energy-loss spectroscopy (EELS) analysis. In addition, with high-pressure annealing (HPA), we were able to reduce the annealing temperature to 450°C leading to a decrease in leakage current (1.5 order). Further, increasing the measurement temperature from 298K to 389K results in the high-κ from 66 to 70, which is the theoretical limit of the κ value of t-phase.

3:50 PM

T15.2 Revealing Mechanism of Non-accumulative Disturb and Approach Toward Disturb Suppression in HZO/Si FeFET Memory, Masaki Otomo[1], Kasidit Toprasertpong[1], Zuocheng Cai[1], Zhenhong Liu[1], Mitsuru Takenaka[1], Shinichi Takagi[1] [1]The University of Tokyo

The mechanism of repeated read/write disturb in $Hf_{0.5}Zr_{0.5}O_2$ (HZO)/Si FeFETs is systematically studied. Disturb in FeFETs, found not to be a simple accumulation of repeated disturbs, is modeled with a combination of two mechanisms: trap dynamics and polarization dynamics. The amount of polarization reversed by disturb is evaluated to separate the two dynamics. We show that the suppression of disturb field in HZO due to de-trapping (trap dynamics model) and the relaxation of partially reversed polarization during the disturb interval (polarization dynamics model) are the two origins of the non-accumulative property of disturb, where each mechanism dominates in different disturb voltage and duration. We also show that the disturb behavior depends on the HZO thickness, and demonstrate a new approach to suppress disturb by applying substrate bias (V_{sub}) during disturb intervals.

4:15 PM

T15.3 BEOL Compatible Ultra-Low Operating Voltage (0.5 V) and Preconfigured Switching Polarization States in Effective 3 nm Ferroelectric HZO Capacitors, Minjong Lee[1], Jiyoung Kim[1], Jin-Hyun Kim[1], Dan N. Le[1], Seojun Lee[1], Si-Un Song[1], Rino Choi[2], Youngbae Ahn[3], Seung Wook Ryu[3], Pil-Ryung Cha[4], Chang-Yong Nam[5], Seongbin Park[6], Jongmug Kang[6], Si Joon Kim[6] [1]The University of Texas at Dallas, [2]Inha University, [3]SK hynix inc. R&D, [4]Kookmin University, [5]Brookhaven National Laboratory, [6]Kangwon National University

We report the record-high remanent polarization value ($2P_r$ ~55 μC/cm^2) at an ultra-low operating voltage (0.5 V) with effective 3 nm hafnium zirconium oxide (HZO) capacitors. This exceptional ferroelectric property is achieved at a back-end-of-line (BEOL) compatible temperature below 400 °C. Moreover, our devices demonstrate configurable ferroelectric saturation characteristics, ensuring reliable and reproducible switching polarization states (P_{sw}). These results potentially allow the design of novel ferroelectric device circuitry. This study highlights the feasibility of extremely low-power ferroelectric applications beyond 0.5 V operation in BEOL.

4:40 PM

T15.4 Comprehensive Analysis of Duty-cycle Induced Degradations in $Hf_xZr_{1-x}O_2$-based Ferroelectric Capacitors: Behavior, Modeling, and Optimization, Guan Feng[1,2], Yu Li[1], Hao Jiang[1], Xiaodong Wang[1,2], Yize Sun[1], Yingfen Wei[1], Qi Liu[1,2], Ming Liu[1,2] [1]State Key Laboratory of Integrated Chips and Systems, Frontier Institute of Chip and System, Fudan University, Shanghai, 200433, China, [2]School of Microelectronics, Fudan University, Shanghai, 200433, China

This work systematically studies degradations in $Hf_xZr_{1-x}O_2$ (HZO)-based ferroelectric (FE) capacitors (FeCaps) under pulses with different duty cycles (DCs): 1) a larger drop in the switchable polarization (P_{sw}) and shift in the coercive voltage (V_c) by duty-cycling are observed when compared with conventional endurance and retention tests; 2) through physical modeling, the wider spread of the generated oxygen vacancies (Vos) during duty-cycling leads to stronger domain pinning and the formation of a larger built-in field (E_{bi}), which explains the above observation; 3) optimizations through engineering the stack and composition of the HZO FE layer are proposed and validated on 128Kbit 2T2C FeRAM chips.

5:05 PM

T15.5 Engineering HZO by Flat Amorphous TiN with 0.3nm Roughness Achieving Uniform c-axis Alignment, Record High Breakdown Field (~10nm HZO), and Record Final $2P_r$ of 56 μC/cm² with Endurance > 4E12, Zefu Zhao[1], Yu-Rui Chen[1], Yu-Tsung Liao[1], Yun-Wen Chen[1], Wan-Hsuan Hsieh[1], Jer-Fu Wang[1], Yu-An Chen[1], Hao-Yi Lu[2], Wei-Teng Hsu[1], Dai-Ying Lee[3], Ming-Hsiu Lee[3], C. W. Liu[1,2,4] [1]Graduate Institute of Electronics Engineering, National Taiwan University, [2]Graduate School of Advanced

Technology, National Taiwan University, [3]Emerging Central Lab., Macronix International Co., Ltd., Hsinchu, Taiwan, R.O.C., [4]Graduate Institute of Photonics and Optoelectronics, National Taiwan University
Metal-ferroelectric-metal capacitors with flat amorphous TiN are demonstrated to achieve c-axis of orthorhombic phase well-aligned along deposition direction, uniform electric field, negligible fatigue, and high remanent polarization ($2P_r$) of 62 μC/cm^2. The large lattice misfit between crystalline TiN and HZO creates larger barrier to form the o-phase HZO as compared to amorphous TiN underlayer. Using chemical-mechanical polishing can obtain a 0.3nm roughness flat TiN, measured by AFM. HZO on flat amorphous TiN exhibits uniform and record breakdown field (EBD) of 4.8/-5.1 MV/cm for positive/negative voltage. A flat TiN mitigates formation of oxygen vacancies as compared to rough TiN due to weak and uniform electric field in HZO. After 4E12 endurance cycles, the HZO on flat TiN exhibits a record final 2Pr of 56 μC/cm^2 due to small dipole pinning by V_o^{2+}. This work demonstrates the way to achieve uniformly high $2P_r$, large EBD, and high endurance by flat amorphous TiN.

Session T16: Reliability, Characterization & Modeling of Oxide Semiconductor and Si Devices-2

3:25 PM, Tapa 2

Co-Chairs: Nandakumar Mahalingam, Texas Instruments
Yoshiki Yamamoto, Renesas Electronics

3:25 PM

T16.1 Unveiling the Impact of AC PBTI on Hydrogen Formation in Oxide Semiconductor Transistors, Gan Liu[1], Qiwen Kong[1], Zuopu Zhou[1], Ying Xu[1], Chen Sun[1], Kaizhen Han[1], Yuye Kang[1], Dong Zhang[1], Xiaolin Wang[1], Yang Feng[1], Wei Shi[1], Bich-Yen Nguyen[2], Kai Ni[3], GengChiau Liang[1,4], Xiao Gong[1]
[1]National University of Singapore, [2]Soitec, [3]University of Notre Dame, [4]Industry Academia Innovation School, National Yang-Ming Chiao Tung University
For the first time, we elucidate the impact of both alternating current (AC) and direct current (DC) positive bias temperature instability (PBTI) on hydrogen (H) formation of oxide semiconductor FETs (OSFET). Our investigation employs a systematic and holistic analysis on the highly stable co-sputtered Indium-Gallium-Zinc-Tin-oxide (IGZTO) FETs. Key discoveries include: (1) There are distinctive variations between AC and DC PBTI results at high temperatures (T). (2) In AC PBTI, both frequency (f) and duty factor (DF) play a crucial role in mitigating the H formation effect. (3) DF exhibits a more influential impact than f. (4) AC PBTI, particularly at 25% DF and 1 MHz, can alleviate up to 99.2% of the threshold voltage change (ΔV_{th}) induced by H formation from DC PBTI. These findings contribute significant insights into the H formation mechanism, providing a more relevant and accurate understanding of PBTI reliability across diverse real-world applications.

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T16.2 Positive Bias Stress Measurement Guideline and Band Analysis for Evaluating Instability of Oxide Semiconductor Transistors, Qi Jiang[1], Koustav Jana[1], Kasidit Toprasertpong[1], Shuhan Liu[1], H.-S. Philip Wong[1] [1]Stanford University
Instability of oxide semiconductor field effect transistors (OSFET) under positive bias stress (PBS) is one of the major hinderances to broad adoption by the semiconductor industry. We present a holistic understanding of the OSFET behavior under PBS, by comparing OSFETs with different channel doping (N_{CH}), hence different initial threshold voltages (V_{TH}). Our analysis reveals that the band profile of OSFETs under a given voltage is strongly dependent on their channel doping, resulting in different stress responses even for the same material properties. This raises the important question of finding the right metric to evaluate the stability of OSFETs. This work makes significant strides in establishing a PBS test guideline to ensure a fair benchmark method of OSFETs with vastly different N_{CH}, and understanding of the associated trade-off between PBS stability and V_{TH}.

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T16.3 Positive to Negative Schottky Barrier Transition in Metal/Oxide Semiconductor Contacts by Tuning Indium Concentration in IGZO, Sumi Lee[1], Chang Niu[1], Yizhi Zhang[1], Haiyan Wang[1], Peide Ye[1]
[1]Purdue University

In this work, we report the tunability of electrical performance and metal-to-semiconductor contact properties in atomic-layer-deposited (ALD) InGaZnO (IGZO) field-effect transistors (FETs) by precisely manipulating the In:Ga:Zn ratios. Our fabricated IGZO FETs exhibit well-behaved saturation in the short channel length (L_{ch}) of 80 nm and a high on-current of 850 μA/μm. Through temperature-dependent characterizations, we observed the transition from a negative to a positive Schottky barrier (Φ_{SB}) by adjusting the indium (In) concentrations. This transition is explained by the changes in the charge neutrality level (CNL) and Fermi level (E_F) at the contact interface. The impact of surface accumulation/depletion at the metal/semiconductor interface provides the new insight into the realm of contact engineering.

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T16.4 Fluorine Plasma Treatment-Enabled ITO Transistors: Excellent Reliability and Comprehensive Understanding of Temperature Dependence from 77 K to 375 K, Xuanqi Chen[1], Gan Liu[1], Wei Shi[1], Yuye Kang[1], Qiwen Kong[1], Yuxuan Wang[1], Rui Shao[1], Bich-Yen Nguyen[2], Gengchiau Liang[1,3], Kaizhen Han[1], Xiao Gong[1] National University of Singapore, [2]Soitec, [3]National Yang-Ming Chiao Tung University

For the first time, we demonstrated the Fluorine (F) plasma-treated indium-tin-oxide field-effect transistors (ITO:F FETs) with comprehensive understanding of their electrical characteristics, low-frequency noise (LFN), and reliability across a broad range of temperatures, spanning from 77 K to 375 K. Remarkably, the ITO:F FET demonstrates excellent reliability. After 1 ks positive bias stressing under an electric field (E_{ov}: V_{ov}/T_{ox}) of 2.5 MV/cm, the ITO:F FET performs threshold voltage shifts (ΔV_{TH}) of 18 mV (300 K) and less than 3.77 mV (77 K) has been achieved. Furthermore, the ITO:F FET maintains its performance in other key figure-of-merits (FoMs) compared to its fluorine-free counterpart, including a field-effect mobility (μ_{eff}) of ~89 $cm^2/V\cdot s$ ($N_{carrier}$ of 5×10^{12} cm^{-2}), a subthreshold swing (SS) of 46 mV/decade at 77 K, and a drive current (I_{ON}) exceeding 1500 μA/μm (77 K).

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T16.5 A Novel Method for Extracting Asymmetric Source and Drain Resistance in IGZO Vertical Channel Transistors, Sungwon Yoo[1], Yongjin Lee[1], WooJe Jung[1], Hwan Kim[1], Seongjae Byeon[1], Miryeon Kim[1], Juho Lee[2], Tackhwi Lee[1], Minji Hong[1], Young Geun Song[1], Seungwon Lee[1], Masayuki Terai[1], Kyongjun Yoo[1], Changhyuk Sung[1], Wonsok Lee[1], Min Hee Cho[1], Dae Sin Kim[2], Daewon Ha[1], Sujin Ahn[1], Jaihyuk Song[1]
[1]Semiconductor R&D Center, Samsung Electronics, [2]Computational Science & Engineering group, Samsung Electronics

Unlike conventional resistance extraction method, a novel method enabling to simply extract the source/drain resistance including contact resistance is, for the first time, hereby proposed in the IGZO vertical channel transistor (VCT). IGZO VCT has uneven source and drain structure inducing considerable asymmetricity in source and drain resistances, thus the extraction of them is very important. This method is based on the fact that the amount of current varies significantly depending on the direction of electron injection in the structure forming the schottky contacts. Experimental results show that this method is adequate to evaluate improvements in the contact resistance and thus applicable for source and drain resistance analysis in oxide semiconductor structures.

Session T17: Memory Technology: NAND, DRAM-2

3:25 PM, Tapa 3

Co-Chairs: Alessandro Calderoni, Micron Technology
Tomohiko Kudo, Micron

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T17.1 DRAM-peri FinFET – A Thermally-stable High-Performance Advanced CMOS RMG Platform with Mo-based pWFM for sub-10nm DRAM, Jishnu Ganguly[1], Hiroaki Arimura[1], Romain Ritzenthaler[1], Harsh Bana[2], Jan Willem Maes[2], Ju-Geng Lai[1], Stephan Brus[1], Waleed Maqsood[1], Ritam Sarkar[1], Balaji Kannan[3], Elena Capogreco[1], Vladimir Machkaoutsan[4], Seunghwan Yoon[5], Alessio Spessot[1], Michael Givens[2], Naoto Horiguchi[1] [1]imec, [2]ASM Leuven, [3]ASM Phoenix, [4]Micron Technology, [5]SK Hynix

We report on an improved thermally-stable, high-performance CMOS RMG FinFET platform for DRAM-periphery beyond the 10nm node. This is a first demonstration of novel Mo and MoN work-function metal (WFM) integration into a high-performance dual-WFM + dual-dipole logic RMG flow, capable of enduring high thermal-budget linked to memory-array fabrication. We demonstrate superior N/P Vt balance compared to a TiN/TiAl dual-WFM + dual-dipole CMOS reference, as well as 0.12V PMOS Vt with Mo pWFM coupled with p-dipole down to scaled gate-lengths with excellent short-channel control.

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T17.2 4F^2 Stackable Polysilicon Channel Access Device for Ultra-Dense NVDRAM, Albert Liao[1], Matthew Jerry[1], Kamal Karda[1], Matt Hollander[1], Pankaj Sharma[1], Ruijing Ge[1], Ting Zhao[1], Gabriel Khalil EL hajjam[1], Marcello Mariani[1], Marcello Calabrese[1], Davide Raimondi[1], Antonino Rigano[1], Tommaso Rossi[1], Karine Florent[1], Nick Tapias[1], Clement Jacob[1], Alessandro Calderoni[1], Sameer Chhajed[1], John Zahurak[1], Nirmal Ramaswamy[1] [1]Micron

We report on the methodology and optimization used to enable a stackable 4F^2 polysilicon thin film transistor (TFT) for ultra-dense 32 Gb NVDRAM. Several key innovations are implemented to meet the strict thermal budget constraints required for a dual-layer technology. Confined heating from pulsed laser annealing is used to crystallize polysilicon and activate source/drain dopants. Material optimization is used to engineer both a gate oxide deposited at low temperatures capable of 10 years equivalent reliability and a Ru wordline (WL) robust to agglomeration and voiding failures. Device performance, robust to top layer processing, is matched across both layers by adjusting process conditions as informed by a TCAD model that accounts for heat transfer and crystallization dynamics.

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T17.3 A Three Dimensional DRAM (3D DRAM) Technology for the Next Decades (Late News), Joodong Park[1], kangsik Choi[1], Seunghwan Kim[1], Jungwon Seo[1], Hongseong Kang[1], Seungwan Chu[1], Seokwon Bae[1], Jeonghoon Kwon[1], Gilseop Kim[1], Yongtaek Park[1], Junha Kwak[1], Dongil Song[1], Sungmean Park[1], Yongtaik Kim[1], Kyoungchul Jang[1], Jinsun Cho[1], Heesun Lee[1], Byungho Lee[1], Jinwon Park[1], Jihye Lee[1], Hyuk Kwon[1], Dosun You[1], Chansun Hyun[1], Jaejung Lee[1], Seungcheol Lee[1], Ildo Kim[1], Juhyun Myung[1], Hyungsik Won[1], Junho Cheon[1], Kyunghoon Kim[1], Jiho Kang[1], Seungbum Kim[1], Kihong Lee[1], Suock Chung[1], Seonsoon Kim[1], Byoungki Lee[1], Choonhwan Kim[1], Seonyong Cha[1] [1]SKhynix

Three dimensional structured DRAM technology has drawn huge attention recently for its potential to fulfill high speed operation and low power consumption. In this paper, 3D DRAM with vertical bit line (BL) architecture is introduced as a promising solution to overcome scaling limitation for future DRAM technology. Full chip integration with 5-layered cell stacked on peri-core wafer is successfully demonstrated for the first time, offering superior on-current performance and gate controllability. A novel process integration scheme using Si/SiGe sacrificial multilayers and hybrid wafer bonding technique is presented with excellent full chip operation of 3D DRAM.

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T17.4 Cell to Core-Periphery Overlap (C2O) based on BCAT for next generation DRAM, Kiseok Lee[1], Hongjun Lee[1], Hyungeun Choi[1], Jeongsu Kim[1], Kyunghwan Kim[1], Moonyoung Jeong[1], Soohyun Bae[1], Hyebin Kim[1], Jiyun Lee[1], Minsoo Kim[1], Keunnam Kim[1], Huijung Kim[1], Sungmin Park[1], Taejin Park[1], Jin-woo Han[1], Jeonghoon Oh[1], Yong Kwan Kim[1], Sungsoo Yim[1], Bongsoo Kim[1], Jemin Park[1], Jaihyuk Song[2] [1]DRAM Technology Development, Samsung Electronics Co. Ltd., [2]Device Solutions CTO, Samsung Electronics Co. Ltd.

The ongoing trend of DRAM design rule scaling has faced with serious challenges. This paper focuses on sustaining the scaling momentum by introducing Cell to Core-Periphery Overlap (C2O) based on Buried Channel Array Transistors (BCAT). This approach enables bit growth and bit cost reduction with less scaling and introducing wafer bonding technique. Moreover, by expanding the core area and reducing mismatch, we significantly enhance sensing characteristics, thereby relaxing the storage capacitance burden. Additionally, stress-induced experiments by the wafer bonding process demonstrate that these improvements do not adversely affect the performance of DRAM core-periphery transistors.

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T17.5 Single metal BCAT breakthrough to open a new era of 12 nm DRAM and beyond, Kyosuk Chae[1], Taiuk Rim[2], Youngwoo Son[3], Heejae Choi[3,3], Jinseong Lee[3,4], Shinwoo Jeong[3], Jieun Lee[3], DONGIN Lee[3], Byunghyun Lee[3,3], Dongsoo Woo[3], Seguen Park[3], Sangjun Hwang[3] [1]Samsung Electronics, [2]Samsung Elecronics, [3]Samsung Elecronics, [4]Samsung Electronics

As the transistor area reaches the atomic scale, many technical challenges have occurred, jeopardizing the lifespan of DRAM scaling, of which word line (WL) resistive defects and Row hammer (R/H) failures are two of the most important quality problems. This paper introduces an innovative process technology to realize a high-purity and low-resistance cell WL that can solve two critical hurdles simultaneously, enabling the DRAM node of 12 nm and beyond. This technology verified a decrease in WL resistance by ~50% and a two orders of magnitude improvement in R/H fail bits. In addition, by reducing interface trap density (Nit), significant enhancements in the on/off characteristic window and air transportation defects were obtained.

Session C28: Processors II

3:25 PM, Honolulu 1

Co-Chairs: Lindsey Kostas, Qualcomm
Yukihiro Sasagawa, Socionext Inc.

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C28.1 Medusa: A 0.83/4.6 μ/Frame 86/91.6%-CIFAR-10 tinyML Processor with Pipelined Pixel Streaming of Bottleneck Layers in 28nm CMOS, Rohan Prashant Doshi[1], Massimo Giordano[1], Justin Olah[1], Zhidong Cao[1], MoonHyung Jang[1], Luke R Upton[1], Athanasios Ramkaj[1], Boris Murmann[1] [1]Stanford University

Medusa is a 28 nm programmable 8-bit processor that achieves state-of-the-art inference energy across a range of always-on tiny Machine Learning (tinyML) tasks. It features custom 6T-latch-based Inner Loop Memories (ILMs) optimized for tinyML that achieve a read energy of 15 fJ/Byte, and its Pipelined Pixel Streaming (PPS) architecture leverages ILMs to reduce system-level memory access energy by up to 9.5x. Medusa performs inference image-to-label, with native support for critical tinyML operations, including memory-intensive depthwise separable convolution-based bottleneck layers. It achieves 0.83/4.6 μJ/Frame at a latency of 0.6/2.6 ms and an accuracy of 86.2/91.6% on CIFAR-10, advancing the state-of-the art in inference energy by 3.4x/4.9x. In addition, it achieves 0.23 μJ/Frame at 0.27 ms and 90.8% on Google Speech Commands and 5.0 μJ/Frame and 3.8 ms at 81.5% on Visual Wake Words.

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C28.2 A Heterogeneous TinyML SoC with Energy-Event-Performance-Aware Management and Compute-in-Memory Two-Stage Event-Driven Wakeup, Yanchi Dong[1], Xueping Liu[1], Kangbo Bai[1], Guoxiang Li[1], Meng Wu[1], Yiqi Jing[1], Yihan Zhang[1], Pixian Zhan[2], Yadong Zhang[2], Yufei Ma[1], Ru Huang[1], Le Ye[1,3], Tianyu Jia[1] [1]Peking University, [2]Nano Core Chip Electronic Technology, [3]Advanced Institute of Information Technology of Peking University

This paper presents a heterogeneous TinyML SoC with E^2P-aware system-level energy management achieving a minimum 3.5µW and 30000× peak-to-idle power ratio. The energy-event-performance (E^2P)-aware management utilizes various fully synthesizable monitors to be aware of the runtime status of heterogeneous blocks and hierarchical voltage regulation for MEP search at system level, which gains >28% energy saving compared to single block MEP. A 2-stage CIM-based event-driven wakeup scheme is also developed to reduce the always-on energy by over 87%. The presented TinyML SoC is suitable for edge AI applications with state-of-the-art low-power features.

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C28.3 A 101mW, 280fps Scene Graph Generation Processor for Visual Context Understanding on Mobile Devices, Chun-Wei Chang[1], I-Ting Lin[1], Chia-Hsiang Yang[1] [1]Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan

This work presents the *first* dedicated scene graph generation (SGG) processor for visual context understanding. Algorithm-architecture co-optimizations are applied to reduce the computational complexity. The memory usage is minimized through hybrid sparsity encoding and the energy efficiency is enhanced by utilizing reconfigurable multiply-accumulate (MAC) array architecture. The characteristic of the sigmoid function is leveraged to reduce the computations for edge features. Fabricated in 40-nm CMOS, the chip achieves a throughput of 280fps with an energy consumption of 0.36mJ/frame. It delivers a 154x higher throughput with 1,800x less power, yielding 2.7×10^5x higher energy efficiency than GPU.

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C28.4 An 11.4mm² 40.2Gbps 17.4pJ/b/iteration Soft-Decision Open Forward Error Correction Decoder for Optical Communication, Cheng-Hsun Lu[1], Wei Tang[1], Jiyoon Han[1], Zhengya Zhang[1] [1]University of Michigan

An iterative soft-decision open Forward Error Correction (oFEC) decoder is presented. The design utilizes a tile-based architecture, a difference-based soft-decision decoding for oFEC's component Bose-Chaudhuri-Hocquenghem (BCH) code, a low-latency general interleaver, and a matrix memory tailored to the oFEC structure. A dual-core prototype, implemented in Intel 16, occupies 11.4mm² and achieves 40.2Gbps at 17.4pJ/b/iteration.

Session C29: PLLs

3:25 PM, Honolulu 2

Co-Chairs: Alvin Loke, NXP Semiconductors
Atsushi Motozawa, Renesas Electronics

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C29.1 A 9-GHz Subsampling-Chopper PLL with Charge-Share Cancelling and Achieving 57.8-fs-rms Jitter with 15dB In-band Noise Improvement, Xiangjian Kong[1], Kai Xu[2], Robert Bogdan Staszewski[3], Mingchao Jian[1], Chunbing Guo[1] [1]Guangdong University of Technology, [2]King's College London, [3]University College Dublin, Ireland

A 9-GHz sub-sampling (SS) PLL employs a new chopping charge-pump (CP) with controlled pre-charging or pre-discharging to cancel the charge sharing during the chopper's phase swapping, thus eliminating its 1/f noise. Fabricated in 65-nm CMOS, the prototype achieves 57.8-fs rms jitter with -111.9-dBc/Hz in-band noise at 1kHz offset.

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C29.2 A 6.5-to-6.9-GHz SSPLL with Configurable Differential Dual-Edge SSPD Achieving 44-fs RMS Jitter, -260.7-dB FOM_{Jitter}, and -76.5-dBc Reference Spur, Tianle Chen[1,2], Hongyu Ren[1,2], Zunsong Yang[1], Yunbo Huang[3], Xianghe Meng[1], Weiwei Yan[1], Weidong Zhang[1], Xuqiang Zheng[1], Xuan Guo[1], Tetsuya Iizuka[4], Pui-In Mak[3], Yong Chen[3], Bo Li[1] [1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China, [2]University of Chinese Academy of Sciences, Beijing, China, [3]University of Macau, Macau, China, [4]The University of Tokyo, Tokyo, Japan

A dual-edge subsampling phase-locked loop (SSPLL) is proposed to reduce the in-band phase noise (PN) of the crystal oscillator (XO) and reference buffer (RBUF) by 3dB without degrading frequency resolution. It is able to achieve even and odd locking modes by configuring the dual-edge subsampling phase detector (SSPD) to ensure that the PLL can lock in steps of F_{REF}. With a 100-MHz input reference and 6.5-to-6.9-GHz output, the prototype in 65-nm CMOS achieves an RMS jitter of 44fs, a jitter-power figure-of-merit (FOM_{Jitter}) of −260.7-dB, and a spur level of −76.5dBc. The total power consumption is 4.4mW at 6.8GHz.

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C29.3 A 79.3fs_{rms} Jitter Fractional-N Digital PLL Based on a DTC Chopping Technique, Riccardo Moleri[1], Simone Mattia Dartizio[1], Michele Rossoni[1], Giacomo Castoro[1], Francesco Tesolin[1], Dmytro Cherniak[2], Carlo Samori[1], Andrea Leonardo Lacaita[1], Salvatore Levantino[1] [1]Politecnico di Milano, [2]Infineon Technologies

This work presents a fractional-N digital PLL leveraging a digital-to-time converter (DTC) chopping technique to improve spectral purity and jitter. By randomly moving the DTC between the reference and divider paths of the PLL, the fractional spurs induced by DTC non-linearity and the DTC flicker noise suppressed. The synthesizer, fabricated in 28nm CMOS, achieves 79.3fs_{rms} jitter and -63.6dBc fractional spur at 9.275GHz near-integer channels

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C29.4 A 5GHz Fractional-N PLL with 97fs_{rms} Jitter and -255.3dB FoM, Zhiqiang Huang[1], Fengjun Chen[1], Shuangfeng Kong[1] [1]The Hong Kong University of Science and Technology

By employing a binary-search-based DTC nonlinearity calibration technique with an auxiliary-DTC-based TDC, a 5GHz fractional-N PLL with a 100MHz reference is proposed to achieve a calibration time of 8.7us for DTC nonlinearity correction. With the DTC nonlinearity calibration, a gated LMS-based DTC gain calibration with DSM-1, and a tree-like DTC to reduce DTC's delay and jitter, the proposed PLL measures -62dBc in-band fractional spurs and an integrated jitter of 97fs with 3.15mW power consumption, resulting in a FoM of -255.3dB.