Technology Short Course

Monday, June 13, Tapa 3, 8:20 a.m. – 4:00 p.m.

Monolithic and Heterogenous Integration

Organizers: S. Datta, Notre Dame, K. Tomida, Sony Semiconductor Solutions Corporation

8:30 a.m.
Advanced Logic Scaling Using Monolithic 3D Integration, Marko Radosavljević, Intel

9:20 a.m.
Embedded Memory Scaling with Monolithic 3D Integration, Gouri Sankar Kar, imec

10:10 a.m. Break

10:30 a.m.
Key low temperature processes for a silicon-based 3D sequential integration, Xavier Garros, CEA-LETI

11:20 a.m.
2.5D and 3D Polylithic Integration Technologies, Muhannad Bakir, Georgia Tech

12:10 p.m. Lunch

1:20 p.m.
Design Challenges for Scale-out Chiplet-Based Systems, Puneet Gupta, University of California, Los Angeles

2:10 p.m.
Advanced Packaging Technology for Memory-Centric Solution, Ho-Young Son, SK Hynix

3:00 p.m. Break

3:20 p.m.
Heterogenous Integration Technologies for Silicon Photonic Transceivers, Ted Letavic, GlobalFoundries.

Circuits Short Course
Monday, June 13, Honolulu, 8:20 a.m. – 5:00 p.m.

Electronics that Drive the Next-Generation Smart Car

Organizers: A. Loke, NXP, K. Yoshioka, Keio University

8:30 a.m.
The Automotive Revolution Driven by Electronics, Vidya Rajagopalan, Rivian

9:20 a.m.
Standardization to Enable Sustainable Vehicle Architecture Development, Martin Bornemann, Aptiv Services Deutschland GmbH

10:10 a.m. Break

10:30 a.m.
Software-Defined SoC Architectures for Disruptive Automotive Applications, Marius Rotaru, NXP Semiconductors

11:20 a.m.
ADAS Domain Controller Computing for Safe and Secure Driving Automation, Katsushige Matsubara, Renesas

12:10 p.m. Lunch

1:20 p.m.
Auto Infotainment Evolution and Experience – A Leap Forward in IVI Experience over Time, Mirza Jahan, Subhomoy Chattopadhyay, Intel

2:10 p.m.
Emerging In-Vehicle-Networks for the Self-Driving Car, Ramin Farjad, Eliyanpro**,** Ragnar Jonsson, Marvell

3:00 p.m. Break

3:20 p.m.
Sensors for Automotive: Extending Human Senses to the Car, Tommaso Ungaretti, Simone Ferri, STMicroelectronics

4:10 p.m.
Fundamentals of Lidar Technology and Latest Developments, OIchi Kumagai, Sony Semiconductor Solutions Corporation

5:00 p.m.
Battery Management System for Automotive, Philippe Perruchoud, NXP Semiconductors

Joint Short Course

Monday, June 13, Tapa 2, 8:20 a.m. – 5:20 p.m.

Advances in Application-Specific Computing Systems and Technologies

Organizers:
S. Yu, Georgia Tech
Aaron Thean, National University of Singapore
R. Staszewski, University College Dublin
M. Yamaoka, Hitachi

8:30 a.m.
Advanced Computing: An Overview, Edoardo Charbon, EPFL

9:20 a.m.
Memory Design for Custom Augmented Reality Silicon, Tony Wu, Meta

10:10 a.m. Break

10:30 a.m.
Silicon-Based Quantum Computing: The Path from the Laboratory to Industrial Manufacture, Andrew Dzurak, University of New South Wales

11:20 a.m.
Quantum Computing-Assisted Neural Networking, Dirk Leipold, Equal1

12:10 p.m. Lunch

1:20 p.m.
Photonics for Neuromorphic Computing, Paul Prucnal, Princeton University

2:10 p.m.
Advance in Embedded Compute-in-Memory Macros, Marvin Chang, TSMC / National Tsing Hua University

3:00 p.m. Break

3:20 p.m.
Near-DRAM Cell Computing on the Commercial DRAM Technology and its Future, Sukhan Lee, Samsung

4:10 p.m.
Intrinsically Stretchable Electronic Materials and Devices, Naoji Matsuhisa, Keio University

Demo Session and Reception – Tapa 1
6:00 p.m. – 8:00 p.m.

Joint Technology/Circuits Panel - Tapa 2
Monday, June 13, 8:00 p.m. – 10:00 p.m.

Organizers:
J. Wuu, AMD
P. Ye, Purdue University
P. Nadeau, Analog Devices
T. Nezuka, MIRISE Technologies Corp.
M. Tada, NanoBridge Semiconductor, Inc.

Supply…Unchained? Will the Chip Shortage Continue?
Moderator: Joe Macri, AMD

How did the semiconductor industry land in the current supply shortage? What would it take to return to a healthy supply chain, or is the shortage here to stay? This panel, moderated by Joe Macri from AMD, brings together industry experts representing viewpoints from leading foundries/IDMs, OSATs, fabless designers, materials suppliers, and equipment makers for an exciting look into (and debate on) where the issues lie, and how the industry can come together to overcome the supply chain shortage.

Panelists:
Yin Chang, ASE
Chidi Chidambaram, Qualcomm
Neil Fernandes, Lam Research
Thomas Piliszczuk, SOITEC
Sang-Pil Sim, Samsung

Session 1 – Tapa 1, 2, 3
Plenary Session

Tuesday, June 14, 8:05 a.m.
Chairpersons: G. Jurczak, Lam Research
B. Nikolić, University of California, Berkley

8:05 a.m. **Welcome and Opening Remarks and Awards**
T. Palacios, Massachusestts Institute of Technology
B. Ginsburg, Texas Instruments

1.1 – 8:40 a.m.
From System-on-Chip (SOC) to System on Multichip (SOMC) Architectures: Scaling Integrated Systems Beyond the Limitations of Deep-Submicron Single Chip Technologies (Invited), Christopher Patrick, Qualcomm, SVP & GM, Mobile Handset

1.2 – 9:20 a.m.
Holistic Patterning to Advance Semiconductor Manufacturing for the 2020s and Beyond (Invited),
Martin van den Brink, ASML, President and CTO

Session T1 - Tapa 1, 2, 3
Highlights
Tuesday, June 14

Co-Chairs: V. Narayanan, IBM
K. Endo, National Institute of Advanced Industrial Science and Technology

T01-1 - 10:15 a.m.
Intel 4 CMOS Technology Featuring Advanced FinFET Transistors optimized for High Density and High-Performance Computing, B. Sell, S. An, J. Armstrong, D. Bahr, B. Bains, R. bambery, D. Basu, D. Bergstrom, S. Bhowmick, D. Caselli, P. Elfick, S. Govindaraju, W. Hafez, M. Hattendorf, M. Jang, G. Kameswaran, Y. Luo, P. Packan, A. Paliwal, R. Ramaswamy, S. Subramanian, Intel

T01-2 - 10:40 a.m.
Scaled FinFETs Connected by Using Both Wafer Sides for Routing via Buried Power Rails, A. Veloso, A. Jourdain, D. Radisic, R. Chen, G. Arutchelvan, B. OSullivan, H. Arimura, M. Stucchi, A. De Keersgieter, M. Hosseini, T. Hopf, K. Dhave, S. Wang, E. Dupuy, G. Mannaert, K. Vandersmissen, S. Iacovo, P. Marien, S. Choudhury, F. Schleicher, F. Sebaai, Y. Oniki, X. Zhou, A. Gupta, T. Schram, B. Briggs, C. Lorant, E. Rosseel, A. Hikavyy, R. Loo, J. Geypen, D. Batuk, G. Martinez, J-P Soulie, K. Devriendt, B. Chan, S. Demuynck, G. Hiblot, G. Van der Plas , J. Ryckaert, G. Beyer, E. Dentoni Litta, E. Beyne, N. Horiguchi, Imec

T01-3 - 11:05 a.m.
A 2-Layer Transistor Pixel Stacked CMOS Image Sensor with Oxide-Based Full Trench Isolation for Large Full Well Capacity and High Quantum Efficiency, K. Zaitsu, A. Matsumoto, M. Nishida, Y. Tanaka, H. Yamashita, Y. Satake, T. Watanabe*, K. Araki*, N. Nei*, K. Nakazawa, J. Yamamoto, M. Uehara, H. Kawashima*, Y. Kobayashi*, T. Hirano, K. Tatani*, Sony Semiconductor Solutions Corporation, *Sony Semiconductor Manufacturing Corporation

T01-4 - 11:30 a.m.
Reliable Sub-nanosecond MRAM with Double Spin-torque Magnetic Tunnel Junctions, C. Safranski, G. Hu, J. Sun, P. Hashemi, S. Brown, L. Buzi, C. D'Emic, E. Edwards, E. Galligan, M. Gottwald, O. Gunawan, S. Karimeddiny, H. Jung, J. Kim, K. Latzko, P. Trouilloud, S. Zare, D. Worledge, IBM TJ Watson Research Center

T01-5 - 11:55 a.m.
Wafer-Scale Bi-Assisted Semi-Auto Dry Transfer and Fabrication of High-Performance Monolayer CVD WS2 Transistor, M-Y Li, C-H Hsu*, S-W Shen, A-S Chou, Y. Lin, C-P Chuu, N. Yang, S-A Chou, L-Y Huang, C-C Cheng, W-Y Woon, S. Liao, C-I Wu*, L-J Li, I. Radu, H-S P. Wang, H. Wang, TSMC, *National Taiwan University

Session C1 - Honolulu Suite
Frequency Generation
Tuesday, June 14

Co-Chairs: C. Sandner, Infineon
K. Okada, Tokyo Institute of Technology

C01-1 - 10:15 a.m.
A Reference-Free Phase Noise Measurement Circuit Achieving 24.2 fs Periodic Jitter Sensitivity and 275 fs_{rms} Resolution with Background Self-Calibration, W-J Jian, W-Z Chen, National Yang Ming Chiao Tung University

C01-2 - 10:40 a.m.
A 10-GHz Inductorless Cascaded PLL with Zero-ISF Subsampling Phase Detector Achieving -63-dBc Reference Spur, 175-fs RMS Jitter and -240-dB FOMjitter, Z. Yang, Z. Xu, M. Osada, T. Iizuka, The University of Tokyo

C01-3 - 11:05 a.m.
A Magnetically Coupled Dual-Core 154-GHz Class-F Oscillator with -177.1 FoM and -87 dBc/Hz PN at 1-MHz Offset in a 22-nm FDSOI with Third-Harmonic Extraction, S. Sharma, H. Gao, G. Hueber, A. Mazzanti*, Silicon Austria Labs, *University of Pavia

C01-4 - 11:30 a.m.
A DPLL-Based Phase Modulator Achieving -46dB EVM with A Fast Two-Step DCO Nonlinearity Calibration and Non-Uniform Clock Compensation, Z. Gao, M. Fritz, J. He, G. Spalink, R. Staszewski*, M. Alavi**, M. Babaie**, Sony Europe B.V., *University College Dublin, **Delft University of Technology

Plenary Session II
Tapa 1, 2, 3

Tuesday, June 14, 1:20 p.m.
Chairpersons: T. Tsunomura, Tokyo Electron Ltd.
M. Hamada, The University of Tokyo

1:20 p.m. **Welcome and Opening Remarks**
K. Miyashita, Toshiba Electronic Devices and Storage Corp.
Y. Oike, Sony Semiconductor Solutions Corp.

1.1 – 1:30 p.m.
The Rise of Memory in the Ever-Changing AI Era – From Memory to More-Than-Memory (Invited), Dr. Seok-Hee Lee, SK Hynix, President and Chief Executive Officer

1.2 – 2:10 p.m.
Semiconductor Innovations, From Device to System, Dr. Y.J. Mii, Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC), Senior Vice President of Research and Development (R&D)

Session T2 - Tapa 1

IGZO Channel FET for Logic and Memory Applications
Tuesday, June 14

Co-Chairs: P. Grudowski, NXP
K. Endo, National Institute of Advanced Industrial Science and Technology

T02-1 - 3:00 p.m.
Ultra-low Leakage IGZO-TFTs with Raised Source/Drain for Vt >0 V and Ion >30 µA/µm, S. Subhechha, N. Rassoul, A. Belmonte, H. Hody, H. Dekkers, M. van Setten, A. Chasin, S. Sharifi, S. Sutar, L. Magnarin, U. Celano, H. Puliyalil, S. Kundu, M. Pak, L. Teugels, D. Tsvetanova, N. Bazzazian, K. Vandersmissen, C. Biasotto, D. Batuk, J. Geypen, J. Heijlen, R. Delhougne, G. Kar, imec

T02-2 - 3:25 p.m.
Extremely Scaled Bottom Gate a-IGZO Transistors Using a Novel Patterning Technique Achieving Record High Gm of 479.5 µS/µm (V_{DS} of 3V), C. Wang, A. Kumar, K. Han, C. Sun, H. Xu, J. Zhang, Y. Kang, Q. Kong, Z. Zheng, Y. Wang, X. Gong, National University of Singapore

T02-3 - 3:50 p.m.
Vertical Channel-All-Around (CAA) IGZO FET under 50 nm CD with High Read Current of 32.8 µA/µm (Vth + 1 V), Well-performed Thermal Stability up to 120 ℃ for Low Latency, High-density 2T0C 3D DRAM Application, K. Huang, X. Duan*, J. Feng, Y. Sun, C. Lu*,C. Chen*, G. Jiao, X. Lin, J. Shao, S. Yin, J. Sheng, Z. Wang, W. Zhang, X. Chuai*, J. Niu*, Y. Wu, W. Jing, Z. Wang, J. Xu, G. Yang*, D. Geng*, L. Li*, M. Liu*, Huawei Technologies Co., LTD., *Institute of Microelectronics of the Chinese Academy of Sciences

T02-4 - 4:15 p.m.
Scaling Dual-Gate Ultra-thin a-IGZO FET to 30 nm Channel Length with Record-high Gm,max of 559 µS/µm at VDS=1 V, Record-low DIBL of 10 mV/V and Nearly Ideal SS of 63 mV/dec, K. Chen, J. Niu, G. Yang, M. Liu, W. Lu, F. Liao, X. Duan, K. Huang, C. Lu, J. Wang, L. Wang, M. Li, D. Geng, N. Lu, L. Li, M. Liu, Institute of Microelectronics, Chinese Academy of Sciences

T02-5 - 4:40 p.m.
Compact Modeling of IGZO-based CAA-FETs with Time-zero-instability and BTI Impact on Device and Capacitor-less DRAM Retention Reliability, J. Guo, Y. Sun*, L. Wang, X. Duan, K. Huang*, Z. Wang*, LTD, J. Feng*, Q. Chen, S. Huang, L. Xu, D. Geng, G. Jiao*, S. Yin*, Z. Wang*, W. Jing*, L. Li, M. Liu, The Institute of Microelectronics of the Chinese Academy of Sciences, *Huawei Technologies

Session C2 – Tapa 2
ML
Tuesday, June 14

Co-Chairs: P. Raina, Stanford Univ.
V. Honkote, Intel

C02-1 - 3:00 p.m.
A 17–95.6 TOPS/W Deep Learning Inference Accelerator with Per-Vector Scaled 4-bit Quantization for Transformers in 5nm, B. Keller, R. Venkatesan, S. Dai, S. Tell, B. Zimmer, W. Dally, C. Gray, B. Khailany, NVIDIA

C02-2 - 3:25 p.m.
Audio and Image Cross-Modal Intelligence via a 10TOPS/W 22nm SoC with Back-Propagation and Dynamic Power Gating, Z. Fan, H. An, Q. Zhang, B. Xu, L. Xu, C-W Tseng, Y. Peng, A. Cao, B. Liu, C. Lee, Z. Wang, F. Liu, G. Wang, S. Jiang, H-S Kim, D. Blaauw, D. Sylvester, University of Michigan, Ann Arbor

C02-3 - 3:50 p.m.
TinyVers: A 0.8-17 TOPS/W, 1.7 µW-20 mW, Tiny Versatile System-on-chip with State-retentive eMRAM for Machine Learning Inference at the Extreme Edge, V. Jain, S. Giraldo, J. De Roose, B. Boons, Magics Instruments, L. Mei, M. Verhelst, KU Leuven

C02-4 - 4:15 p.m.
A 2.4GHz, Double-Buffered, 4kb Standard-Cell-Based Register File with Low-Power Mixed-Frequency Clocking for Machine Learning Accelerators, S. Hsu, A. Agarwal, M. Anders, A. Raha, R. Sung, D. Mathaikutty, R. Krishnamurthy, J. Tschanz, V. De, Intel Corp.

C02-5 - 4:40 p.m.
A 12nm 121-TOPS/W 41.6-TOPS/mm2 All Digital Full Precision SRAM-based Computie-in-Memory with Configurable Bit-width For AI Edge Applications, C-F Lee, C-H Lu, C-E Lee, H. Mori, H. Fujiwara, Y-C Shih, T-L Chou, Y-D Chih, J. Chang, TSMC

Session C3 – Tapa 1
Wireline
Tuesday, June 14

Co-Chairs: P. Upadhyaya, Xilinx
T. Iwai, Kioxia

C03-1 - 3:00 p.m.
A 1-to-112Gb/s DSP-Based Wireline Transceiver with a Flexible Clocking Scheme in 5nm FinFET, A. Varzaghani, B. Bozorgzadeh, J. Lam, A. Goel, X. Yuan, M. Elzeftawi, M. Izad, S. Sarkar, A. Baldisserotto, S-R Ryu, S. Mikes, J. Hwang, V. Joshi, S. Naraghi, D. Kadia, M. Ranjbar, P. Lee, D. loizos, S. Zogopoulos, S. Verma, S. Sidiropoulos, Cadence

C03-2 - 3:25 p.m.
A 72GS/s, 8-bit DAC-based Wireline Transmitter in 4nm FinFET CMOS for 200+Gb/s Serial Links, T. Dickson, Z. Deniz, M. Cochet, M. Kossel, T. Morf, Y-H Choi*, P. Francese, M. Braendli, T. Beukema, C.

Baks, J. Proesel, J. Bulzacchelli, M. Beakes, B-J Yoo*, H. Ahn*, D-H Lim*, G. Kang*, S-H Park*, M. Meghelli, H-G Rhew*, D. Friedman, M. Choi*, M. Soyuer, J. Shin*, IBM Research, *Samsung Electronics

C03-3 - 3:50 p.m.
0.41-pJ/b/dB Asymmetric Simultaneous Bidirectional Transceivers With PAM-4 Forward and PAM-2 Back Channels for 5-m Automotive Camera Link, Y. Lee, W. Lee, M. Shim, S. Shin, Samsung Electronics, W-S Choi, D-K Jeong, Seoul National University

C03-4 - 4:15 p.m.
A 9 Gb/s 1.1 V_{pp} Precision Single-Ended Pin Electronics Driver in 40nm CMOS, P. van der Wagt, A. Parks, G. Warwar, L. Choi, B. Salz, S-T Chen, R. Sartschev, D. Gajjar, Teradyne

C03-5 - 4:40 p.m.
A 200Gb/s PAM-4 Transmitter with Hybrid Sub-Sampling PLL in 28nm CMOS Technology, Z. Wang, M. Choi*, P. Kwon, K. Lee**, B. Yin, Z. Liu, K. Park, A. Biswas, J. Han***, S. Du^, E. Alon, University of California, Berkeley, *Samsung Semiconductor, **University of California, San Francisco, Hanyang*** University, ^Delft University of Technology

Panel Sessions

Tuesday, June 14, 8:00 p.m. – 10:00 p.m.

Technology Panel Session - Tapa 1
Organizers: P. Ye, Purdue University
M. Tada, Nanobridge Semiconductor

What will it take to bring new material from lab to manufacturing?
Moderator: Robert Clark, Tokyo Electron

How can we make sure the thousands of newly explored materials in academic, government, and industry labs are relevant to manufacturing technologies? What are the fundamental factors to convert a success story to a technology transfer? Is there anything to be learned from history? Robert Clark from TEL will moderate a panel of distinguished guests from across industry and academia to offer their valuable insights and thoughts and share their experience on this important and interesting topic.

Panelists:
Michael Givens, ASM
Naoto Horiguchi, imec
Benjamin Jurcik, Air Liquide
Aki Nishiyama, Kioxia
Shinichi Takagi, Univ. of Tokyo
Kashyap Yellai, SRC

Circuits Panel Session - Tapa 2
Organizers: J. Wuu, AMD
A. Thomsen, Cirrus Logic
T. Nezuka, MIRISE Technologies Corp.

Building the 2030 Workforce: How to attract great students and what to teach them?
Moderator: B. Murmann, Stanford

With declining university enrollment in the semiconductor fields, and a shortage of skilled engineers across the industry, what can universities do to reverse the trend and ensure a robust workforce heading into 2030? What should the students learn to best prepare them for the industry's emerging needs? Prof. Boris Murmann from Stanford University will moderate a panel of distinguished guests from across the industry and academia to offer their valuable insights and explore this important topic.

Panelists:

Edith Beigne, Meta
Raja Koduri, Intel
Lawrence Loh, MediaTek
Shanti Pavan, Indian Institute of Technology
Jan Rabaey, imec
Vivienne Sze, MIT

Session T3 - Tapa 3
Memory Technology: NAND, DRAM, FBRAM
Wednesday, June 15

Co-Chairs: J. Yu, Western Digital
K. Hamada, Micron Memory Japan

T03-1 - 8:10 a.m.
Multi-bit per-cell 1T SiGe Floating Body RAM for Cache Memory in Cryogenic Computing, W. Chakraborty, P. Shrestha*, A. Gupta, R. Saligram**, S. D. Spetalnick**, J. Campbell***, A. Raychowdhury**, S. Datta, University of Notre Dame, *National Institute of Standards and Technology, **Georgia Institute of Technology, ***Theiss Research

T03-2 - 8:35 a.m.
First Demonstration of 1-bit Erase in Vertical NAND Flash Memory, H-N Yoo, J-W Back, N-H Kim*, D. Kwon, B-G Park, J-H Lee, Seoul National University, *SK Hynix Inc.

T03-3 - 9:00 a.m.
High Performance Thermally Resistant FinFETs DRAM Peripheral CMOS FinFETs with VTH Tunability for Future Memories, R. Ritzenthaler, E. Capogreco, E. Dupuy, H. Arimura, J. Bastos, P. Favia, F. Sebaai, D. Radisic, V. Nguyen, G. Mannaert, B. Chan, V. Machkaoutsan*, Y. Yoon**, H. Itokawa***, M. Yamaguchi***, Y. Chen^, P. Fazan*, S. Subramanian, A. Spessot, E. Dentoni Litta, S. Samavedam, N. Horiguchi, imec, *Micron, **SK-Hynix, ***Kioxia, ^Western Digital

T03-4 - 9:25 a.m.
Optimal Cell Structure/Operation Design of 3D Semicircular Split-gate Cells for Ultra-high-density Flash Memory, T. Morooka, , T. Ishikawa, , M. Komura, T. Kato, Y. Koyama, y. Han, Y. Sugawara, D. Kuwabara, Y. Aarayashiki, A. Murayama, K. Nishiyama, K. Sugimae, T. Ogura, H. Takeda, N. Kariya, Y. Goki, S. Konuma, Y. Kamiya, H. Yamashita, H. Shiga, K. Itagaki, R. Tanaka, T. Maeda, N. Ohtani, M. Fujiwara, Kioxia

Technology Focus Session 1 - Tapa 2
New Device Concepts for Scaled Logic, Memory and QC Application
Wednesday, June 15

Co-Chairs: N. Collaert, imec
B.H. Lee, Pohang University of Science and Technology

TFS1-1 - 8:10 a.m.
Specificities of linear Si QD arrays integration and characterization (Invited), H. Niebojewski, B. Bertrand, E. Nowak, T. Bédécarrats, B. Cardoso Paz*, L. Contamin, P.A. Mortemousque, V. Labracherie, L. Brevard, H. Sahin, J. Charbonnier, C. Thomas, M. Assous, M. Cassé, M. Urdampilleta*, Y.-M. Niquet**, F. Perruchot, F. Gaillard, S. De Franceschi**, T. Meunier*, M. Vinet, Université Grenoble Alpes and CEA-Leti, *CNRS Institut Néel, **CEA-Irig

TFS1-2 - 8:35 a.m.
Prospective Innovation of DRAM, Flash, and Logic Technologies for Digital Transformation (DX) Era (Invited), D. Ha, H-S Kim, Samsung Electronics

TFS1-3 - 9:00 a.m.
300 mm MOCVD 2D CMOS Materials for More (Than) Moore Scaling, K. Maxey, C. Naylor, K. O'Brien, A. Penumatcha, A. Oni, C. Mokhtarzadeh, C. Dorow, C. Rogan, B. Holybee, T. Tronic, D. Adams, N. Arefin, A. Sen Gupta, C-c Lin, T. Zhong, S. Lee, A. Kitamura, R. Bristol, S. Clendenning, U. Avci, M. Metz, Intel

TFS1-4 - 9:25 a.m.
On the PBTI Reliability of Low EOT Negative Capacitance 1.8 nm HfO2-ZrO2 Superlattice Gate Stack on Lg=90 nm nFETs, N. Shanker, L-C Wang, S. Cheema, W. Li, N. Choudhury*, C. Hu, S. Mahapatra*, S. Salahuddin, University of California, Berkeley, *Indian Institute of Technology Bombay

Session C4 - Tapa 1
ML Processors
Wednesday, June 15

Co-Chairs: A. Raychowdhury, Georgia Tech
Y. Lee, Pohang University of Science and Technology

C04-1 - 8:10 a.m.
A 32.2 TOPS/W SRAM Compute-in-Memory Macro Employing a Linear 8-bit C-2C Ladder for Charge Domain Computation in 22nm for Edge Inference, H. Wang, R. Liu, R. Dorrance, D. Dasalukunte, X. Liu, D. Lake, B. Carlton, M. Wu, Intel Labs

C04-2 - 8:35 a.m.
Neuro-CIM: A 310.4 TOPS/W Neuromorphic Computing-in-Memory Processor with Low WL/BL activity and Digital-Analog Mixed-mode Neuron Firing, S. Kim, S. Kim, S. Um, S. Kim, K. Kim*, H-J Yoo, KAIST, *University of Zurich

C04-3 - 9:00 a.m.
A 40-nm 646.6TOPS/W Sparsity-Scaling DNN Processor for On-Device Training, Z-S Fu, Y-C Lee, A. Park*, C-H Yang, National Taiwan University, *Qualcomm

C04-4 - 9:25 a.m.
A 28-nm 25.1 TOPS/W Sparsity-Aware CNN-GCN Deep Learning SoC for Mobile Augmented Reality, W-C Huang, I-T Lin, W-C Chen*, L-Y Lin*, N-S Chan*g, C-P Lin*, C-S Chen*, C-H Yang, National Taiwan University, *Taiwan Semiconductor Research Institute

Session C5 - Honolulu 1
Time-of-Flight and Low-Power Image Sensors
Wednesday, June 15

Co-Chairs: M. Rose, NXP Semiconductors
T. Takahashi, Sony Semiconductor Solutions Corp.

C05-1 - 8:10 a.m.
A 640×480 Indirect Time-of-Flight Image Sensor with Tetra Pixel Architecture for Tap Mismatch Calibration and Motion Artifact Suppression, J. Kang, Y. Park, J-H Hwang, J-H Chun*, J. Choi*, S-J Kim, Ulsan National Institute of Science and Technology, *SolidVue

C05-2 - 8:35 a.m.
A Hybrid Indirect ToF Image Sensor for Long-Range 3D Depth Measurement under High Ambient Light Conditions, K. Hatakeyama, Y. Okubo, T. Nakagome, M. Makino*, H. Takashima*, T. Akutsu**, T. Sawamoto**, M. Nagase**, T. Noguchi, S. Kawahito**, Toppan Inc., *Toppan Technical Design Center Co., Ltd., **Brookman Technology, Inc.

C05-3 - 9:00 a.m.
A 4-Tap CMOS Time-of-Flight Image Sensor with In-pixel Analog Memory Array Achieving 10Kfps High-Speed Range Imaging and Depth Precision Enhancement, C-C Kuo, R. Kuroda, Tohoku University

C05-4 - 9:25 a.m.
Imager with Dynamic LSB Adaptation and Ratiometric Readout for Low-Bit Depth 5- µW Peak Power in Purely-Harvested Systems, K. Ahmed, L. Lin, P. Salamani, M. Alioto, National University of Singapore

Session C6 - Honolulu 2
Oversampled ADCs
Wednesday, June 15

Co-Chairs: S. Ho, MediaTek
S. Kondo, Toshiba Corp.

C06-1 - 8:10 a.m.
A 600mV$_{PP}$-Input-Range 94.5dB-SNDR NS-SAR-Nested DSM with 4th-Order Truncation-Error Shaping and Input-Impedance Boosting for Biosignal Acquisition, K. Jeong, G. Yun, S. Ha*, M. Je, KAIST, *New York University Abu Dhabi

C06-2 - 8:35 a.m.
An 81.6dB SNDR 15.625MHz BW 3rd Order CT SDM with a True TI NS Quantizer, S. Lee, T. Kang, S. Song, K. Kwon, M. Flynn, University of Michigan

C06-3 - 9:00 a.m.

A 100kHz-Bandwidth 98.3dB-SNDR Noise-Shaping SAR ADC with Improved Mismatch Error Shaping and Speed-Up Techniques, K. Hasebe, S. Etou, D. Miyazaki, T. Iguchi, Y. Yagishita, M. Takasaki, T. Nogamida, H. Watanabe, T. Matsumoto, Y. Katayama, Sony Semiconductor Solutions Corporation

C06-4 - 9:25 a.m.
A First-Order Continuous-Time Noise-Shaping SAR ADC with Duty-Cycled Integrator, H. Li, Y. Shen, E. Cantatore, P. Harpe, Eindhoven University of Technology

Session C7 - Honolulu 3
Biomedical Systems
Wednesday, June 15

Co-Chairs: V. Chen, Carnegie Mellon Univ.
M. Je, KAIST

C07-1 - 8:10 a.m.
A 128-Channel AC-Coupled 1st-order Δ-Δ∑ IC for Neural Signal Acquisition, X. Yang, M. Ballini, C. Sawigun, W-Y Hsu, J-W Weijers, J. Putzeys, C. Lopez, imec

C07-2 - 8:35 a.m.
A 0.0014 mm^2, 1.18 TΩ Segmented Duty-Cycled Resistor Replacing Pseudo-Resistor for Neural Recording Interface Circuits, C. Livanelioglu, W. Choi, D. Kim, KAIST, J. Liao, R. Incandela, G. Cristiano, T. Jang, ETH Zürich

C07-3 - 9:00 a.m.
A 260×274 μm^2 572 nW Neural Recording Micromote Using Near-Infrared Power Transfer and an RF Data Uplink, G. Atzeni, J. Lim*, J. Liao, A. Novello, J. Lee*, E. Moon*, M. Barrow*, J. Letner*, J. Costello*, S. Nason*, P. Patel*, P. Patil*, H-S Kim*, C. Chestek*, J. Phillips*, D. Blaauw*, T. Jang, ETH Zurich, Zurich, *University of Michigan, Ann Arbor

C07-4 - 9:25 a.m.
Helix: An Electrochemical CMOS DNA Synthesizer, O. Ghadami, H. Lu, M. Chan, M. Tan, S. Chung, S. H. Lee, M. Holden, R. de Ridder, Avery Digital, B. Merriman, Avery Digital, D. Hall, University of California, San Diego

Session T4 - Tapa 3
Nonvolatile Memories: RRAM and PCM
Wednesday, June 15

Co-Chairs: A. Calderoni, Micron
M. Tada, NanoBridge Semiconductor, Inc.

T04-1 - 10:05 a.m.
First Demonstration of $Ge_2Sb_2Te_5$-Based Superlattice Phase Change Memory with Low Reset Current Density (~3 MA/cm^{-2}) and Low Resistance Drift (~0.002 at 105°C), A. I. Khan, C. Perez, X. Wu, B. Won*, K. Kim**, H. Kwon, P. Ramesh, K. Neilson, M. Asheghi, K. Saraswat, Z. Lee**, I-K Oh*, H-S P. Wong, K. Goodson, E. Pop, Stanford University, *Ajou University, **Ulsan National Institute of Science and Technology

T04-2 - 10:30 a.m.
Enhanced performance and low-power capability of SiGeAsSe-GeSbTe 1S1R phase-change memory operated in bipolar mode, T. Ravsher, D. Garbin*, A. Fantini*, R. Degraeve*, S. Clima*, G. Donadio*, S. Kundu*, H. Hody*, W. Devulder*, J. Van Houdt*, V. Afanas'ev, R. Delhougne*, G. Kar*, KU Leuven, *IMEC

T04-3 - 10:55 a.m.
8-Layer 3D Vertical Ru/AlO_xN_y/TiN RRAM with Mega-Ω Level LRS for Low Power and Ultrahigh-density Memory, S. Qin, M. Tung, E. Belliveau, S. Liu, J. Kwon, W-C Chen, Z. Jiang, S. S. Wong, H-S P. Wong, Stanford University

T04-4 - 11:20 a.m.
Highly Reliable 40nm Embedded Dual-Interface-Switching RRAM Technology for Display Driver IC Applications, L. Zhao, Z. Chen, D. Manea, S. Li, J. Li, Y. Zhu*, Z. Sui*, Z. Lu, Hefei Reliance Memory Ltd., *Semiconductor Manufacturing International (Beijing) Corp.

T04-5 - 11:45 a.m.
Demonstration of High Endurance Capability on Mega-Bit RRAM Macro and Model of ppm Level Failures, C-F Yang, C-Y Wu, M-C Shih, M-T Yang, M-H Yang, Y-T Wu, T-C Chien, C-W Lai, S-C Tsai, W-T Chu, A. Hung, TSMC

Technology Focus Session 2 - Tapa 2
Front and Backside Advanced Interconnect
Wednesday, June 15

Co-Chairs: M. Delaus, Analog Devices
O. Cheng, United Microelectronics Corp.

TFS2-1 - 10:05 a.m.
Advanced BEOL Materials, Processes, and Integration to Reduce Line Resistance of Damascene Cu, Co, and Subtractive Ru Interconnects (Invited), T. Nogami, O. Gluschenkov, Y. Sulehria, S. Nguyen, B. Peethala, H. Huang, H. Shobha, N. Lanzillo, R. Patlolla, D. Sil, A. Simon, D. Edelstein, N. Felix, J. Liu*, T. Tabata**, F. Massamuto**, S. Halty**, F. Roze**, Y. Okuno*, A. Uedono***, IBM Research, * SCREEN Semiconductor Solutions Co., **LASSE, ***Tsukuba University

TFS2-2 - 10:30 a.m.
Impact of Material Interface Geometry on Interconnect Resistance (Invited), L. Brogan, J. Reid, Lam Research Corp.

TFS2-3 - 10:55 a.m.
First demonstration of Two Metal Level Semi-damascene Interconnects with Fully Self-aligned Vias at 18MP, G. Murdoch, M. O'Toole, G. Marti, A. Pokhrel, D. Tsvetanova, S. Decoster, S. Kundu, Y. Oniki, A. Thiam, Q. T. Le, O. Pedreira, A. Lesniewska, G. Martinez, Z. Tokei, S. Park, imec

TFS2-4 - 11:20 a.m.
Backside PDN and 2.5D MIMCAP to Double Boost 2D and 3D ICs IR-Drop beyond 2nm Node, R. Chen, g. sisto, M. Stucchi, A. Jourdain, K. Miyaguchi, P. Schuddinck, P. Woeltgens*, H. lin, N. Kakarla, A.

Veloso, D. Milojevic**, O. Zografos, P. Weckx, G. Hellings, G. Van der Plas , J. Ryckaert, E. Beyne, Imec, *ASML, **University of Brussels

TFS2-5 - 11:45 a.m.
Enabling Active Backside Technology for ESD and LU Reliability in DTCO/STCO, K. Serbulova, S-H Chen*, G. Hellings*, A. Veloso*, A. Jourdain*, D. Linten*, J. De Boeck, G. Groeseneken, J. Ryckaert*, G. Van der Plas*, E. Beyne*, E. Dentoni Litta*, N. Horiguchi*, KU Leuven, *IMEC

Session C8 - Tapa 1
Processors
Wednesday, June 15

Co-Chairs: D. Stark, Meta
Y. Sasagawa, Socionext

C08-1 - 10:05 a.m.
An 8-core RISC-V Processor with Compute near Last Level Cache in Intel 4 CMOS, G. Chen, P. Knag, C. Tokunaga, R. Krishnamurthy, Intel

C08-2 - 10:30 a.m.
Amber: A 367 GOPS, 538 GOPS/W 16nm SoC with a Coarse-Grained Reconfigurable Array for Flexible Acceleration of Dense Linear Algebra, A. Carsello, K. Feng, T. Kong, K. Koul, Q. Liu, J. Melchert, G. Nyengele, M. Strange, K. Zhang, A. Nayak, J. Setter, J. Thomas, K. Sreedhar, P-H Chen, N. Bhagdikar, Z. Myers, B. D'Agostino, P. Joshi, S. Richardson, R. Bahr, C. Torng, M. Horowitz, P. Raina, Stanford University

C08-3 - 10:55 a.m.
A 22nm 3.5TOPS/W Flexible Micro-Robotic Vision SoC with 2MB eMRAM for Fully-on-Chip Intelligence, Q. Zhang, H. An, Z. Fan, Z. Wang, Z. Li, G. Wang, H-S Kim, D. Blaauw, D. Sylvester, University of Michigan

C08-4 - 11:20 a.m.
A 44.3mW 62.4fps Hyperspectral Image Processor for MAV Remote Sensing, Y-C Lo, Y-C Wu, C-H Yang, National Taiwan University

C08-5 - 11:45 a.m.
MAQO: A Scalable Many-Core Annealer for Quadratic Optimization, M. Bagherbeik, W. Xu, S. F. Mousavi, K. Kanda*, H. Tamura**, A. Sheikholeslami, University of Toronto, *Fujitsu Limited, **DXR Laboratory

Session C9 - Honolulu 1
Image Ranging, and Motion Sensors
Wednesday, June 15

Co-Chairs: P. Nadeau, Analog Devices
T. Izuka, University of Tokyo

C09-1 - 10:05 a.m.

A 39,000 Subexposures/s CMOS Image Sensor with Dual-tap Coded-exposure Data-memory Pixel for Adaptive Single-shot Computational Imaging, R. Gulve, N. Sarhangnejad, G. Dutta, M. Sakr, D. Ngyuen, R. Rangel, W. Chen, Z. Xia, M. Wei, N. Gusev, E. Lin, X. Sun, L. Hanxu, N. Katic, A. Abdelhadi, K. Kutulakos, R. Genov, University of Toronto

C09-2 - 10:30 a.m.
1200x84-pixels 30fps 64cc Solid-State LiDAR RX with a HV/LV transistors Hybrid Active-Quenching-SPAD Array and Background Digital PT Compensation, T. Sugimoto, T. T. Ta, K. Kokubun, S. Kondo, T. Itakura, H. Katagiri, Y. Ota, M. Sengoku, H. Kwon, K. Sasaki, H. Kubota, K. Suzuki, K. Kimura, A. Sai, TOSHIBA

C09-3 - 10:55 a.m.
A 100×80 CMOS Flash LiDAR Sensor with 0.0011mm2 In-Pixel Histogramming TDC Based on Analog Counter and Self-Calibrated Single-Slope ADC, S-H Han, B. Kim, S. Park, Y. Park, J-H Chun, SolidVue, J. Choi, SolidVue, S-J Kim, Ulsan National Institute of Science and Technology

C09-4 - 11:20 a.m.
A 184nW, 121μg/√Hz Noise Floor Triaxial MEMS Accelerometer with Integrated CMOS Readout Circuit and Variation-Compensated High Voltage MEMS Biasing, Y. Peng, S. Jeong, K. Choo, Y. Kim, L-Y Chen, R. Rothe, L. Xu, I. Gurin*, O. Oliaei**, V. Tsinker*, S. Bart*, P. Hartwell*, D. Blaauw, D. Sylvester, University of Michigan, Ann Arbor, *InvenSense Inc.

Session C10 - Honolulu 2
Nyquist Data Converters
Wednesday, June 15

Co-Chairs: A. Thomsen, Cirrus Logic
M. Fukazawa, Renesas

C10-1 - 10:05 a.m.
A 12-bit 8GS/s RF Sampling DAC with Code-Dependent Nonlinearity Compensation and Intersegmental Current-Mismatch Calibration in 5nm FinFET, B. Koo, S. Do, S. Nam, H. Shin, S. Lee, E. Oh, J. Hong, J. Lee, Y. Cho, M. Choi, J. Shin, Samsung Electronics

C10-2 - 10:30 a.m.
A 50 MS/s 65 dB-SNDR Pipelined SAR ADC using Capacitively Degenerated Two-Stage Dynamic Amplifier, H. Yoon, T. Kim, Y. Kwon, Y. Chae, Yonsei University

C10-3 - 10:55 a.m.
A 0.56mW 63.6dB SNDR 250MS/s SAR ADC in 8nm FinFET, J. Lee, Y. Lim, J. Lee, T. Jang, K. Kang, J. Cho, S. Oh, J. Lee, Samsung Electronics

C10-4 - 11:20 a.m.
A 9.8-fJ/conv.-step FoMW 8b 2.5-GS/s Single-Channel CDAC-Assisted Subranging ADC with Reference-Embedded Comparators, J-C Wang, B-Y Li, T-H Kuo, National Cheng Kung University

C10-5 - 11:45 a.m.

RaM-SAR: A Low Energy and Area Overhead, 11.3fJ/conv.-step 12b 25MS/s Secure Random-Mapping SAR ADC with Power and EM Side-channel Attacks Resilience, R. Chen, H. Wang, A. Chandrakasan, H-S Lee, Massachusetts Institute of Technology

Session C11 - Honolulu 3
Wireless, Phased Arrays
Wednesday, June 15

Co-Chairs: N. Kocaman, Broadcom
K. Matsunaga, NTT Corp.

C11-1 - 10:05 a.m.
A 28-GHz Fully-Passive Retro-Reflective Phased-Array Backscattering Transceiver for 5G Network with 24-GHz Beam-Steered Wireless Power Transfer, M. Ide, Y. Keito, S. Kato, D. You, A. A. Fadila, J. Pang, A. Shirane, K. Okada, Tokyo Institute of Technology

C11-2 - 10:30 a.m.
A 39-GHz CMOS Bi-Directional Doherty Phased-Array Beamformer Using Shared-LUT DPD with Inter-Element Mismatch Compensation Technique for 5G Base-Station, Z. Li, J. Pang, Y. Zhang, Y. Yamazaki, Q. Wang, P. Luo, W. Chen, Y. Liao, M. Tang, Z. Guo, Y. Wang, X. Fu, D. You, N. Oshima*, S. Hori*, , K. Kunihiro*, A. Shirane, K. Okada, Tokyo Institute of Technology, *NEC Corporation

C11-3 - 10:55 a.m.
A 30GHz-BW <-57dB-IM3 Direct RF Receiver Analog Front End in 16nm FinFET, A. Ramkaj, A. Cantoni*, G. Manganaro*, S. Devarajan*, M. Steyaert, F. Tavernier, KU Leuven, Belgium, *Analog Devices Inc.

C11-4 - 11:20 a.m.
An Ultra-compact Bidirectional T/R Folded 25.8-39.2GHz Phased-Array Transceiver Front-End with Embedded TX Power Detection/Self-calibration Path Supporting 64- /256-/512-QAM at 28-/39-GHz band for 5G in 65nm CMOS Technology, W. Zhu, J. Zhang, Tsinghua University

C11-5 - 11:45 a.m.
Fully Integrated 2x2 MIMO Real Simultaneous Dual Band WiFi CMOS Power Amplifiers With a Single Inductor Multiple Output Supply Modulation Technique, J-S Paek, J-K Lee, W. Kim, J-S Bang, J. Lee, Samsung Electronics

Session T5 - Tapa 3
Selectors and Devices with Oxide Semiconductor Channels
Wednesday, June 15

Co-Chairs: A. Agraval, Intel
R. Tsuchiya, Hitachi, Ltd.

T05-1 - 1:30 p.m.
Improving the SiGeAsTe Ovonic Threshold Switching (OTS) Characteristics by Microwave Annealing for Excellent Endurance (>10^{11}) and Low Drift Characteristics, J. Lee, S. Kim, S. Lee, S. Ban, S. Heo, D. Lee, O. Mosendz*, H. Hwang, POSTECH, *Western Digital Corporation

T05-2 - 1:55 p.m.

Thermal Studies of BEOL-compatible Top-Gated Atomically Thin ALD In_2O_3 FETs, P-Y Liao, S. Alajlouni, M. Si, Z. Zhang, Z. Lin, J. Noh, C. Wilk*, A. Shakouri, P. Ye, Purdue University, *BASIS Scottsdale

T05-3 - 2:20 p.m.
First Fire-free, Low-voltage (~1.2 V), and Low Off-current (~3 nA) SiO_xTe_y Selectors, S. Vaziri, I. Datye, E. Ambrosi, A. Khan*, H. Kwon*, Stanford University, C-H Wu, C-F Hsu, J. Guy, T. Lee, H-S P. Wong*, X. Bao, TSMC, * Stanford University

T05-4 - 2:45 p.m.
Sub-10nm Ultra-thin ZnO Channel FET with Record-High 561 µA/µm I_{ON} at V_{DS} of 1V, High µ-84 cm^2/V-s and1T-1RRAM Memory Cell Demonstration with Embedded Memory Implications for Energy- Efficient Deep-Learning Computing, U. Chand, M. Sabry Aly*, M. Lal, C-K Chen, S. Hooda, S-H Tsai, Z. Fang, H. Veluri, A.V-Y Thean*, National University of Singapore, *Nanyang Technological University

Session T6 - Tapa 2
Monolithic Integration and Cryoelectronics
Wednesday, June 15

Co-Chairs: M. Vinet, CEA-LETI
Y. Yamamoto, Renesas Electronics Corp.

T06-1 - 1:30 p.m.
3D stackable cryogenic InGaAs HEMTs for heterogeneous and monolithic 3D integrated highly scalable quantum computing systems, J. Jeong, S. K. Kim, J. Kim*, D-M Geum, J. Lee**, S-Y Park**, S. Kim, KAIST, *KANC, **KBSI

T06-2 - 1:55 p.m.
Demonstration of 3D sequential FD-SOI on CMOS FinFET stacking featuring low temperature Si layer transfer and top tier device fabrication with tier interconnections, A. Vandooren, N. Parihar, J. Franco, R. Loo, H. Arimura, R. Rodriguez, F. Sebaai, S. Iacovo, K. Vandersmissen, W. Li, G. Mannaert, D. Radisic, E. Rosseel, A. Hikavyy, A. Jourdain, O. Mourey*, G. Gaudin*, G. Besnard*, C. Roda Neve*, B-Y Nguyen*, I. Radu*, E. Dentoni Litta, N. Horiguchi, imec, * SOITEC

T06-3 - 2:20 p.m.
Methodology for Active Junction Profile Extraction in thin film FD-SOI Enabling performance driver identification in 500°C devices for 3D sequential integration, T. Frutuoso, X. Garros, P. Batude, B. Laurent, J. Lacord, B. Sklenard, V. Lapras, C. Fenouillet-Beranger, M. Ribotta , A. Magalhaes-Lucas, J. Kanyandekwe, R. Kies, G. Romano, E. Catapano, M. Casse, J. Lugo-Alvarez, P. Ferrari*, F. Gaillard, CEA, Leti, Minatec Campus, and University Grenoble Alpes, *University Grenoble Alpes, Grenoble INP, RFIC-Lab

T06-4 - 2:45 p.m.
Effect of Conduction Band Edge States on Coulomb-Limiting Electron Mobility in Cryogenic MOSFET Operation, H. Oka, T. Inaba, S. Iizuka, H. Asai, K. Kato, T. Mori, National Institute of Advanced Industrial Science and Technology

Session C12 - Tapa 1
ML and Vision
Wednesday, June 15

Co-Chairs: Z. Zhang, Univ. Michigan
Y. Sasagawa, Socionext

C12-1 - 1:30 p.m.
A Sparse Convolution Neural Network Accelerator for 3D/4D Point-Cloud Image Recognition on Low Power Mobile Device with Hopping-Index Rule Book for Efficient Coordinate Management, Q. Cao, J. Gu, Northwestern University

C12-2 - 1:55 p.m.
***i*-FlatCam: A 253 FPS, 91.49 µJ/Frame Ultra-Compact Intelligent Lensless Camera for Real-Time and Efficient Eye Tracking in VR/AR,** Y. Zhao, Z. Li*, Y. Fu, Y. Zhang, C. Li, C. Wan, H. You, S. Wu, X. Ouyang, V. Boominathan, A. Veeraraghavan, Y. Lin, Rice University, *Facebook Reality Labs

C12-3 - 2:20 p.m.
A 135.6Tbps/W 2R2W SRAM with 12T Logic Bit-cell with Vmin Down to 335mV Targeted for Machine-Learning Applications in 6nm FinFET CMOS Technology, N. E. C. Akkaya, G. Chan, H. Liao, Y. Wang, J. Chang, TSMC

C12-4 - 2:45 p.m.
Gain-Cell CIM: Leakage and Bitline Swing Aware 2T1C Gain-Cell eDRAM Compute in Memory Design with Bitline Precharge DACs and Compact Schmitt Trigger ADCs, S. Xie, C. Ni, P. Jain*, F. Hamzaoglu*, J. Kulkarni, The University of Texas at Austin, * Intel Corporation

Session C13 - Honolulu 1
Sensors and Sensor Interfaces
Wednesday, June 15

Co-Chairs: D. Griffith, Texas Instruments
M. Je, KAIST

C13-1 - 1:30 p.m.
A 2.54µJ·ppm^2-FOM$_S$ Supply- and Temperature-Independent Time-Locked Δσ Capacitance-to-Digital Converter in 0.18-µm CMOS, S. Baik, T. Seol, S. Lee, G. Kim, S. Cho, KAIST, A. K. George, J. Lee, DGIST

C13-2 - 1:55 p.m.
An Impedance-boosted Switched-capacitor Low-noise Amplifier Achieving 0.4 NEF, G. Atzeni, R. Incandela, Y. Ji, A. Novello, H. Ghiasi, G. Cristiano, J. Liao, Q. Huang, T. Jang, ETH Zurich

C13-3 - 2:20 p.m.
A 90.9kS/s, 0.7nJ/conversion Hybrid Temperature Sensor in 4nm-class CMOS, Y. Li, D. Duarte, Y. Fan, Intel Corporation

C13-4 - 2:45 p.m.

A 210nW BJT-based Temperature Sensor with an Inaccuracy of ±0.15°C (3σ) from -15°C to 85°C, T. Someya, V. van Hoek, J. Angevare, S. Pan, K. Makinwa, Delft University of Technology

Session C14 - Honolulu 2
Circuits Joint Focus Session -Advanced Wireless
Wednesday, June 15

Co-Chairs: G. Hueber, Silicon Austria Labs
N. Kocaman, Broadcom

C14-1 - 1:30 p.m.
InP HBT Technologies for sub-THz Communications (Invited), to be announced

C14-2 - 1:55 p.m.
High Efficiency 29-/38-GHz Hybrid Transceiver Front-Ends Utilizing Si CMOS and GaAs HEMT for 5G NR Millimeter-Wave Mobile Applications, Y. Kim, H. Park, I. Lee, J. Hur, S. Yoo, Samsung Electronics

C14-3 - 2:20 p.m.
5G mmWave Power Amplifier and Low-Noise Amplifier in 300mm GaN-on-Si Technology, Q. Yu, H. W. Then, D. Thomson, J. Chou, J. Garrett, I. Huang, I. Momson, S. Ravikumar, S. Hwangbo, A. Latorre-Rey, A. Roy, M. Radosavljevic, M. Beumer, P. Koirala, N. Thomas, N. Nair, H. Vora, S. Bader, J. Rode, J. Jensen, S. Rami, Intel Corporation

C14-4 - 2:45 p.m.
A Packaged 90-to-96GHz 16-Element Phased Array with 18.8/15.8dBm Psat/OP1dB, 14.8% TX PAE in 65nm CMOS Process and +51dBm Array EIRP, W. Zhu, J. Zhang, Tsinghua University

Session C15 - Honolulu 3
Memory
Wednesday, June 15

Co-Chairs: S. Kang, Qualcomm Technologies
K. Miyano, Micron Memory Japan

C15-1 - 1:30 p.m.
A 16 GB 1024 GB/s HBM3 DRAM with On-Die Error Control Scheme for Enhanced RAS Features, Y. Ryu, Y-C Kwon, J. H. Lee, S-g Ahn, J. Park, K. Lee, Y. H. Choi, H-W Cho, J. S. Kim, J. Lee, H. Lee, S. H. Song, J. M. Ryu, Y. H. Yun, U. Shin, D. Cho, J. H. Park, J-S Jeong, S. Lee, K-H Lim, T-S Kim, K. Kim, Y. J. Cha, I. J. Lee, T. K. Byun, H. S. Yoo, Y. G. Song, M-K Lee, S. Cho, S-R Kim, J-M Choi, H. M. Kim, S. Y. Kim, J. Youn, M-O Kim, K. Sohn, S. Hwang, J. Lee, Samsung Electronics

C15-2 - 1:55 p.m.
A 32Mb Embedded Flash Memory based on 28nm with the best Cell Efficiency and Robust Design achievement featuring 13.48Mb/mm² at 0.85V, H. Shin, S. Won, D. Kim, B. Choi, G. Kim, M. Oh, J. Choi, J. Kye, Samsung Electronics

C15-3 - 2:20 p.m.

A 22nm 32Mb Embedded STT-MRAM Macro Achieving 5.9ns Random Read Access and 5.8MB/s Write Throughput at up to Tj of 150 °C, T. Shimoi, K. Matsubara, T. Saito, T. Ogawa, Y. Taito, Y. Kaneda, M. Izuna, K. Takeda, H. Mitani, T. Ito, T. Kono, Renesas Electronics

C15-4 - 2:45 p.m.

A High Output Power 1V Charge Pump and Power Switch for Configurable, In-Field-Programmable Metal eFuse on Intel 4 Logic Technology, S. Hutchins, J. Li, A. Sanne, U. Ikram, Z. Chen, M. M. Hasan, U. Bhattacharya, E. Karl, J. P. Kulkarni*, Intel Corporation, *The University of Texas at Austin

Session T7 - Tapa 3
Ferroelectrics for Memory and Logic Applications
Wednesday, June 15

Co-Chairs: F. Arnaud, ST Microelectronics
M. Kobayashi, The University of Tokyo

T07-1 - 3:25 p.m.
Machine Learning Assisted Statistical Variation Analysis of Ferroelectric Transistors: From Experimental Metrology to Predictive Modeling, G. Choe, P. Ravindran, A. Lu, J. Hur, M. Lederer*, A. Reck*, S. Lombardo, N. Afroze, J. Kacher, A. Khan, S. Yu, Georgia Institute of Technology, *Fraunhofer IPMS

T07-2 - 3:50 p.m.
Determination of Domain Wall Velocity and Nucleation Time by Switching Dynamics Studies of Ferroelectric Hafnium Zirconium Oxide, X. Lyu, P. Shrestha*, M. Si, P. Wang**, J. Li, K. Cheung*, S. Yu**, P. Ye, Purdue University, *National Institute of Standards and Technology, **Georgia Institute of Technology

T07-3 - 4:15 p.m.
Insight to Data Retention loss in ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ pFET and nFET from simultaneous PV and IV measurements, M. N. K. Alam, Y. Higashi*, B. Truijen, B. Kaczer*, M. Popovici*, B. OHSullivan*, P. Roussel*, R. Degraeve*, M. Heyns^, J. Van Houdt**, imec, *Kioxia Corporation, ^KU Leuven

T07-4 - 4:40 p.m.
Atomic visualization of the emergence of orthorhombic phase in $Hf_{0.5}$ Z $_{0.5}O_2$ ferroelectric film with in-situ rapid thermal annealing, T. Xin, Y. Zheng, Y. Cheng, K. Du*, Y. Wang, Z. Gao, D. Su*, Y. Zheng, Q. Zhong, C. Liu, R. Huang, C. Duan, S. Song**, Z. Song**, H. Lyu, East China Normal University, *Huawei Technologies Co., **Shanghai Institute of Microsystem and Information Technology

Session T8 - Tapa 2
Image Sensors and Displays
Wednesday, June 15

Co-Chairs: M. Schulaker, Massachusetts Institute of Technology
R. Kuroda, Tohoku University

T08-1 - 3:25 p.m.
First Demonstration of High-Sensitivity (NEP<1fW·Hz$^{-1/2}$) Back-Illuminated Active-Matrix Deep UV Image Sensor by Monolithic Integration of Ga2O3 Photodetectors and Oxide Thin-Film-Transistors, Y. Qin, C. Lu, Z. Yu, Z. Yao, F. Wu*, D. Dong, X. Zhao*, G. Xu*, Y. Zhang**, S. Long*, L. Li, M. Liu, Institute of Microelectronics of Chinese Academy of Sciences, *University of Science and Technology of China, **Virginia Polytechnic Institute and State University

T08-2 - 3:50 p.m.
Low-Noise Multi-Gate Pixel Transistor for Sub-Micron Pixel CMOS Image Sensors, S. Kitamura, N. Kimizuka, A. Honjo, K. Baba, T. Kurobe, H. Kumano, T. Toyofuku, K. Takeuchi*, S. Nishimura*, A. Kato, T. Hirano, Y. Oike, Sony Semiconductor Solutions Corporation, Sony Semiconductor Manufacturing Corporation

T08-3 - 4:15 p.m.
Wafer Level Pixelation of Colloidal Quantum Dot Image Sensors, Y. Li, G. Karve, P. Malinowski, J. H. Kim, E. Georgitzikis, V. Pejović, M-J Lim, L. Moreno Hagelsieb, R. Puybaret, I. Lieberman, J. Lee, D. Cheyns, P. Heremans, H. Osman, D. Sabuncuoglu Tezcan, imec

T08-4 - 4:40 p.m.
A 0.6μm Small Pixel for High Resolution CMOS Image Sensor with Full Well Capacity of 10,000e- by Dual Vertical Transfer Gate Technology, J. Yun, S. Lee, S. Cha, J. Kim, J. Lee, H. Kim, E. Lee, S. Kim, S. Hong, H. Kim, J. Huh, S. Kim, K. Kakehi, J-H Kim, J-M Koo, E. Cho, H. Jeong, H. Park, K. Lee, J. Ahn, J. Yim, Samsung Electronics

T08-5 - 5:05 p.m.
Advanced novel optical stack technologies for high SNR in CMOS Image Sensor, H. Y. Park, Y. Lee, J. Park, H. song, T. Lee, H. K. Gweon, Y. Jung, J. Bae, B. Kim, J. Han, S. Kim, C. Yoon, J. Kim, C. Lee, S. Yoo, E. kim, H. Baek, H. Park, B. Kim, J. Ahn, J. Yim, Samsung Electronics

Joint Session - Tapa 1
Cryo CMOS
Wednesday, June 15

Co-Chairs: B. Staszewski, Univ. College Dublin

J1-1 - 3:25 p.m.
A 3V 15b 157μW Cryo-CMOS DAC for Multiplexed Spin-Qubit Biasing, L. Enthoven, J. van Staveren, J. Gong, M. Babaie, F. Sebastiano, Delft University of Technology

J1-2 - 3:50 p.m.
Scalable 1.4 μW cryo-CMOS SP4T multiplexer operating at 10 mK for high-fidelity superconducting qubit measurements, R. Acharya, A. Potočnik*, S. Brebels. Grill*, J. Verjauw, T. Ivanov*, D. Lozano*, D. Wan*, F. A. Mohiyaddin*, J. van Damme, A. M. Vadiraj*, M. Mongillo*, G. Gielen, F. Catthoor*, J. Craninckx*, I. Radu**, B. Govoreanu*, KU Leuven, *imec, **TSMC

J1-3 - 4:15 p.m.
A 0.31V Vmin Cryogenic SRAM in 14 nm FinFET for Quantum Computing, R. Joshi, J. Timmerwilke*, K. Tien*, M. Yeck*, S. Chakraborty*, IBM Thomas J. Watson Research Center, *IBM

J1-4 - 4:40 p.m.
A Cryogenic CMOS Current Comparator for Spin Qubit Readout Achieving Fast Readout Time and High Current Resolution, H. Fuketa, I. Akita, T. Ishikawa, H. Koike, T. Mori, National Institute of Advanced Industrial Science and Technology

J1-5 - 5:05 p.m.
13-K T_{noise} Cryo-CMOS Parametric Amplifier at 80 mK for Quantum Computers, G. Baek, S. Bae, M. Lee, H. Park, K. Lee, J-Y Sim, M. Lee, H-J Song, Pohang University of Science and Technology

Session C16 - Honolulu 1
Hardware Security
Wednesday, June 15

Co-Chairs: C. Tokunaga, Intel
N. Miyura, Osaka University

C16-1 - 3:25 p.m.
A 7Gbps SCA-Resistant Multiplicative-Masked AES Engine in Intel 4 CMOS, R. Kumar, V. Suresh, S. Taneja, M. Anders, S. Hsu, A. Agarwal, V. De, , S. Mathew, Intel

C16-2 - 3:50 p.m.
On-Chip Laser Voltage Probing Attack Detection with 100% Area Coverage at Above/Below the Bandgap Wavelength and Fully-Automated Design, H. Zhang, L. Lin*, Q. Fang, M. Alioto, National University of Singapore, *Southern University of Science and Technology

C16-3 - 4:15 p.m.
An Automotive ASIL-D Safety Mechanism in ADC and DAC for Communication Application, K. Lee, J. Park, Y. Park, B. Koo, S. Do, W. Lim, S. Lee, H. Shin, E. Oh, Y. Cho, M. Choi, J. Shin, Samsung Electronics

C16-4 - 4:40 p.m.
Fully-Digital Broadband Calibration-Less Impedance Monitor for Probe Insertion Detection against Power Analysis Attacks, V. Konandur Rajanna, H. Raghav, T. Wang, M. Alioto, National University of Singapore

C16-5 - 5:05 p.m.
An FLL-Based Clock Glitch Detector for Security Circuits in a 5nm FINFET Process, S. Song, S. Tell, B. Zimmer, S. Kudva, N. Nedovic, C. Gray, NVIDIA

Session C17 - Honolulu 2
Advanced Wireline and Memory Interfaces
Wednesday, June 15

Co-Chairs: I. Arsovski, Groq
K. Sohn, Samsung

C17-1 - 3:25 p.m.

A 40-Gb/s/pin Low-Voltage POD Single-Ended PAM-4 Transceiver with Timing Calibrated Reset-less Slicer and Bidirectional T-Coil for GDDR7 Application, H. N. Rie, C. S. Yoon, J. Byun, S. Lee, G. Kim, J. Kim, J. Park, H. Cho, Y. Um, H. Jin, K. Shin, M. Jung, G-E Cha, Y. Kim, Y. Kim, B. Han, Y. Jeon, J. Lee, E. Shin, H-J Kwon, Y. Choi, J-H Choi, H. Ko, Samsung Electronics

C17-2 - 3:50 p.m.
A 68.7-fJ/b/mm 375-GB/s/mm Single-Ended PAM-4 Interface with Per-Pin Training Sequence for the Next-Generation HBM Controller, J-H Park, K-H Lee, Y. Lee, J-W Sull, Y. Song, S. Lee, H. Lee, H. Cho, J. Oh, Columbia University, H-G Ko, ONEsemiconductor, D-K Jeong, Seoul National University

C17-3 - 4:15 p.m.
A Low Power TSV I/O with Data Rate up to 10 Gb/s for Next Generation HBM, J-Y Kim, T. Kim, J. You, K. Kim*, B. M. Moon*, Samsung Electronics Co., Ltd., K. Sohn*, S-O Jung, VLSI system Lab, Yonsei University, * Samsung Electronics Co., Ltd.,

C17-4 - 4:40 p.m.
A 0.297-pJ/bit 50.4-Gb/s/wire Inverter-Based Short-Reach Simultaneous Bidirectional Transceiver for Die-to-Die Interface in 5nm CMOS, Y. Nishi, CA, J. Poulton, NVIDIA, X. Chen, CA, S. Song, CA, B. Zimmer, CA, W. Turner, S. Tell, N. Nedovic, J. Wilson, W. Dally, C. Gray, NVIDIA

C17-5 - 5:05 p.m.
A 25.78125Gbps Bi-directional Transceiver with Framed-Pulsewidth Modulation (FPWM) for Extended Reach Optical Links in 28nm CMOS, W. Kwon, H. Won*, T. Kim*, H. Choi, H-I Song*, S. Jeon**, S-W Kwon**, H. Jin*, J-G Jo*, T-Y Kim*, J. Eu*, J. Park*, H-M Bae, KAIST, *Point2 Technology, **Samsung Electronics

Session C18 - Honolulu 3
Power and Analog
Wednesday, June 15

Co-Chairs: X. Zhang, IBM
M. Takamiya, University of Tokyo

C18-1 - 3:25 p.m.
A 286nW, 103V High Voltage Generator and Multiplexer for Electrostatic Actuation in Programmable Matter, Y. Peng, G. Carichner, Y. Kim, L-Y Chen, R. Tribhout*, B. Piranda*, J. Bourgeois*, D. Blaauw, D. Sylvester, University of Michigan, Ann Arbor, *FEMTO-ST Institute

C18-2 - 3:50 p.m.
A Shared-Inductor Structure-Reconfigurable Regulating Rectifier (SR-RR) Enabling 6.78-MHz AC-DC Rectification and 1-MHz DC-DC Energy Recycling, F-B Yang, D-H Yao, P-H Chen, National Yang Ming Chiao Tung University

C18-3 - 4:15 p.m.
A Scalable Standing-Wave-Oscillator-based Imager with Near-Field-Modulated Pixels Achieving 64% Filling Factor for RF Intraoperative Imaging, J-C Chien, Z-J Cheng, S-Y Chuang, H-C Yeh, G-Y Huang, H-Y Hou, Y-T Chen, W-Y Weng, C-Y Tseng, L-I Lin, National Taiwan University

C18-4 - 4:40 p.m.
A 0.4mm^3 Battery-Less Crystal-Less Neural-Recording SoC Achieving 1.6cm Backscattering Range with 2mm×2mm On-Chip Antenna, C. Yang, B. Zhao, Y. Zhang, Z. Chang, Z. Li, T. Zheng, Y. Luo, S. Zhang, K. Xu, G. Pan, Zhejiang University

C18-5 - 5:05 p.m.
Palm-sized LiDAR module with III/V-on-Si optical phased array, K. Son, D. Shin, J. Lee, B. Jang, D. Shim, H. Byun, C. Lee, Y. Cho, T. Otsuka, C. Shin, I. Hwang, E. K. Lee, K. Ha, H. Choo, Samsung

Session T9 - Tapa 3
Ferroelectric Memory
Thursday, June 16

Co-Chairs: S. Yu, Georgia Tech
S. Fujii, Kioxia Corp.

T09-1 - 8:10 a.m.
Memory Array Demonstration of fully integrated 1T-1C FeFET concept with separated ferroelectric MFM device in interconnect layer, K. Seidel, D. Lehninger, R. Hoffmann, T. Ali, M. Lederer, Fraunhofer IPMS, R. Revello, K. Mertens, K. Biedermann, Y. Shen, D. Wang, M. Landwehr, Fraunhofer IPMS, A. Heinig, Fraunhofer IPMS, T. Kämpfe, H. Mähne*, * K. Bernert*, S. Thiem*, Center Nanoelectronic Technologies, Fraunhofer IPMS, *XFAB Dresden GmbH & Co. KG

T09-2 - 8:35 a.m.
Experimental Demonstration of An Inversion-Type Ferroelectric Capacitive Memory and its 1 kbit Crossbar Array Featuring High CHCS/CLCS, Fast Speed, and Long Retention, Z. Zhou, L. Jiao, J. Zhou, Z. Zheng, Y. Chen, K. Han, Y. Kang, X. Gong, National University of Singapore

T09-3 - 9:00 a.m.
NVDimm-FE: A High-density 3D Architecture of 3-bit/c 2TnC$_{FE}$ to Break Great Memory Wall with 10 ns of PGM-pulse, 10^{10} Cycles of Endurance, and Decade Lifetime at 103 °C, E. R. Hsieh, J. Chang*, * T. Y. Tang, Y. J. Li*, J. C. Guo*, S. S. Chung*, National Central University, *National Yang Ming Chiao Tung University

T09-4 - 9:25 a.m.
Interfacial-Layer Design for Hf$_{1-x}$Zr$_x$O$_2$-Based FTJ Devices: From Atom to Array, T. Chen, H-L Chiang, J-F Wang, K-H Lin*, C-H Nien, J-J Wu, K-Y Hsiang**, C-P Chuu, Y-W Chen***, X. Zhang***, C. W. Liu***, T. Wang**, C-C Wang*, M-H Lee^, M-F Chang, C-S Chang, TSMC, *Synopsys Taiwan Co. Ltd., **NYCU, ***NTU, ^NTNU

Joint Focus Session 1 - Tapa 2
Memory Technologies and Circuits for CIM
Thursday, June 16

Co-Chairs: G. Bronner, Rambus
H. Wu, Tsinghua University

JFS1-1 – 8:10 a.m.
Computing-in-Memory with SuperFlash® memBrain™ Technology (Invited), N. Do, H. Tran, M. Reiten, Microchip Technology

JFS1-2 - 8:35 a.m.
BEOL Compatible Ferroelectric Routers for Run-time Reconfigurable Compute-in-Memory Accelerators, A. Khanna, H. Ye, Y. Luo*, G. Bajpai, M. San Jose, W. Chakraborty, S. Yu*, P. Fay, S. Datta, University of Notre Dame, *Georgia Institute of Technology

JFS1-3 - 9:00 a.m.
A Thousand State Superlattice(SL) FEFET Analog Weight Cell, K. A. Aabrar, S. G. Kirtania, A. Lu*, A. Khanna, W. Chakraborty, M. San Jose, S. Yu*, S. Datta, University of Notre Dame, *Georgia Institute of Technology

JFS1-4 - 9:25 a.m.
4 Bits/cell Hybrid 1F1R for High Density Embedded Non-Volatile Memory and its Application for Compute in Memory, W-C Chen, F. Huang, S. Qin, Z. Yu, Q. Lin, P. McIntyre, S. S. Wong, H-S P. Wong, Stanford University

Session C19 - Tapa 1
Time-Interleaved ADCs
Thursday, June 16

Co-Chairs: R. Kapusta, Analog Devices
S. Kondo, Toshiba Corp.

C19-1 - 8:10 a.m.
An 8-bit 56GS/s 64x Time-Interleaved ADC with Bootstrapped Sampler and Class-AB Buffer in 4nm CMOS, A. Yonar, P. Francese, M. Braendli, M. Kossel, T. Morf, J. Proesel, S. Rylov, H. Ainspan, M. Cochet, Z. Deniz, T. Dickson, T. Beukema, C. Baks, M. Beakes, J. Bulzacchelli, Y-H Choi*, B-J Yoo*, H. Ahn*, D-H Lim*, G. Kang*, S-H Park*, M. Meghelli, H-G Rhew*, D. Friedman, M. Choi*, M. Soyuer, IBM Research, J. Shin*, *Samsung Electronics

C19-2 - 8:35 a.m.
A 6.0mW 3.8GS/s 7b VTC/TDC-Assisted Interleaved SAR ADC with 13GHz ERBW, A. Whitcombe, C. Lee*, A. Kuriparambil Thekkumpate, S. Kundu*, J. Timbadiya, A. Agrawal, B. Carlton, P. Sagazio, S. Pellerano, C. Hull, Intel Labs, *Nebula Microsystems

C19-3 - 9:00 a.m.
A 12-bit 10GS/s 16-Channel Time-Interleaved ADC with a Digital Processing Timing-Skew Background Calibration in 5nm FinFET, K-J Moon, D-R Oh, Y-H Park, K-H Lee, S-J Park, S-N Lee, H-C Hwang, H-C Shin, Y-J Cho, M. Choi, J-S Shin, Samsung Electronics

C19-4 - 9:25 a.m.
A Relative-Prime Rotation Based Fully On-Chip Background Skew Calibration for Time-Interleaved ADCs, D-J Chang, S-T Ryu, KAIST

Session C20 - Honolulu 1

Power Conversion 1
Thursday, June 16

Co-Chairs: P. Mercier, Univ. California, San Diego
S.-W. Hong, Sogang University

C20-1 - 8:10 a.m.
A 90.4% Peak Efficiency 48V/1V Three-Level Hybrid Dickson Converter with Gradient Descent Run-Time Optimizer and GaN/Si Hybrid Conversion, M. Gong, X. Zhang*, A. Raychowdhury, Georgia Institute of Technology, *IBM

C20-2 - 8:35 a.m.
A 90.7% 4-W 3P4S Hybrid Switching Converter Using Adaptive V_{CF} Rebalancing Technique and Switching Node Dual-Edge tdead Modulation for Extreme 48V/1V Direct DC-DC Conversion, Y. Huang, Y. Ramadass*, D. B. Ma, The University of Texas at Dallas, * Texas Instruments,

C20-3 - 9:00 a.m.
A 5.6W-Power 96.6%-Efficiency Boost-Oriented SIDO Step-Up/Down DC-DC Converter Embedding Buck Conversion with an Energy-Balancing Capacitor, G-G Kang, J-H Lee, S-U Shin*, G-H Cho, H-S Kim, KAIST, *UNIST

C20-4 - 9:25 a.m.
A Monolithic 48V-to-1V 10A Quadruple Step-Down DC-DC Converter with Hysteretic Copied On-Time 4-Phase Control and 2× Slew Rate All-Hysteretic Mode, H. Han, M-W Ko, J-H Cho, G-G Kang, S-T Koh, H-H Bae, H-S Kim, KAIST

Joint Focus Session 2 - Honolulu 2
Biomedical
Thursday, June 16

Co-Chairs: C. Mora Lopez, imec

JFS2-1 - 8:10 a.m.
A Wireless Urine Detection System and Platform with Power-Efficient Electrochemical Readout ASIC and ABTS-CNT Biosensor (Invited), S-Y Lee, H-Y Lee, D-S Ciou, Z-X Liao, P-W Huang, Y-T Hsieh, Y-C Wei, C-Y Lin, M-D Shieh J-Y Chen, National Cheng Kung University

JFS2-2 - 8:35 a.m.
A 90-µW Penny-Sized 1.2-gram Wireless EEG Recorder with 12-Channel FDMA Transmitter for Month-Long Continuous Mental Health Monitoring, C. Chen, J. Yang, H. Wang, Z. Cao, , S. Kananian, K. Chen, A. Poon, Stanford University

JFS2-3 - 9:00 a.m.
A Galvanically Coupled Electron Paramagnetic Resonance Spectrometer for Deep Tissue Hypoxia Diagnosis, L. Zhang, UC Berkeley, A. Niknejad, UC Berkeley

JFS2-4 - 9:25 a.m.

e-G2C: A 0.14-to-8.31 µJ/Inference NN-based Processor with Continuous On-chip Adaptation for Anomaly Detection and ECG Conversion from EGM, Y. Zhao, Y. Zhang, Y. Fu, X. Ouyang, C. Wan, S. Wu, A. Banta, M. John*, A. Post*, M. Razavi*, J. Cavallaro, B. Aazhang, Y. Lin, Rice University, *Texas Heart Institute

Session T10 - Tapa 3
Advanced CMOS Devices and Technology
Thursday, June 16

Co-Chairs: S-C Song, Qualcomm
Y. Masuoka, Samsung Electronics Co., Ltd.

T10-1 - 10:05 a.m.
Standard Cell Design Optimization with Advanced MOL Technology in 3nm GAA Process, G. Yang, H. Jung, J. Lim, J. Seo, I. Kim, J. Yu, H. You, J. Kong, G. Kim, M. Jung, C. Park, S. An, W. Rim, H. Kim, D. Lee, S. Baek, J. Jung, T. Song, J. Kye, Samsung Electronics

T10-2 - 10:30 a.m.
PPAC of sheet-based CFET configurations for 4 track design with 16nm metal pitch, P. Schuddinck, F. Bufler, Y. Xiang, A. Farokhnejad, G. Mirabelli, A. Vandooren, B. Chehab, A. Gupta, C. Roda-Neve, SOITEC, G. Hellings, J. Ryckaert, imec

T10-3 - 10:55 a.m.
300 mm Wafer-scale *In-situ* CVD Growth Achieving 5.1×10^{-10} Ω-cm^2 P-Type Contact Resistivity: Record 2.5×10^{21} cm^{-3} Active Doping and Demonstration on Highly-Scaled 3D Structures, H. Xu, R. Khazaka*, J. Zhang, Z. Zheng, Y. Chen, X. Gong, National University of Singapore, * ASM

T10-4 - 11:20 a.m.
Comprehensive Feasibility Study of Single FIN Transistors for Scaling Both Switching Energy and Device Footprint, H. Fukutome, K. S. Suh, W. Kim, Y. Moriyama, S. Kang, B. Eom, Y. Kim, J. Kim, C. Yoon, W. Kwon, Y. Chung, Y. Nam, Y. Kim, S-C Park, J. Park, H-J Cho, K. Rim, S. Kwon, Samsung

T10-5 - 11:45 a.m.
Self-Heating in iN8-iN2 CMOS Logic Cells: Thermal Impact of Architecture (FinFET, Nanosheet, Forksheet and CFET) and Scaling Boosters, B. Vermeersch, E. Bury, Y. Xiang, P. Schuddinck, K. Bhuwalka*, G. Hellings, J. Ryckaert, imec, *Huawei Technologies R&D

Joint Focus Session 3 - Tapa 2
3D Heterogenous Integration
Thursday, June 16

Co-Chairs: M. Kanda, Toshiba Electronic Devices & Storage Corp.
P. Whatmough, ARM

JFS3-1 - 10:05 a.m.
Unleash Scaling Potential of 3D NAND with Innovative Xtacking® Architecture (Invited), Z. Huo, W. Cheng, S. Yang, Yangtze Memory Technologies Co., Ltd.

JFS3-2 - 10:30 a.m.

(Why do we need) Wireless Heterogeneous Integration (anyway?) (Invited), to be announced

JFS3-3 - 10:55 a.m.
SoIC_H Technology for Heterogenous System Integration, C-T Wang, C-C Lin, C-H Lu, W-T Chen, C-H Tsai, D. C. Yu, TSMC

JFS3-4 - 11:20 a.m.
5.12 Tbps Co-Packaged FPGA and Silicon Photonics Interconnect I/O, K. Hosseini, E. Kok, S. Y. Shumarayev, D. Jeong*, A. Chan, A. Katzin*, S. Liu*, R. Roucka*, M. Raval*, M. Mac, C-P Chiu, T. Tran, K. A. Singh, S. Raman, Y. Ke, C. Li*, L-F Yang*, P. Chao*, H. Lu*, F. Luna*, X. Li, T. T. Hoang, A. Sarkar, A. Toda, R. Mahajan, N. Deshpande, C. O'Keeffe, U. Krishnamoorthy, V. Stojanovic*, C. Madden*, C. Zhang*, M. Sysak*, P. Bhargava*, C. Sun*, M. Wade, Intel, *Ayar Labs

JFS3-5 - 11:45 a.m.
An Embedded Multi-Die Active Bridge (EMAB) Chip for Rapid-Prototype Programmable 2.5D/3D Packaging Technology, Z. Jie, L. Wei, H. Po-Tsang , L. Sih-Han , H. Tsung-Yi , W. Shih-Hsien , D. Ming-Ji , C. I-Shan , C. Wen-Chao , W. Chin-Hung , S. Shyh-Shyuan , C. Hung-Ming*, C. Kuan-Neng , L. Wei-Chung , W. Chih-I , Industrial Technology Research Institute, *National Yang Ming Chiao Tung University

Session C21 - Tapa 1
Analog
Thursday, June 16

Co-Chairs: N. Markulic, Analog Devices
T. Izuka, University of Tokyo

C21-1 - 10:05 a.m.
A 31-Feature, 80nW, 0.53mm^2 Audio Analog Feature Extractor based on Time-Mode Analog Filterbank Interpolation and Time-Mode Analog Rectification, S. Ray, P. Kinget, Columbia University

C21-2 - 10:30 a.m.
Common-mode Stable Multilevel Output Stage with EMI Reduction Feedback Loop for Class-D audio Amplifier, N. Nishimura, A. Matamura, P. Birdsong, S. Liu, A. Bandyopadhyay, M. Markova, R. Morajkar, Analog Devices

C21-3 - 10:55 a.m.
A Single-Clock-Phase Sense Amplifier Architecture with 9x Smaller Clock-to-Q Delay Compared to the StrongARM & 6.3dB Lower Noise Compared to Double-Tail, X. Lin, M. Megahed, T. Anand, Oregon State University

C21-4 - 11:20 a.m.
A 3nm GAAFET Analog Assisted Digital LDO with High Current Density for Dynamic Voltage Scaling Mobile Applications, S. Kim, H. Lee, Y. Lee, D. Lee, B. Lee, J. Jin, S. Kim, M. Noh, K. Kang, S. Kim, T. Nomiyama, J-S Paek, J. Lee, Samsung Electronics

Session C22 - Honolulu 1
Power Conversion 2

Thursday, June 16

Co-Chairs: H. Lam, Texas Instruments
K. Kanda, Fujitsu

C22-1 - 10:05 a.m.
Fully Integrated Voltage Regulators with Package-Embedded Inductors for Heterogeneous 3D-TSV-Stacked System-in-Package with 22nm CMOS Active Silicon Interposer Featuring Self-Trimmed, Digitally Controlled ON-Time Discontinuous Conduction Mode (DCM) Operat, N. Desai, H. Krishnamurthy, S. Kim, C. Schaef, S. Weng, B. Choi, W. Lambert, K. Ravichandran, J. Tschanz, V. De, Intel Corporation

C22-2 - 10:30 a.m.
A 97.6%-Efficient 1-2MHz Hysteretic Buck Converter with 7V/µs DVS-Rate Enabled by Isosceles-Triangular Shunt Current Push-Pull Technique, H-H Bae, J-H Cho, G-G Kang, Y. Park, H-S Kim, KAIST

C22-3 - 10:55 a.m.
A Fully-Integrated 0.9W/mm^2 79.1%-Efficiency 200MHz Multi-Phase Buck Converter with Flying-Capacitor-Based Inter-Inductor Current Balancing Technique, J-H Cho, H-H Bae, G-W Lim, T-H Kong*, J-H Yang*, H-S Kim, KAIST, *Samsung Electronics

C22-4 - 11:20 a.m.
A 0.7 mm^2 Power Management Unit for Implantable Electroceutical Device with a 91.4 % Peak Efficiency Buck-based Hybrid Step-up and -down MISIMO Converter, Y. Huh, C. Bae, H. Lee, S. J. Kim, Samsung Electronics

C22-5 - 11:45 a.m.
A 96.5%-Power-Efficiency Hybrid Buck-Boost Photovoltaic Energy Harvester Employing Adaptive FOCV MPPT Control for >98% MPPT Efficiency Across a 10,000× Dynamic Range, H. Phan, H. Shin, Y. Park, H. Nguyen, D. Cho, S. Ha*, C. Kim, M. Je, KAIST, New York University Abu Dhabi

Session C23 - Honolulu 2
Communication and Signal Processors
Thursday, June 16

Co-Chairs: F. Sheikh, Intel
H. Yamaguchi, Fujitsu

C23-1 - 10:05 a.m.
A 507 GMACs/J 256-Core Domain Adaptive Systolic-Array-Processor for Wireless Communication and Linear-Algebra Kernels in 12nm FINFET, K-Y Chen, C-S Yang, Y-H Sun, W Tseng, M. Fayazi, X. He, S. Feng, Y. Yue, T. Mudge, R. Dreslinski, H-S Kim, D. Blaauw, University of Michigan

C23-2 - 10:30 a.m.
A 1.1µ s 1.56Gb/s/mm^2 Cost-Efficient Large-List SCL Polar Decoder Using Fully-Reusable LLR Buffers in 28nm CMOS Technology, D. Kam, B. Y. Kong*, Y. Lee, POSTECH, *Kongju National University

C23-3 - 10:55 a.m.
Non-linear CNN-based Read Channel for Hard Disk Drive with 30% Error Rate Reduction and Sequential 200Mbits/second Throughput in 28nm CMOS, Y. Qin, R. Purdy, A. Probst, C-Y Lin, J-G Zhu, Carnegie Mellon University

C23-4 - 11:20 a.m.
NetFlex: A 22nm Multi-Chiplet Perception Accelerator in High-Density Fan-Out Wafer-Level Packaging, T. Chou, W. Tang, M. Rotaru*, C. Liu, R. Dutta*, S. Lim*, D. Ho*, S. Bhattacharya*, Z. Zhang, University of Michigan * A*STAR

C23-5 - 11:45 a.m.
NanoWattch: A Self-Powered 3-nW RISC-V SoC Operable from 160mV Photovoltaic Input with Integrated Temperature Sensing and Adaptive Performance Scaling, D. Truesdell, X. Liu, J. Breiholz, S. Gupta, S. Li, B. Calhoun, University of Virginia

Session T11 - Tapa 3
MRAM
Thursday, June 16

Co-Chairs: K. Knobloch, Infineon
T-H Hou, National Yang Ming Chiao Tung University

T11-1 - 1:50 p.m.
Accurate and Fast STT-MRAM Endurance Evaluation Using a Novel Metric for Asymmetric Bipolar Stress and Deep Learning, Z. Wei, W. Kim, Z. Wang, L. Hu, D. Jung, J. Zhang, Y. Huai, Avalanche Technology

T11-2 - 2:15 p.m.
Selective operations of multi-pillar SOT-MRAM for high density and low power embedded memories, K. Cai, S. Van Beek, S. Rao, K. Fan, M. Gupta, V. Nguyen, G. Jayakumar, G. Talmelli, S. Couet, G. Kar, imec

T11-3 - 2:40 p.m.
High speed (1ns) and low voltage (1.5V) demonstration of 8Kb SOT-MRAM array, M. Song, C-M Lee, S-Y Yang*, G. Chen*, K. Chen*, I. Wang*, Y. Hsin*, K-T Chang, C-F Hsu, S. Li*, J. Wei*, T. Lee, M. M. Chang, X. Bao, C. Diaz, S-J Lin, TSMC, *Industrial Technology Research Institute

T11-4 - 3:05 p.m.
A 4K-400K Wide Operating-Temperature-Range MRAM Technology with Ultrathin Composite Free Layer and Magnesium Spacer, M-C Hong, Y-J Chang, Y-C Hsin, L-M Liu*, K-M Chen, Y-H Su, G-L Chen, S-Y Yang, I-J Wang, S. Z. Rahaman, H-H Lee, S-C Chiu, C-Y Shih, C-Y Wang, F-M Chen, J-H Wei, S-S Sheu, W-C Lo, M-T Lin*, National Taiwan University, C-I Wu, T-H Hou**, Industrial Technology Research Institute, *National Taiwan University, **National Yang Ming Chiao Tung University

Session T12 - Tapa 2
Monolithic and Heterogenous Integration
Thursday, June 16

Co-Chairs: S. Chowdhury, Stanford Univ.
M. Takenaka, The University of Tokyo

T12-1 - 1:50 p.m.
A Wafer Scale Hybrid Integration Platform for Co-packaged Photonics using a CMOS based Optical InterposerTM, S. Venkatesan, J. Lee, S. Goh, B. Pile, D. Meerovich, J. Mo, Y. Jing, L. Soldano, B. Xu*, Z. Yu*, A-Y Thean*, Y. K. Lim*, Poet Technologies, *NUS

T12-2 - 2:15 p.m.
Monolithic 3D sequential integration realizing 1600-PPI red micro-LED display on Si CMOS driver IC, J. Park, D. Geum, W. Baek, S-h Kim, Korea Advanced Institute of Science and Technology

T12-3 - 2:40 p.m.
Low-ESL (<1 pH @ 8.5 GHz) Multi-Terminal Si Capacitor Embedded in 3D Functional Interposer for Power Delivery Network, K. Kobinata, T. Funaki, Y. Satake, H. Matsuno, S. Hidaka, S. Abe, H. Ito, C-C

Hsiao*, S. Y. Li*, Y. Kim, T. Ohba, Tokyo Institute of Technology, *Industrial Technology Research Institute

T12-4 - 3:05 p.m.
Room Temperature Cu-Cu Direct Bonding Using Wetting/Passivation Scheme for 3D Integration and Packaging, Z-J Hong, D. Liu, S-T Hsieh, H-W Hu, M-W Weng, C-I Cho, J-H Liu, H-C Cheng, K-N Chen, National Yang Ming Chiao Tung University

Session C24 - Tapa 1
Advanced SRAM Design
Thursday, June 16

Co-Chairs: J. Wuu, AMD
K. Miyano, Micron Memory Japan

C24-1 - 1:50 p.m.
Energy-Efficient High Bandwidth 6T SRAM Design on Intel 4 CMOS Technology, Y. Kim, C. Ong, A. Mahadevan Pillai, H. Jagadeesh, G. Baek, I. Rajwani*, Z. Guo, E. Karl, Advanced Design, Technology Development, Intel Corporation, *AXG, Intel Corporation

C24-2 - 2:15 p.m.
A 14-nm Low Voltage SRAM with Charge-Recycling and Charge Self-Saving Techniques for Low-Power Applications, K. Cho, G. Kim, J. Oh, K. Kim, C. Sim*, *Y. Bae, M. Kim*, S. Baeck*, T. Song*, S-O Jung, Yonsei University, *Samsung Electronics

C24-3 - 2:40 p.m.
Co-Optimization of SRAM Circuits with Sequential Access Patterns in a 7nm SoC Achieving 58% Memory Energy Reduction for AR Applications, D. Morris, H. Liu, T. Wu, H. E. Sumbul, E. Ansari, A. Barachant, J. Reid, E. Beigne, Meta

C24-4 - 3:05 p.m.
4nm Voltage Auto-Tracking SRAM Pulse Generator with Fully RC Optimized Row Auto-Tracking Write Assist Circuits, I. Lee, D. Seo, Y. Li, M. Kim, S. Baeck, Samsung Electronics Co., Ltd.

Session C25 - Honolulu 1
Beyond CMOS
Thursday, June 16

Co-Chairs: A. Loke, NXP Semiconductors
M. Yamaoka, Hitachi

C25-1 - 1:50 p.m.
Experimental demonstration of novel scheme of HZO/Si FeFET reservoir computing with parallel data processing for speech recognition, E. Nako, K. Toprasertpong, R. Nakane, M. Takenaka, S. Takagi, The University of Tokyo

C25-2 - 2:15 p.m.

3D Reservoir Computing with High Area Efficiency (5.12 TOPS/mm^2) Implemented by 3D Dynamic Memristor Array for Temporal Signal Processing, W. Sun, W. Zhang, j. Yu, Y. Li, Z. Guo, J. Lai, D. Dong, X. Zheng, F. Wang, S. Fan, X. Xu, D. Shang, M. Liu, Institute of Microelectronics, Chinese Academy of Sciences (IMECAS)

C25-3 - 2:40 p.m.
Few-shot graph learning with robust and energy-efficient memory-augmented graph neural network (MAGNN) based on homogeneous computing-in-memory, W. Zhang, S. Wang*, Y. Li, X. Xu, D. Dong, N. Jiang, F. Wang, Z. Guo, R. Fang, C. Dou, K. Ni**, Z. Wang*, D. Shang, M. Liu, Institute of Microelectronics of the Chinese Academy of Sciences, *The University of Hong Kong, **Rochester Institute of Technology

C25-4 - 3:05 p.m.
A Novel Ambipolar Ferroelectric Tunnel FinFET based Content Addressable Memory with Ultra-low Hardware Cost and High Energy Efficiency for Machine Learning, J. Luo, W. Xu, B. Fu, Z. Yu, M. Yang, Y. Li, Q. Huang, R. Huang, Peking University

Session T13 - Tapa 3
Ferroelectric Memory 2
Thursday, June 16

Co-Chairs: G. Yeric, Cerfe Labs
D. Kil, SK Hynix Semiconductor, Ltd.

T13-1 - 3:45 p.m.
Boosting the Memory Window of the BEOL-Compatible MFMIS Ferroelectric/Anti Ferroelectric FETs by Charge Injection, Z. Zheng, C. Sun, L. Jiao, D. Zhang, Z. Zhou, X. Wang, G. Liu, Q. Kong, Y. Chen, K. Ni*, X. Gong, National University of Singapore, *Rochester Institute of Technology

T13-2 - 4:10 p.m.
Ultra-Fast Operation of BEOL-Compatible Atomic-Layer-Deposited In_2O_3 Fe-FETs: Achieving Memory Performance Enhancement with Memory Window of 2.5 V and High Endurance >10^9 Cycles without VT Drift Penalty, Z. Lin, M. Si, P. Ye, Purdue University

T13-3 - 4:35 p.m.
Endurance >10^{11} Cycling of 3D GAA Nanosheet Ferroelectric FET with Stacked $HfZrO_2$ to Homogenize Corner Field Toward Mitigate Dead Zone for High-Density eNVM, C-Y Liao, K-Y Hsiang, Z-F Lou*, H-C Tseng*, C-Y Lin*, Z-X Li*, F-C Hsieh*, C-C Wang*, F-S Chang*, W-C Ray*, Y-Y Tseng**, S-T Chang***, T-C Chen^, M-H Lee, National Taiwan Normal University, **Synopsys Taiwan Co., Ltd., ***National Chung Hsing University

T13-4 - 5:00 p.m.
Asymmetric Double-Gate Ferroelectric FET to Decouple the Tradeoff Between Thickness Scaling and Memory Window, Z. Jiang, Y. Xiao*, S. Chatterjee**, H. Mulaosmanovic***, S. Duenkel***, S. Soss***, S. Beyer*, R. Joshi^, Y. Chauhan^^, H. Amrouch^^^, V. Narayanan*, K. Ni, Rochester Institute of Technology, *The Pennsylvania State University, **University of Stuttgart, ***GlobalFoundries Fab1 LLC & Co. KG, ^IBM Thomas J. Watson Research Center, ^^Indian Institute of Technology, Kanpur, ^^^University of Stuttgart

Session T14 - Tapa 2
New Channel Materials for Advanced CMOS
Thursday, June 16

Co-Chairs: N. Mahalingam, Texas Instruments
Y-C Yeo, TSMC

T14-1 - 3:45 p.m.
Lg = 130 nm GAA MBCFETs with three-level stacked $In_{0.53}Ga_{0.47}$ As nanosheets, H-B Jo, I-G Lee, J-M Baek, S. T. Lee*, S-M Choi, H-J Kim, H-S Jung, W-S Park, J-H Yoo, H-Y Lee, J-G Kim, D-Y Yun, S-W Son, D-H Ko**, T-W Kim***, H-M Kwon^, S-K Kim^^, J-G Kim^^, J. Yun^^, T. Kim^^, J. H. Lee, J-H Lee, C-S Shin*, K-S Seo*, D-H Kim, Kyungpook National University, *Korea Advanced Nano-Fab Center, **Yonsei University, ***University of Ulsan, ^Polytech, ^^QSI

T14-2 - 4:10 p.m.
First Demonstration of Vertical Stacked Hetero-Oriented n-Ge (111)/p-Ge (100) CFET toward Mobility Balance Engineering, X-R Yu, A. Agarwal*, W-H Chang**, T-C Hong***, P-H Wu^, P-Y Fu*, J-H Lin^, P-J Sung, W-J Chen*, W-H Lu*, S-W Chang*, C-T Wu, T-C Cho, G-L Luo, K-H Kao*, D-D Lu*, R. W. Chuang*, W-Y Ma^, C-J Su, Y-J LEE, W-F Wu, T. Maeda**, T-S Chao***, W-K Yeh, Y-H Wang*, Taiwan Semiconductor Research Institute, *National Cheng Kung University, **National Institute of Advanced Industrial Science and Technology, ***National Yang Ming Chiao Tung University, ^Natl. Sun Yat-Sen University

T14-3 - 4:35 p.m.
Nearly Ideal Subthreshold Swing and Delay Reduction of Stacked Nanosheets Using Ultrathin Bodies, C-E Tsai, C-Y Cheng, B-W Huang, H-C Lin, T. Chou, C-T Tu, Y-C Liu, S-R Jan, Y-R Chen, W-H Hsieh, K-Y Chiu, S-J Chueh, C. W. Liu, National Taiwan University

T14-4 - 5:00 p.m.
Perspective on Low-dimensional Channel Materials for Extremely Scaled CMOS, S-K Su, E. Chen, T. Hung, M-Z Li, G. Pitner, C-C Cheng, H. Wang, J. Cai, H-S P. Wong, I. Radu, TSMC

Joint Focus Session 4 - Tapa 2
Compute in Memory
Thursday, June 16

Co-Chairs: A. Raychowdhury, Georgia Tech

JFS4-1 - 3:45 p.m.
An 8-bit 20.7 TOPS/W Multi-Level Cell ReRAM-based Compute Engine, J. Correll, L. Jie, S. Song, S. Lee, J. Zhu, W. Tang, L. Wormald, J. Erhardt, N. Breil*, R. Quon*, D. Kamalanathan*, S. Krishnan*, M. Chudzik*, Z. Zhang, W. Lu, M. Flynn, University of Michigan, *Applied Materials

JFS4-2 - 4:10 p.m.
A 40nm Analog-Input ADC-Free Compute-in-Memory RRAM Macro with Pulse-Width Modulation between Sub-arrays, H. Jiang, W. Li, S. Huang, S. Yu, Georgia Institute of Technology

JFS4-3 - 4:35 p.m.

A 22nm 128-kb MRAM Row/Column-Parallel In-Memory Computing Macro with Memory-Resistance Boosting and Multi-Column ADC Readout, P. Deaville, B. Zhang, N. Verma, Princeton University

JFS4-4 - 5:00 p.m.
In-Memory Approximate Computing Architecture Based on 3D-NAND Flash Memories, P-H Tseng, Y-H Lin, F-M Lee, T-C Bo, Y-C Li, M-H Lee, K-Y Hsieh, K-C Wang, C-Y Lu, Macronix International Co., Ltd.

Session T15 - Honolulu 1
Integrated Photonics
Thursday, June 16

Co-Chairs: T. Letavic, Globalfoundries
Y. Shiratori, NTT Corp.

T15-1 - 3:45 p.m.
First Demonstration of Fully CMOS-compatible Non-volatile Programmable Photonic Switch Enabled by Ferroelectric-SOI Waveguide for Next Generation Photonic Integrated Circuit, Y. Chen, G. Zhang, J. Zhou, Z. Zheng, L. Jiao, H. Wang, Z. Zhou, A. Kumar, J. Zhang, Y. Wang, Q. Kong, C. Sun, X. Gong, National University of Singapore

T15-2 - 4:10 p.m.
First Monolithic Integration of Group IV Waveguide Photodetectors and Modulators on 300 mm Si Substrates for 2-μm Wavelength Optoelectronic Integrated Circuit, H. Wang, G. Zhang, Y. Chen, J. Zhang, K. Han, Y. C. Huang*, X. Gong, National University of Singapore, *Applied Materials

T15-3 - 4:35 p.m.
First Si-Waveguide-Integrated InGaAs/InAlAs Avalanche Photodiodes on SOI Platform, J. Zhang, H. Xu, K. H. Tan, S. Wicaksono, Q. Kong, G. Zhang, Y. Chen, C. Sun, H. Wang, C. Wang, Z. Zheng, L. Jiao, Z. Zhou, C. C. W. Lim, S. F. Yoon, X. Gong, National University of Singapore

T15-4 - 5:00 p.m.
Low-capacitance Ultrathin InGaAs Membrane Photodetector on Si Slot Waveguide towards Receiver-less System, T. Akazawa, D. Wu, K. Sumita, N. Sekine, M. Okano*, K. Toprasertpong, S. Takagi, M. Takenaka, The University of Tokyo, *National Institute of Advanced Industrial Science and Technology

T15-5 - 5:25 p.m.
A sub-micron-thick InGaAs broadband (400-1700 nm) photodetectors with a high external quantum efficiency (>70%), D. Geum, J. Lim, J. Jang, S. Ahn, S. K. Kim, S. K. Kim, J. Shim, B. h. Kim, J. Park, W. J. Baek, J. Jeong, S. Kim, KAIST

Worshops
Thursday, June 16 – 8:00 p.m. – 10:00 p.m.

Technology Workshop 1 – Honolulu 1
Machine Learning Applications in Semiconductor Processes and Equipment Development

Machine learning has taken the forefront as the newest set of computational and analytical tools that can utilize large amounts of data and output patterns, solutions, diagnostics, and warnings, to enhance human decision making for the purposes of improving semiconductor process development and manufacturing. This workshop aims to highlight select applications, such as metrology, end-point detection, defect analysis, and plasma process development that have recently integrated Machine Learning and Artificial Intelligence as part of the semiconductor fabrication tool-set.

Technology Workshop 2 – Tapa 1
Heterogenous Integration – The Next Scaling Frontier: Material and Process Challenges

As traditional Moore's law driven scaling gets slower and more expensive with each node – heterogenous integration (HI) – or the integration of multiple dies in packages provides an alternate opportunity to scale and realize unique architectures. In this workshop, we will first discuss why HI is unique and important starting with a roadmap and high-level design overview session. Enabling HI schemes requires several advancements over traditional packaging technology. We will follow up the roadmap session with detailed focus talks from leaders in the industry and academia elaborating on some of these unique material and process requirements – hybrid bonding, fan out wafer level packaging, through silicon vias, and thermal management. We will end with a panel discussion with technology leaders identifying some of the key challenge areas where further advancements are needed to allow HI technology to fully mature.

Joint Workshop Honolulu 2
Cryogenic Electronics for Quantum Computing

Quantum computing has been heralded as a new computation paradigm, capable of solving today's intractable problems. The core of a quantum computer is a qubit array where superposition, entanglement, and interference are quantum mechanical properties that enable computation. Several styles of qubit have been proposed, while solid-state qubits have recently emerged as the most compelling devices to enable scalable quantum machines. Nevertheless, solid-state qubits are extremely fragile and generally require cryogenic operation. In this workshop, we look at the control of qubits by way of the most advanced CMOS technologies, which have recently been shown to operate near and below a Kelvin. The presentations will focus on scalability in quantum computing and how cryogenic electronics makes it possible, in principle, to achieve large counts of qubits operating continuously and reliably. The speakers will emphasize these and other aspects of electronic control for solid-state qubits, while introducing a vision for the future.

Circuits Workshop 1 – Honolulu 3
Recent Advances in Radar, Mm-Wave, and Sub-THz: Technology, Circuits, and Packaging

Circuits Workshop 2 – Tapa 2
The Emerging Ecosystem of Open-Source Chip Design

Open-source development has revolutionized the creation, maintenance, and distribution of software products over the past two decades. In recent years, open source aficionados have set out to replicate this success story for hardware design, including custom VLSI chips. The potential benefits of an open-source ecosystem for chip design are manifold and include: (1) Design re-use and cost-efficient agile design, (2) new opportunities in standardization, crowdsourcing and open global collaboration, (3) democratizing access to chip technology and attracting new talent. The purpose of this workshop is to review the latest developments in this space with a focus on open-source design automation tools and the potential for corporate adoption.

Circuits Workshop 3 – Tapa 3
Analog Circuits for IoTn

As traditional Moore's law driven scaling gets slower and more expensive with each node – heterogenous integration (HI) – or the integration of multiple dies in packages provides an alternate opportunity to scale and realize unique architectures. In this workshop, we will first discuss why HI is unique and important starting with a roadmap and high-level design overview session. Enabling HI schemes requires several advancements over traditional packaging technology. We will follow up the roadmap session with detailed focus talks from leaders in the industry and academia elaborating on some of these unique material and process requirements – hybrid bonding, fan out wafer level packaging, through silicon vias, and thermal management. We will end with a panel discussion with technology leaders identifying some of the key challenge areas where further advancements are needed to allow HI technology to fully mature.

Friday Forum – Tapa 1 and 2
June 17 – Friday

VLSI for infrastructure and infrastructure for VLSI

Organizers: Y. Liang, Nvidia; C. Sandner, Infineon Technologies; S. Fujii, Kioxia Corp.; M. Takamiya, The University of Tokyo

8:30 a.m. **Forum Opening,** Y. Liang

8:40 a.m. **Green Mobility - Future Concepts for a Sustainable Charging Infrastructure and Energy Delivery,** Uwe Kirchner, Infineon

9:25 a.m. **Creating New Opportunities with Connected Electric Vehicles in Security and Communication,** Jeff Cunningham, NXP

10:10 a.m. **Equipment to Fab digitization to enable Eco-Sustainability in explosive Semi Growth in Digital Era,** Sanjiv Mittal, AMAT

10:55 a.m. BREAK

11:10 a.m. **Computational Sensing Technologies for Cyber-Physical Infrastructure**, Atsutake Kosuge, Univ. of Tokyo

11:55 p.m. **Smart Design and Manufacturing Strategies for New Product Introduction and Volume Production in Leading Edge Technologies,** Andrzej Strojwas, PDF

12:40 a.m. Closing

These speakers are not able to come to the conference in-person, therefore the talks are available as pre-recording only:

Moore's Law and The Pursuit of Efficiency in Information and Communication Technology (ICT): Which Ecological Outcome?, David Bol, UC Louvain *(Pre-recording)*

Mixed-signal ICs for Power Electronics: A Key Driver for Bringing Out the Potential of Advanced Power Semiconductor Devices, Kohei Onizuka, Toshiba *(Pre-recording)*

Data Platform Technology for Big Data Utilization in Semiconductor Manufacturing, Hiroshi Akahori, Koxia *(Pre-recording)*