2023 Symposium on VLSI Technology and Circuits

Workshops

Organizers: M. Kanda, Toshiba Electronic Devices & Storage Corp.
K. Kanda, Fujitsu Research
T. Letavic, GLOBALFOUNDRIES Inc.

Workshop 1

Open Source PDKs and EDAs, Community Experiences toward Democratization of Chip Design [La Cigogne]

Sunday, June 11, 17:30-19:15

Organizer: M. Ikeda, The Univ. of Tokyo

Workshop 2

EUV Lithography & Path to High NA EUV Patterning Solutions [Suzaku I+II]

Sunday, June 11, 20:00-21:45

Organizer: A. Gabor, IBM Corp.

Development of Current EUV Tools and Future High NA Tools, A. Yen, ASML

Novel Resists to Achieve Promised High NA EUV Resolution, R. Wise, Lam Research Corp.

EUV and High NA EUV Mask Challenges, N. Hayashi, Dai Nippon Printing Co., Ltd.

High NA EUV Exposure Tool Implications to Chip and Mask Layouts, D. Schmidt, IBM Research

Resolution Capability and Stitching of Features Across the High NA Exposure Fields, E. van Setten, ASML

Workshop 3

Towards Functional Backside : What's Next After Backside Power Delivery? [Suzaku III]

Sunday, June 11, 20:00-21:45

Organizers: R. Chen, imec
G. Sisto, imec
G. Hellings, imec

System and Physical Design: Backside PDN for Mobile Applications, S.-C. Song, Google

System and Physical Design: Design and Process Considerations for Implementing Holistic Routing : Power Delivery, Clocking, and Signaling, R. Preston, ARM Ltd.

System and Physical Design: A New VLSI R&D Frontier : Cell-Level Interconnects to Enable Back-Side Power Delivery Networks (BSPDN) and Device Stacking, M. Kobrinsky, Intel Corp.

Electronic Design Automation: Backside Clock Delivery : Opportunities and Challenges from System Design Perspectives, S. K. Lim, Georgia Institute of Technology

Electronic Design Automation: Enabling Backside Technology Benefits Using Cadence Digital Full Flow, T. Makii, Cadence

Electronic Design Automation: Realizing PPA Benefits of Backside Power and Signal Routing Using Synopsys Digital Design Flow, A. Khurana, Synopsys, Inc.

Process and Integration: 3D Integration of SoC Power Delivery : Contacting the Standard Cell Power Grid from the Wafer Backside, A. Veloso, imec

Process and Integration: Evolution of Backside PDN and its Impact on Lithography, P. Wöltgens, ASML

Workshop 4

The Deployment of Materials to System Co-Optimization Methodology (MSCO) to Enable Rapid PPACt Assessment for Advanced Node Technology Development [Le Bois]

Sunday, June 11, 20:00-21:45

Organizers: S.-H. Yen, Applied Materials, Inc.
E. M. Bazizi, Applied Materials, Inc.

Materials to Systems Co-Optimization: Accelerating Technological Innovations,
B. Ayyagari-Sangamalli, Applied Materials, Inc.

Transition from Gate-All-Around to Stacked Transistor Architecture for Logic and SRAM, V. Moroz, Synopsys

System to Device Co-Optimization for Efficient Development of Analog In-Memory Accelerators,
G. Pedretti, Hewlett Packard Enterprise

Building a Methodology for Design- and System-Technology Co-Optimization, G. Hellings, imec

Design Technology Co-Optimization Solutions for Enhanced PPAC for CFET Device Architectures,
J. Smith, Tokyo Electron's Technology Center

Application Dependent Architectural Design Technology Innovation and Co-Optimization for Feature Rich Technologies, N. Jain, GlobalFoundries

Workshop 5

Uniform and Rigorous Benchmarking of Machine Learning ICs and Systems [La Cigogne]

Sunday, June 11, 20:00-21:45

Organizer: N. Shanbhag, Univ. of Illinois at Urbana-Champaign

MLPerf Tiny : Benchmarking Ultra-Low-Power Machine Learning Systems, V. Janapa Reddi, Harvard Univ./MLCommons

Proper Benchmarking of In-Memory Computing Architectures, N. Shanbhag, Univ. of Illinois at Urbana-Champaign

Characterizing and Assessing In-Memory Computing Processors, N. Verma, Princeton Univ.

Benchmarking Novel AI Accelerators : Striving to Be Both Fair and Comprehensive, G. Burr, IBM Research

Challenges in Designing and Evaluating Neural Processing Units, J.-S. Park, Samsung Electronics Co., Ltd.

Workshop 6

3D Image Sensor [Le Cygne]

Sunday, June 11, 20:00-21:45

Organizer: D. Shin, Samsung Advanced Institute of Technology

Role and Function of LiDAR Sensor for Autonomous Driving: Beyond Autonomous Driving Level 3,
K. Kweon, Hyundai Motor Company

3D Sensing Technologies for Immersive Experiences in the Metaverse, H. Finkelstein, Meta

Integrated LiDAR Sensors for L4 Autonomous Vehicles, J. Dunphy, Google

Indirect-ToF System for Non-Mobile Application, S.-C. Shin, Samsung Electronics Co., Ltd.

Time of Flight 3D-Sensing Architectures, B. Rae, STMicroelectronics

Silicon-Based FMCW Imaging for Human-Like Vison, M. Asghari, SiLC

Satellite Workshop

2023 Silicon Nanoelectronics Workshop [Shunju I+II]
Sunday, June 11, 8:30-18:30

Short Course 1

Advanced CMOS Technologies for 1 nm & Beyond [Shunju II+III]

Monday, June 12, 8:25-17:00

Chairpersons: K. Tomida, Rapidus Corp.
Y. Liang, NVIDIA Corp.

8:25 **Introduction**

8:30 **Transistor Scaling, Nanosheets/CFET + Seq.-3D,** C. Lin, Intel Corp.

9:20 **Advances in EUV lithography: From 0.33NA Technology towards High-NA and Beyond,** E. van Setten, ASML

10:10 **Break**

10:40 **Process Technology (Incl. Equipment) for adv. Logic, Non-BEOL,** N. Yoshida, Applied Materials, Inc.

11:30 **Challenges and Innovations for Advanced BEOL Scaling at the 1nm Node and Beyond,** C. Penny, IBM Corp.

12:20 **Lunch**

13:10 **CMOS Scaling by Backside Power Delivery,** N. Horiguchi, imec

14:00 **Process Control Solutions for the Era of 3D Architecture Devices,** S. H. Han, Nova

14:50 **Break**

15:10 **Semiconductor Packaging Revolution in the Era of Chiplets,** Y. Orii, Rapidus Corp.

16:00 **Device Technology for 2D Layered Semiconductor FETs: Challenge & Perspective,**
K. Nagashio, The Univ. of Tokyo

Short Course 2

Future Directions in Highspeed Wireline/Optical IO [Suzaku I+II]

Monday, June 12, 8:25-17:00

Chairpersons: K. Yoshioka, Keio Univ.
C. Tokunaga, Intel Corp.

8:25 **Introduction**

8:30 **Industry Megatrends Driving Connectivity R&D,** T. Carusone, Univ. Tronto

9:20 **SerDes System Design and Implementation,** T. Toifl, Cisco

10:10 **Break**

10:40 **Trends in Digital Coherent Technologies with DSP ASICs for Optical Communication Systems,**
F. Hamaoka, NTT Corp.

11:30 **Silicon Photonics Transceiver for High-Density Optical Interconnection,** T. Nakamura, AIO Dore Co., Ltd.

12:20 **Lunch**

13:10 **Beyond the Interconnect, a Survey of Challenges on the Way to Enabling Heterogenous Chiplets in Package,** A. Kashem, Advanced Micro Devices, Inc. (AMD)

14:00 **Architecture and Circuit Design of High-Speed Wireline Receivers,** A. Balankutty, Intel Corp.

14:50 **Break**

15:10 **Design Considerations for High-Speed Transmitters in Wireline and Optical Communications,**
A. Vasani, Broadcom Ltd.

16:00 **Recent Developments and Challenges for NAND Flash Memory Interface,** T. Toi, KIOXIA Corp.

Satellite Workshops

2023 Silicon Nanoelectronics Workshop [Shunju I]
Monday, June 12, 8:30-17:30

2023 Spintronics Workshop [La Cigogne]
Monday, June 12, 19:30-21:30

Demo Session & Welcome Reception [Suzaku I+II+III]

Monday, June 12, 17:30-19:30

Organizers: Y. Masuoka, Samsung Electronics Co., Ltd.
H. Yamaguchi, Fujitsu Ltd.
C. M. Lopez, imec

Opening and Plenary Session 1 [Shunju I+II+III]

Tuesday, June 13, 8:00-10:00

8:00-
Opening Remarks
K. Miyashita, Toshiba Electronic Devices & Storage Corp.
Y. Oike, Sony Semiconductor Solutions Corp.

8:40-
Plenary Session 1

Chairperson: T. Tsunomura, Tokyo Electron Ltd.

PL1-1 - 08:40 (Plenary)
Multi-Chiplet Heterogeneous Integration Packaging for Semiconductor System Scaling, S. Bhattacharya, A*STAR IME, Singapore

Since the invention of the transistor, we have enjoyed tremendous impact of semiconductors on electronic systems. Transistor scaling has played a critical role in achieving increased functionality of semiconductor systems in main-frames, personal computers, and mobile phones by enabling lower power, cost and area per function through monolithic System-on-Chip (SoC). However, over the past decade, the diverse system requirements from wide ranging markets have driven the industry to use heterogeneous integration of multiple chiplets enabled by advanced packaging as a key new toolbox for System-in-Package scaling. This paper provides an overview of multi-chiplet heterogeneous integration (MCHI) packaging platforms to address system scaling needs in coming decades.

Chairperson: R. Kapusta, Analog Devices, Inc.

PL1-2 - 09:20 (Plenary)
A Six-Word Story on the Future of VLSI:AI-driven, Software-defined, and Uncomfortably Exciting, P. Ranganathan, Google, USA

We are at an interesting inflection point in the design of computing systems. On one hand, demand for computing is accelerating at phenomenal rates, powered by the AI revolution and ever deeper processing on larger volumes of data, and amplified by smart edge devices and cloud computing. On the other hand, Moore's law is slowing down. This is challenging traditional assumptions around cheaper and more energy-efficient systems every generation, and leading to a significant supply-demand gap for future computing systems. In this paper, we discuss how this current computing landscape motivates a significant rethinking of how we design future hardware. We present two broad themes around (1) efficient design of hardware through custom silicon accelerators and (2) efficient utilization of hardware through software-defined systems design. Summarizing our experience in these areas, we identify key learnings and future opportunities for innovation. Looking ahead, we discuss some additional grand challenges and opportunities for the community, specifically touching on key themes around agility, modularity, reliability, and sustainability, as well as the disruptive potential of using machine learning for hardware design, and the opportunities beyond compute, around storage.

Circuits Session 1

Neural Interfaces [Suzaku III]

Tuesday, June 13, 10:30-12:35

Chairpersons: M. Je, KAIST
C. M. Lopez, imec

C1-1 - 10:30
A Wireless Sensor-Brain Interface System for Tracking and Guiding Animal Behaviors Through Goal-Directed Closed-Loop Neuromodulation, Y. Zhu*,**, Y. Hou*, J. Ji*, A. Zhou*, A. G. Richardson*** and X. Liu*,**, *Univ. of Toronto, **Univ. Health Network, Canada and ***Univ. of Pennsylvania, USA

This paper presents a wireless sensor-brain interface (SBI) system featuring a linked bidirectional neural interface IC and an image sensor IC for animal tracking. The system enables a novel experiment in which swimming rats navigate a water maze guided solely by brain stimulation. Closed-loop mapping of extracted rat behaviors to stimulation parameters is implemented with novel hardware acceleration for real-time operation with short latency. The neural interface device integrates stimulators with a new charge-balancing design and neural recording front-ends with stimulation artifacts rejection. A low-power UWB link is designed for wireless communication. The system has been successfully validated in multiple rats.

C1-2 - 10:55
A Wireless Neural Stimulator IC for Cortical Visual Prosthesis, J. Lee*, J. Letner*, J. Lim*, Y. Sun*, S. Jeong*, Y. Kim*, B. Koo*, G. Atzeni**, J. Liao**, J. Richie*, E. della Valle*, P. Patel*, T. Jang**, C. Chestek*, J. Phillips***, J. Weiland*, H.-S. Kim*, D. Sylvester* and D. Blaauw*, *Univ. of Michigan, USA, **ETH Zurich, Switzerland and ***Univ. of Delaware, USA

We propose a 0.25 x 0.25 x 0.3 mm (~0.02 mm^3) optically powered mote for visual cortex stimulation to restore vision. Up to 1024 implanted motes can be individually addressed. The complete StiMote system was confirmed fully functional when optically powered and cortex stimulation was confirmed in-vivo with a live rat brain.

C1-3 - 11:20
A 1024-Channel 268 nW/pixel 36x36 µm²/ch Data-Compressive Neural Recording IC for High-Bandwidth Brain-Computer Interfaces, M. Jang*, W.-H. Yu**, C. Lee***, M. Hays*, P. Wang*, N. Vitale*, P. Tandon*, P. Yan*, P.-I. Mak**, Y. Chae***, E.J. Chichilnisky*, B. Murmann* and D. G. Muratore****, *Stanford Univ., USA, **Univ. of Macau, Macau, ***Yonsei Univ., Korea and ****Delft Univ. of Technology, Netherlands

This paper presents a neural recording IC featuring lossy compression during digitization, thus preventing data deluge and enabling a compact active digital pixel design. The wired-OR-based compression discards unwanted baseline samples while allowing the reconstruction of spike samples. The IC features a 32x32 MEA with 36um pixel pitch and consumes 268nW per pixel from a single 1V supply. It achieves 9.8uV_{RMS} input-referred noise and 0.3-5kHz bandwidth, resulting in NEF/PEF of 3.7/14.1.

C1-4 - 11:45
AA 1,024-Channel, 64-Interconnect, Capacitive Neural Interface Using a Cross-Coupled Microelectrode Array and 2-Dimensional Code-Division Multiplexing, W. Choi*, Y. Chen*, D. Kim*, **, S. Weaver*, T. Schlotter*, C. Livanelioglu*, J. Liao*, R. Incandela*, P. Davami*, G. Atzeni*, S. Arjmandpour*, S.-H. Cho** and T. Jang*, *ETH Zurich, Switzerland and **KAIST, Korea

This paper presents a neural interface that senses the electrical double layer (EDL) capacitance as a function of the ion concentration produced by neurons firing action potentials (AP). Unlike conventional microelectrode arrays (MEAs) detecting voltage, capacitance sensing allows access to multiple recording sites with a single wire using code-division multiplexing (CDM), thereby significantly reducing the number of required interconnects. In this work, we implemented 32 drivers and 32 analog front-end circuits (AFEs) to realize 1,024 channel concurrent neural recordings while using a total of 64 interconnects and improving area efficiency for large-scale integration. This work achieves 9.7uW power/ch and 0.005mm² area/ch efficiency with the highest electrode density of 10,000mm^{-2}, and the fewest interconnects to the authors' best knowledge.

C1-5 - 12:10
A Wireless, Mechanically Flexible, 25µm-Thick, 65,536-Channel Subdural Surface Recording and Stimulating Microelectrode Array with Integrated Antennas, N. Zeng*, T. Jung*, M. Sharma*, G. Eichler*, J. Fabbri*, R. J. Cotton**, E. Spinazzi*, B. Youngerman*, L. Carloni* and K. L. Shepard*, *Columbia Univ. and **Northwestern Univ., USA

This paper presents a fully wireless microelectrode array (MEA) system-on-chip (SoC) with 65,536 electrodes for non-penetrative neural recording and stimulation, featuring a total sensing area of 6.8mm x 7.4mm with a 26.5um x 29um electrode pitch. Sensing, data telemetry, and powering are monolithically integrated on a single chip, which is made mechanically flexible to conform to the surface of the brain by substrate removal to a total thickness of 25um allowing it to be contained entirely in the subdural space under the skull.

Circuits Session 2

Non-Volatile Memory and Low Power SRAM [Suzaku I+II]

Tuesday, June 13, 10:30-12:35

Chairpersons: M. Miyamura, NanoBridge Semiconductor, Inc.
J. Kulkarni, Univ. of Texas, Austin

C2-1 - 10:30
A 1Tb 3b/Cell 3D-Flash Memory of more than 17Gb/mm² bit Density with 3.2Gbps Interface and 205MB/s Program Throughput, M. Sako*, T. Nakajima*, F. Kono*, T. Nakano*, M. Fujiu*, J. Musha*, D. Nakamura*, N. Kanagawa*, Y. Shimizu*, K. Yanagidaira*, T. Utsumi*, T. Kawano***, Y. Hosomura*, H. Yabe**, K. Hayashi**, Y. Watanabe*, T. Kouchi*, M. Kano**, H. Sugawara** and A. H. Sravan**, *KIOXIA Corp., Japan, **Western Digital Corp., USA and ***KIOXIA Systems Corp., Japan

A 210+ WL layers 1Tb 3b/cell 3D-Flash Memory achieves the high bit density of >17Gb/mm². Physical 8plane architecture realizes low read latency of 40us and high program throughput of 205MB. High interface speed of 3.2Gbps is accomplished by reducing DQ area in the X direction to 41%. Hybrid row address decoders (X-DEC) can deal with the wiring congestion issue caused by the new architecture, minimizing the read latency degradation. One-pulse-two-strobe technique reduces sensing time by 18% and contributes to the achievement of 205MB/s program throughput.

C2-2 - 10:55
A 14nm 128Mb Embedded MRAM Macro Achieved the Best Figure-Of-Merit with 80MHz Read Operation and 18.1Mb/mm² Implementation at 0.64V, G. Kang, H. Shin, H. Jung, S. Lee, J. Choi, S. Baek, J. Hyunsung, D. Kim, S. Hwang, S. Han, Y. Ji and S. S. Yoon, Samsung Electronics Co., Ltd., Korea

This paper describes an embedded spin transfer torque magnetic random access memory (STT-MRAM) focusing on minimizing macro area. By exploiting bit write operating condition, a merged source follower write driver (MSWD) is proposed to reduce write driver size and minimize write voltage mismatch. With a boosted pass-gate column mux (BPCM), additional local inverter for switching logic is eliminated. The proposed gated WL driver (GWLD) achieves faster wordline voltage settling time without increasing its size. Cell-based read offset compensation (CROC) is employed to improve read window for high-density memory and low Vdd operation. The proposed MRAM tolerant to solder-reflow process has been fabricated in a 14nm FinFET process, and the area of 128Mb macro is 18.1Mb/mm². The measurement results show that the proposed MRAM achieves 80MHz read access time in 0.64V core voltage at 150C temperature.

C2-3 - 11:20
A 3.0 Gb/s/pin 4th Generation F-Chip with Toggle 5.0 Specification for 16Tb NAND Flash Memory Multi Chip Package, Y. Jo, A. Kavala, T. Kim, B. Chun, J.-J. Park, T. Lee, J. Seo, M. Yang, T. Park, H. Kwon, C. Lee, Y. Son, J. Kwak, Y. Lee, H. S. Ku, D. Na, C. Yu, J. Park, J. Kim, H. Kwon, C. Kim, M.-K. Jung, C. Park, D. Seo, M. Kim, S. Lee, J.-Y. Lee, D. Kang, C. Yoon and S. Hur, Samsung Electronics Co., Ltd., Korea

A 1.2 V, 3.0 Gb/s/pin 16Tb NAND flash memory package with proposed 4th generation F-chip is presented. It is implemented with self-training techniques such as hybrid delay locked loop (DLL) and 3-step duty cycle correction (DCC) to overcome the speed bottlenecks in F-chip to NAND interface. Also, its multi-termination feature improves power efficiency by providing the use of different terminations on its interfaces. This work achieves an I/O speed of 3.0 Gb/s and power consumption of 58mW which are an improvement of 66% and 23.3%, respectively, in comparison with 3rd generation F-chip.

C2-4 - 11:45
A 40 nm 2 kb MTJ-Based Non-Volatile SRAM Macro with Novel Data-Aware Store Architecture for Normally Off Computing, K. Suzuki*, K. Hiraga*, K. Bessho*, K. Usami** and T. Umebayashi*, *Sony Semiconductor Solutions Corp. and **Shibaura Institute of Technology, Japan

We propose a magnetic tunnel junction (MTJ)-based non-volatile SRAM (NVSRAM) to obtain normally off computing. The proposed NVSRAM not only combines SRAM performance and non-volatility but also shows improved area efficiency by sharing the driver with peripheral circuits. Moreover, the data-aware store scheme enables reduction in store energy by data comparison control and a verify operation that mitigates MTJ process variation. We fabricated a 2 kb macro by using a 40 nm process with optimized memory cells to overcome the risk of latch destruction of conventional cells. The measurement results demonstrated a non-volatile function and 3.5x store energy reduction by the store control optimization.

C2-5 - 12:10
3.7-GHz Multi-Bank High-Current Single-Port Cache SRAM with 0.5V-1.4V Wide Voltage Range Operation in 3nm FinFET for HPC Applications, Y. Osada*, T. Nakazato*, K. Nii*, J.-J. Liaw**, S.-Y. M. Wu**, Q. Li**, H. Fujiwara**, H.-J. Liao** and T.-Y. J. Chang**, *TSMC Design Technology Japan, Japan and **TSMC, Taiwan

3.7-GHz Multi-Bank High-Current Single-Port Cache SRAM with 0.5V-1.4V Wide Voltage Range Operation in 3nm FinFET for HPC Applications
Wordline driver sleep (WLSLP) and write driver sleep (WDSLP) circuits are introduced to reduce leakage power while keeping fast write speed. With WLSLP and WDSLP, leakage power is reduced by 71%. In our SRAM design, it demonstrates 3.7GHz at 1.4 V and wide-range operation down to 0.5 V. It achieves the best FoM defined as density x frequency.

Technology Session 1

Highlight 1 [Shunju I+II+III]

Tuesday, June 13, 10:30-12:35

Chairpersons: K. Endo, Tohoku Univ.
B. Colombeau, Applied Materials, Inc.

T1-1 - 10:30
E-Core Implementation in Intel 4 with PowerVia (Backside Power) Technology, M. Shamanna, E. Abuayob, G. Aenuganti, C. Alvares, J. Antony, A. Bahudhanam, A. Chandran, P. Chew, A. Chatterjee, B. Chauhan, N. Dandeti, J. Desai, M. Doyle, T. Dmukauskas, P. Farache, E. Fetzer, K. Fischer, P. Hack, Y. Greenzweig, J. Giacobbe, W. Hafez, E. Haralson, A. Hegde, A. Illa, M. Islam, S. Jain, M. Jang, J. Nguyen, T. Tong, L. Jiang, E. Karl, P. Kalangi, G. Khoo, A. Krishnamoorthy, B. Kuns, W. A. Li, R. Livengood, T. Malik, R. Priyanka, H. Faraby, Y. Maymon, K. Mistry, K. Morgan, S. Natarajan, O. Nevo, M. L. Oh, P. Pardy, J. Park, P. Penmatsa, B. Phelps, C. Peterson, S. Rajappa, A. Raveh, A. Rezaie, T. Ravishankar, R. Ramaswamy, S. Reddy, R. Saha, S. Sen, R. Sanchez, R. Sanaga, B. Simkhovich, B. Sell, M. Senger, B. Schnarch, M. Seshadri, O. Sidorov, S. Subramaniam, K. Subramanian, B. Truong, S. Bangalore, J. Hicks, S. Venkatesh, D. Christensen, K. Bhargav, M. Von Haartman, P. Joshi, S. Zickel, C.-h. Lin, J. Huening, T.-h. Wu, N. Bakken, A. Afzal, A. Raman, S. Rao, V. Kawar, J. Neirynck, D. Bradley, M. Duwe, S. Wu, V. Patil and M. Bayoumy, Intel Corp., USA

PowerVia Technology is a novel innovation to extend Process Scaling by having Power Delivery on the backside. This paper presents the pre and post silicon findings from implementing an Intel E-Core in PowerVia Technology. PowerVia enabled standard cell utilization of greater than 90 percent in large areas of the core while showing greater than 5 percent frequency benefit in silicon due reduced IR drop. Successful Post silicon debug is demonstrated with slightly higher but acceptable throughput times. The thermal characteristics of the PowerVia testchip is inline with higher power densities expected from logic scaling

T1-2 - 10:55
World's First GAA 3nm Foundry platform Technology (SF3) with Novel Multi-Bridge-Channel-FET (MBCFET™) Process, J. Jeong, S. H. Lee, S.-a. Masuoka, S. Min, S. Lee, S. Kim, T. Myung, B. Choi, C.-W. Sohn, S. W. Kim, J. Choi, J. Park, H. Lee, T. Kim, S. Kim, Y. Yasuda-Masuoka, J.-H. Ku and G. Jeong, Samsung Electronics Co., Ltd., Korea

In this paper, 3nm Gate-All-Around technology (SF3) having more advanced 2nd generation of Multi-Bridge-Channel FET (MBCFET) has been demonstrated with additional process optimization from 1st generation GAA device (SF3E) already in mass production. As a result, SF3 platform successfully has 22% speed, 34% power gain and 0.79x logic area over our previous 4nm FinFET platform with additional design flexibility using various nano-sheet(NS) widths of MBCFET device in the same cell type.

T1-3 - 11:20
Nanosheet-based Complementary Field-Effect Transistors (CFETs) at 48nm Gate Pitch, and Middle Dielectric Isolation to Enable CFET Inner Spacer Formation and Multi-Vt Patterning, H. Mertens, M. Hosseini, T. Chiarella, D. Zhou, S. Wang, G. Mannaert, E. Dupuy, D. Radisic, Z. Tao, Y. Oniki, A. Hikavyy, E. Rosseel, A. Mingardi, S. Choudhury, P. Puttarame Gowda, F. Sebaai, A. Peter, K. Vandersmissen, J.-P. Soulie, A. De Keersgieter, L. Petersen Barbosa Lima, C. Cavalcante, D. Batuk, G. T. Martinez,, J. Geypen, F. Seidel, K. Paulussen,, P. Favia, J. Boemmels, R. Loo, P. Wong, A. Sepulveda Marquez, B. T. Chan, J. Mitard, S. Subramanian, S. Demuynck, E. Dentoni Litta, N. Horiguchi, S. Samavedam and S. Biesemans, imec, Belgium

We report on Si nanosheet monolithic Complementary Field-Effect Transistors (CFETs) at industry-relevant 48nm gate pitch, with source-drains (SDs) and SD contacts formed for either bottom or top devices. SD epi patterning at 30nm vertical N-P space and high-aspect-ratio SD contact formation are successfully demonstrated. Functional devices with excellent subthreshold slope (SS_{SAT}=70-75mV/dec) are reported for bottom and top devices, for both N- and PMOS. Middle dielectric isolation (MDI) formed by SiGe replacement processing is introduced as an enabler for monolithic CFET inner spacer formation and multi-Vt patterning.

T1-4 - 11:45
Scaled Contact Length with Low Contact Resistance in Monolayer 2d Channel Transistors, T. Y. T. Hung*, W.-C. Wu*, **, M. D. Sathaiya*, D. Fan***, G. Arutchelvan*, C.-F. Hsu*, S.-K. Su*, A. S. Chou*, E. Chen*, W. Li***, Z. Yu***, H. Qiu***, Y.-M. Yang****, K.-I. Lin****, Y.-Y. Shen**, W.-H. Chang**, S. L. Liew*, V. Hou*, J. Cai*, C.-C. Wu*, J. Wu*, P. H.-S. Wong*, X. Wang***, C.-H. Chien**, C.-C. Cheng* and I. P. Radu*, *TSMC and **National Yang Ming Chiao Tung Univ., Taiwan, ***Nanjing Univ., China and ****National Cheng Kung Univ., Taiwan

Two-dimensional transition metal dichalcogenides (2D TMDs) are expected to enable extremely scaled logic transistors for their ultrathin body and superior electrostatic control, i.e. gate length scaling. Aggressive scaling requires also contact length scaling. Here we demonstrate contact length scaling with low contact resistance of sub-100 ohms-um (best data in TLM) through optimized surface preparation and semimetal/metal stack. Monolayer-MoS_2 channel transistors have the same driving current at contact length down to 30 nm. A calibrated TCAD model which captured device trends is used to extrapolate to ~250 ohms-um at sub-15nm contact length per nanosheet of MoS2

T1-5 - 12:10
Contact Cavity Shaping and Selective SiGe:B Low-Temperature Epitaxy Process Solution for Sub 10^{-9} Ω.cm² Contact Resistivity in Nonplanar FETs, N. Breil*, B. C. Lee*, J. Avila Avendano*, J. Jewell*, M. Vellaikal*, E. Newman*, E. M. Bazizi*, A. Pal*, L. Lu*, O. Gluschenkov**, A. Greene**, S. Mochizuki**, N. Loubet**, B. Colombeau* and B. Haran*, *Applied Materials, Inc. and **IBM Research, USA

In order to tackle the CMOS contact resistance bottleneck, we developed a contact cavity shaping process that leverages a Reactive Ion Etching (RIE) technology, and a selective highly doped SiGe:B epitaxial process allowing an active boron doping level of 2E21 at.cm^{-3}. By co-optimizing these processes in the contact module on 300mm wafers, we demonstrate a record low transistor contact resistance of 11 ohms.um of W_{eff} with corresponding effective contact resistivity of 5.2x10-10 ohms.cm², which translates into a device I_{eff} performance gain of 44/19percent (median/leading edge).

Diversity Meeting [Le Bois]

Tuesday, June 13, 12:45-13:55

Circuits Session 3

Processors [Suzaku III]

Tuesday, June 13, 14:00-15:40

Chairpersons: V. Honkote, Intel Corp.
P. Raina, Stanford Univ.

C3-1 - 14:00
A 26.4mW, 18.6MS/s Image Reconstruction Processor for IoT Compressive Sensing, Y.-C. Lin*, C. Park**, W. Zhao***, N. Sun****, Y. Chae** and C.-H. Yang*, *National Taiwan Univ., Taiwan, **Yonsei Univ., Korea, ***The Univ. of Texas at Austin, USA and ****Tsinghua Univ., China

This work presents the *first* energy-efficient, real-time image reconstruction processor for IoT compressive sensing. The chip implemented in 40nm CMOS dissipates only 26.4mW with a throughput of 60fps for VGA images, delivering 5.4E6x and 6.5E4x higher energy and area efficiency than a high-end CPU. It supports an equivalent throughput of 18.6MS/s for 2D images, achieving 27.2x and 19.5x improvements in energy and area efficiency than state-of-the-art 1D compressive sensing reconstruction processors.

C3-2 - 14:25
A 169mW Fully-Integrated Ultrasound Imaging Processor Supporting Advanced Modes for Hand-Held Devices, Y.-L. Lo, Y.-C. Lo and C.-H. Yang, National Taiwan Univ., Taiwan

This work presents the first fully-integrated imaging processor that can support both standard and advanced modes. The TX delays are shared for different firing angles in plane-wave beamforming, reducing the number of stored delay values by 99.8%. Exchanging the processing order for the proposed coarse delay finding scheme reduces the storage size by 78.1% for elastography imaging. The chip dissipates 169mW at 200MHz from a 0.91V supply. It delivers a 20.3x higher beamforming rate with 6.7-to-36.6x less power dissipation than the state-of-the-art design, in addition to the capability for supporting ad-vanced modes.

C3-3 - 14:50
183.4nJ/inference 152.8μW Single-Chip Fully Synthesizable Wired-Logic DNN Processor for Always-On 35 Voice Commands Recognition Application, A. Kosuge, R. Sumikawa, Y.-C. Hsu, K. Shiba, M. Hamada and T. Kuroda, The Univ. of Tokyo, Japan

A 183.4nJ/inference single-chip wired-logic DNN processor that can recognize all 35 commands defined in the industrial standard voice recognition data set (Google Speech Command Dataset) is developed. This fully synthesizable processor can thus recognize 3.5 times more commands with 1.6 times better energy efficiency than the state-of-the-art analog processor while keeping design cost low. By implementing all the processing circuits and wiring required for the 16-layer DNN onto a single chip (7.63 mm^2 in 40nm), the need to store weight coefficients and intermediate data in DRAM/SRAM is eliminated. Owing to the proposed architecture, a low power consumption of 152.8uW is achieved, which is low enough for battery-powered always-on applications.

C3-4 - 15:15
A 12-nm 0.62-1.61 mW Ultra-Low Power Digital CIM-based Deep-Learning System for End-to-End Always-on Vision, E.-J. Chang*, C.-X. Xue*, C. Deshpande**, G. Jedhe**, J. Liang*, C.-C. Cheng*, H.-W. Lin*, C.-D. Lee*, S. Kumar**, K. S. Jway***, Z. Guo**, R. Garg**, A.-C. Lu*, C.-H. Lin*, M.-H. Hsieh*, T.-Y. Lin* and C.-C. Chen*, *MediaTek Inc., Taiwan, **MediaTek Inc., USA and ***MediaTek Inc., Singapore

This work proposes an ultra-low power DCIM-based DL system (DCIM-DLS) for end-to-end AoV with the power range from 0.62 to 1.61 mW (INT8, 2-15 fps). Compared to the prior art [3], the power consumption of DCIM-DLS can be reduced by 70.9% based on the following techniques: 1) an area and energy efficient DCIM that reduces compute RC loading by using pushed-rule 2p8T SRAM bitcell with folded kernels selector, 2) a DCIM-friendly dataflow strategy with dual accumulators that minimizes the DCIM power of weight update and avoids redundant data movement for power saving, and 3) a reconfigurable DCIM control scheme that supports mixed-precision to further reduce power consumption.

Circuits Session 4

Continuous-Time A/D Converteres [Suzaku II]

Tuesday, June 13, 14:00-15:40

Chairpersons: Y. S. Shu, MediaTek Inc.
S. Ho, MediaTek Inc.

C4-1 - 14:00
A 6.4-GS/s 1-GHz BW Continuous-Time Pipelined ADC with Time-Interleaved Sub-ADC-DAC Achieving 61.7-dB SNDR in 16-nm FinFET, R. Mittal*, H. Shibata**, S. Patil**, E. Krommenhoek***, P. Shrestha***, G. Manganaro****, A. P. Chandrakasan* and H.-S. Lee*, *MIT, USA, **Analog Devices, Inc., Canada, ***Analog Devices, Inc. and ****MediaTek Inc., USA

In this work, we present a continuous-time (CT) pipeline ADC with time-interleaved sub-ADC-DAC path in its first stage. The proposed sub-ADC-DAC path helps in increasing the ADC bandwidth by improving the signal cancellation at the stage-1 summing node. We have also designed an inductorless delay line for the first stage to improve amplitude and phase matching which reduces the input signal leakage into the backend ADC. A prototype ADC was fabricated in 16nm FinFET process. The ADC achieves 61.7/60.8dB (low/high frequency) SNR over 1-GHz bandwidth. The active area is 0.77mm^2 and the ADC consumes 240mW. The Schreier figure-of-merit (FOM_S) is 157.9dB which is amongst the best for ADCs with digitization bandwidth greater than 500MHz.

C4-2 - 14:25
A 0.024mm^2 84.2dB-SNDR 1MHz-BW 3rd-Order VCO-Based CTDSM with NS-SAR Quantizer (NSQ VCO CTDSM), H.-W. Chen*, S. Lee*, ** and M. Flynn*, *Univ. of Michigan and **Qualcomm Technologies, Inc., USA

This paper presents a VCO-Based Continuous-Time (CT) delta-sigma modulator (DSM) with a noise-shaping (NS) SAR quantizer for a 3rd order NTF. An anti-aliasing filter (AAF) enables this new hybrid architecture. The 28nm CMOS prototype NSQ VCO CTDSM achieves 84.2dB SNDR and 86.8dB DR within a 1MHz bandwidth while consuming 1.62mW at 100MS/s. The core circuit occupies only 0.024mm^2. No calibration or coefficient tuning is required.

C4-3 - 14:50
A 6GHz Multi-Path Multi-Frequency Chopping CTΔΣ Modulator Achieving 122dBFS SFDR from 150kHz to 120MHz BW, S. Javvaji*, M. Bolatkale*, **, S. Bajoria**, R. Rutten**, B. O. Essink**, K. Beijens**, K. Makinwa* and L. Breems*, **, *Delft Univ. of Technology and **NXP Semiconductors N.V., Netherlands

Advances in CMOS technologies have led to the development of continuous-time DS modulators (CTDSMs) with GHz sampling rates that achieve better than -100dBc linearity and bandwidths above 100MHz. However, at low frequencies (below ~10 MHz), their SNDR is limited by 1/*f* noise, which limits their use in radio receivers intended to cover both the AM and the FM bands. In this work, a multi-path multifrequency chopping scheme is proposed to suppress 1/*f* noise, while maintaining interferer robustness, noise, spurious, and linearity performance. Implemented in a CTDSM sampling at 6GHz, it reduces its 1/*f* noise corner frequency by 22x and achieves -98.3dBc THD, 122dBFS SFDR in 120MHz BW.

C4-4 - 15:15
A 4.4 GS/s 220 MHz ΣΔ ADC with a Linearized Back-Gate Controlled GmC Filter, J. Edler, M. Runge, S. Linnhoff and F. Gerfers, Technical Univ. of Berlin, Germany

This paper presents a 4.4 GS/s 220Mhz bandwidth continuous time sigma delta modulator with a linear GmC loop filter enabled by voltage tracking through multi-bit feedback and an active linearization scheme employing the back-gate node. An auxiliary amplifier drives the back-gate node of the main differential pair to linearize the overall $G_m(V_{in})$ curve. The fabricated prototype shows a 27dB reduction in third order intermodulation (IM3) products down to -78dBc and a SNDR of 62dB while consuming 22 mW, reaching excellent 49fJ/step power efficiency.

Circuits Session 5

Wireless Transceivers [Suzaku I]

Tuesday, June 13, 14:00-15:40

Chairpersons: W. Deng, Tsinghua Univ.
G. Hueber, Silicon Austria Labs

C5-1 - 14:00
A Time-Mode-Modulation Digital Quadrature Power Amplifier Based on 1-bit Delta-Sigma Modulator and Transformer Combined FIR FIlter, Y. Zhang, Z. Sun, B. Liu, J. Qiu, D. Xu, Y. Zhang, X. Fu, D. You, H. Huang, W. Madany, A. A. Fadila, Z. Liu, W. Wang, Y. Xiong, A. Shirane and K. Okada, Tokyo Institute of Technology, Japan

This paper proposes a Time-Mode Modulation (TMM) digital quadrature power amplifier (PA), which can realize high efficiency at power back-off (PBO) by applying the proposed 1-bit DSM and transformer (XFMR) combined FIR filter. The 1-bit Delta-Sigma Modulator (DSM) and digital mixer encode the input into a 2-level intrinsically linear on/off signal for TMM operation. The XFMR combined FIR filter suppresses the DSM quantization noise to avoid efficiency degradation and is insensitive to delay mismatches. The TMM PA is fabricated in 65 nm CMOS. Without digital pre-distortion (DPD), it achieves 26.4% efficiency with 40MS/s 64-QAM at 2.6GHz and supports 256-QAM.

C5-2 - 14:25
An 8.7 mW/TX, 21 mW/RX 6-to-9GHz IEEE 802.15.4a/4z Compliant IR-UWB Transceiver with Pulse Pre-Emphasis Achieving 14mm Ranging Precision, M. Song, E. Allebes, C. Marshall, A. N. Bhat, E. Bechthum, J. Dijkhuis, S. Traferro, E. Tiurin, P. Vis, J. van den Heuvel, M. El Soussi, P. Boer, A. Sheikh, B. Meyer, J. Liu, S. van der Ven, N. Winkel, M. Hijdra, G. K. Ramachandra, Y. Baykal, H. Visser, P. Zhang, A. Breeschoten, Y.-H. Liu and C. Bachmann, imec, Netherlands

This work presents an IEEE 802.15.4a4z compliant IR-UWB transceiver for high-precision ranging. By virtue of the proposed digital deserialization-serialization, the TX can generate the Inter-Symbol-Interference (ISI) free IEEE 802.15.4a4z packet. The proposed analog Finite Impulse Response (FIR)-based TX pre-emphasis improves 3.5x ranging precision without substantial power overhead and fulfills the spectrum requirement of the standard and the worldwide UWB regulations. The presented transceiver consumes 8.7 mW in TX mode and 21 mW in RX mode.

C5-3 - 14:50
A 6.5nW, -73.5dBm Sensitivity, Cryptographic Wake-Up Receiver with a PUF-Based OTP and Temperature-Insensitive Code Recovery, J. Park*, C. Jeon**, D. Minn*, H. Roh* and J.-Y. Sim*, *POSTECH and **Samsung Electronics Co., Ltd., Korea

This work proposes an algorithm and circuits for a cryptographic wake-up receiver (WuRX). Main contributions include 1) an algorithm and its implementation of OTP-based wake-up code generation that enables resynchronization, 2) implementation of a physically unclonable function (PUF) for the WuRX, 3) temperature-compensated ring-oscillator circuit, and 4) transition-based correlator that prevents accumulation of timing error to extend frequency mismatch tolerance up to 58%.

C5-4 - 15:15
An All-Digital Outphasing Transmitter IC for Ka-Band Bit-to-RF Concurrent Multi-Beam DBF Array, D. Wang*, J. Zhou*, h. Xu*, N. Zhang*, X. Su*, Z. Shen*, H. Jiang*, F. Yang*, Y. Wang**, J. Liu* and H. Liao*, *Peking Univ., China and **The Univ. of British Columbia, Canada

The first Ka-band DTX-based bit-to-RF multi-beam transmitter array is demonstrated in this work. The DTX IC features a prototype digital outphasing architecture with a 4x frequency multiplication scheme and a piecewise varactor array (PVA) linearization technique. Further, a compact wideband ADPLL with 24-bit phase shifting is integrated, eliminating the high-frequency LO distribution and improving the phase/gain alignment in the array. Leveraging these techniques, a low-cost 24.5-30GHz DTX is fabricated in 40nm CMOS. It achieves an EVM of -24.2dB for 16QAM without calibration and only occupies a core area of 1.2 x 1.35mm^2. Bit-to-RF concurrent multi-beam forming is demonstrated with a 1x8 uniform linear array (ULA) and the best normalized energy/area efficiency are achieved.

Technology Session 2

Reliability and Characterization [Shunju III]

Tuesday, June 13, 14:00-15:40

Chairpersons: Y. Yamamoto, Renesas Electronics Corp.
N. Mahalingam, Texas Instruments Inc.

T2-1 - 14:00
A Novel Bridge Transmission Line Method for Thin-Film Semiconductors: Modelling, Simulation Verification, and Experimental Demonstration, K. Han, Y. Kang, Y. Chen and X. Gong, National Univ. of Singapore, Singapore

A novel bridge transmission line method BTLM for thin-film semiconductors is proposed with validation from experiment. Our BLTM enjoys the advantages of parasitic resistance elimination, simple fabrication, highly accurate specific contact resistivity extraction, and most importantly strong variation immunity, which has rarely been considered in previous TLMs. The extraction accuracy and the variation immunity of BTLM were carefully verified by simulations By applying our proposed BTLM to nickel indium tin oxide contact, a record low contact resistivity of 4.4e-8 ohm cm^2 was obtained among all oxide semiconductors without gate bias.

T2-2 - 14:25
First Study of the Charge Trapping Aggravation Induced by Anti-Ferroelectric Switching in the MFIS Stack, Z. Zhou, L. Jiao, Z. Zheng, X. Wang, D. Zhang and X. Gong, National Univ. of Singapore, Singapore

In this work, we perform systematic and deep understanding of the interplay between polarization switching and charge trapping (CT) for both ferroelectric (FE) metal-ferroelectric-insulator-semiconductor (MFIS) stack and anti-ferroelectric (AFE) MFIS stack.

T2-3 - 14:50
Catching the Missing EM Consequence in Soft Breakdown Reliability in Advanced FinFETs: Impacts of Self-Heating, On-State TDDB, and Layout Dependence, Z. Dong*, Z. Sun**, X. Yang*, X. Li*, Y. Xue***, C. Luo*, P. Cai**, Z. Wang**, S. Wang***, Y. Zhang*, C. Wang*, P. Ren***, Z. Ji***, X. Wu*, R. Wang** and R. Huang**, *East China Normal Univ., **Peking Unive. and ***Shanghai Jiaotong Univ., China

For the first time, the *on-state* (V_{gs}>0, V_{ds}>0) time-dependent dielectric breakdown (TDDB) in FinFET technology is systematically studied. The assumption that the kinetics of soft breakdown (SBD) would remain the same and have no effect on electromigration (EM) is not true using advanced physical characterization techniques (TEM/EDX/EELS), as well as electrical-statistical tests and multiphysics simulations. By catching the missing EM consequence in SBD, the impacts of self-heating and an EM-aware layout topology is studied. Our study provide solid evidence of the SBD-induced EM, which is vital for the accurate prediction and boosting circuit reliability of advanced FinFETs and other multiple-gate device technology.

T2-4 - 15:15
FeRAM Recovery up to 200 Periods with Accumulated Endurance 10^{12} Cycles and an Applicable Array Circuit toward Unlimited eNVM Operations, K.-Y. Hsiang*, **, J.-Y. Lee*, ***, F.-S. Chang*, Z.-F. Lou*, Z.-X. Li*, Z.-H. Li*, J.-H. Chen*, C. W. Liu***, T.-H. Hou** and M.-H. Lee*, *National Taiwan Normal Univ., **National Yang Ming Chiao Tung Univ. and ***National Taiwan Univ., Taiwan

Asymmetric Field Cycling Recovery (AFCR) with a low E-field is proposed for the first time to extend the endurance cycles of a ferroelectric (FE) capacitor and is experimentally demonstrated for 200 periods and accumulated to 1e12 switching cycles. Positive and negative Asymmetric minor loops (AmL) with AFCR achieve the nondegradation and complete restoration of 2Pr toward the prospect of unlimited operation. Furthermore, an FeRAM array circuit with an inverting amplifier is designed to execute the Write/Read and Recovery procedures simultaneously by AFCR scheme.

Technology Session 3

NAND Flash [Shunju II]

Tuesday, June 13, 14:00-15:40

Chairpersons: D. Kil, SK hynix Inc.
J. Yu, Western Digital Corp.

T3-1 - 14:00
Novel Strategies for Highly Uniform and Reliable Cell Characteristics of 8th Generation 1Tb 3D-NAND Flash Memory, C. Lee, M.-t. Yu, S. Park, H. Lee, B. Kim, S. Lim, J. Lee, S.-h. Lee, M. Park, S. J. Ahn and S. H. Hur, Samsung Electronics Co., Ltd., Korea

The industry leading 8th generation 1Tb 3D-NAND flash memory (8th 3D-NAND) has been developed while possessing the smallest unit cell volume among all 3D-NAND products. Despite increasing stacking layers from 176 to 236, we improved the uniformity of channel hole size by utilizing the state of the art HARC (high-aspect ratio contact) etching technology. Degradation of interference and retention characteristics due to the cell scale-down is overcome by several ingenious technologies, leading to the development of highly reliable high performance device.

T3-2 - 14:25
Beyond 10 µm Depth Ultra-High Speed Etch Process with 84% Lower Carbon Footprint for Memory Channel Hole of 3D NAND Flash over 400 Layers, Y. Kihara, M. Tomura, W. Sakamoto, M. Honda and M. Kojima, Tokyo Electron Miyagi Ltd., Japan

A novel High-Aspect-Ratio (HAR) dielectric etch technology which is capable of etching beyond 10 µm depth memory channel hole for future generations of 3D NAND flash memory has been successfully developed for the first time. Ten micron depth etching is not practical with conventional etching technology, but our novel technology using cryogenic wafer stage and new gas chemistry can achieve not only 10 µm etch capability but also quite short process time (33 minutes) with 84% carbon footprint reduction of greenhouse gases. Etched profile was also confirmed to be excellent. Thus, this is a key technology for highly productive, cost effective and sustainable manufacturing of 3D NAND flash memory device.

T3-3 - 14:50
Demonstration of Recovery Annealing on 7-Bits per Cell 3D Flash Memory at Cryogenic Operation for Bit Cost Scalability and Sustainability, Y. Aiba, Y. Higashi, H. Tanaka, H. Tanaka, F. Kikushima, T. Fujisawa, H. Mukaida, M. Miura and T. Sanuki, KIOXIA Corp., Japan

This report is the first to demonstrate cryogenic 3D flash memory of 7-bits per cell with the recovery annealing applied repeatedly. We combined 77 K cryogenic operation and epi-Si channel to improve the data retention, read noise, and program noise, and their degradation caused by Program/Erase (P/E) cycles. We further applied 200 degree celsius annealing which recovers performance degradations under appropriate cell Vth conditions. Reliable 7-bits per cell operation can maintain performance and energy efficiency competitive to current QLC and NL-HDD technologies. Co-optimization of process technology, memory operation, and cooling system is a promising solution for future sustainable bit cost scaling.

T3-4 - 15:15
High Bit Cost Scalability and Reliable Cell Characteristics for 7th Generation 1Tb 4Bit/Cell 3D-NAND Flash, K. Kim, Y. Seo, S. Park, W. Jang, D. Yoo, J. Lim, I.-h. Park, j. Lee, K. Noh, S. Ahn and S. Hur, Samsung Electronics Co., Ltd., Korea

The continuous increase of total number of word-line (WL) layers and the reduction of unit cell size make it difficult to implement quad-level cell (QLC) in 3D-NAND flash. In this paper, we introduce several technological breakthroughs to realize QLC with high performance and reliability for 7th generation 3D-NAND (7th QLC). By introducing advanced technologies, the QLC reliability is enhanced by 74% compared to before the improvement, which is equivalent the previous generation QLC 3D-NAND with 92-layer (5th QLC). Furthermore, the average performance is 25% increased and bit density is doubled compare to 5th QLC.

Technology Session 4

DTCO [Shunju I]

Tuesday, June 13, 14:00-15:40

Chairpersons: O. Cheng, United Microelectronics Corp. (UMC)
Y. Liang, NVIDIA Corp.

T4-1 - 14:00
Breakthrough Design Technology Co-Optimization Using BSPDN and Standard Cell Variants for Maximizing Block-Level PPA, S. Lee, S. Jung, Y. Jang, J. Do, J. Yu, H. You, M. Jeong, J. Lim, J. Han, S. Park, Y. Kim, J. Kwon, H. Kim and S. Yoon, Samsung Electronics Co., Ltd., Korea

The challenge in designing a modern process beyond 3nm is that scaling is no longer based on incremental change purely at the process level. In facing end of Moore's Law, we need to find out novel innovative ideas to reduce the gap between reality and Moore's Law trend. In this paper, we introduce breakthrough design technology co-optimization knobs to maximize block-level PPA for advanced CMOS technology. Through these knobs, we improve Fmax +3.6% and block area -14.8% with back-side power delivery network (BSPDN). Furthermore, through the standard cell variants, block area is reduced up to -2.4% and block performance is improved about +1.6%

T4-2 - 14:25
PPA and Scaling Potential of Backside Power Options in N2 and A14 Nanosheet Technology, S. Yang, P. Schuddinck, M. Garcia-Bardon, Y. Xiang, A. Veloso, B. T. Chan, G. Mirabelli, G. Hiblot, G. Hellings and J. Ryckaert, imec, Belgium

This paper evaluates Power-Performance-Area (PPA) tradeoffs and integration challenges of three types of backside power connections: Through Silicon Via in the Middle Of Line (TSVM), Self-Aligned Front-to-Back via (BPR) and Backside contact (BSC) for nanosheets at N2 and A14 nodes. From TSVM to BPR to BSC, solid PPA gains are shown for High Density Logic, at the expense of increased process complexity. While TSVM remains competitive in N2 7-Track high-performance technology, BSC shows maximal gains in A14 5-Track high density node.

T4-3 - 14:50
Upcoming Challenges of ESD Reliability in DTCO with BS-PDN Routing via BPRs, W.-C. Chen*, **, S.-H. Chen**, A. Veloso**, K. Serbulova*, **, G. Hellings** and G. Guido*, **, *KU Leuven and **imec, Belgium

In this paper, the impact of double-sided connectivity and buried power rails (BPR) on electrostatic discharge (ESD) diodes is reported. Connection from the backside and BPRs can change ESD current path and uniformity. It also introduces parasitic capacitance and layout penalty to ESD diodes. The ESD performance is strongly dependent on layout styles. Guidelines for a better layout style of double-sided connectivity cooperating with BPRs are proposed.

T4-4 - 15:15
Towards DTCO in High Temperature GaN-On-Si Technology: Arithmetic Logic Unit at 300 °C and CAD Framework Up to 500 °C, Q. Xie*, M. Yuan*, J. Niroula*, B. Sikder**, S. Luo***, K. Fu***, ****, N. S. Rajput*****, A. B. Pranta*****, P. Yadav*, Y. Zhao***, N. Chowdhury** and T. Palacios*, *MIT, USA, **Bangladesh Univ. of Engineering and Technology, Bangladesh, ***Rice Univ., ****Univ. of Utah, USA and *****Technology Innovation Institute, United Arab Emirates

This article reports advances in high temperature (HT) GaN-on-Si technology by taking pioneering steps towards design technology co-optimization (DTCO). A computer-aided design (CAD) framework was established and experimentally validated up to 500 °C, the highest temperature achieved by such a framework for GaN technology. This framework was made possible thanks to (1) demonstration of multiple key functional building blocks (e.g. arithmetic logic unit (ALU)) by the proposed technology at HT; (2) experimentally calibrated transistor compact models up to 500 °C (highest temperature modeled for an Enhancement-mode GaN transistor). Excellent agreement was achieved between experimental and simulated circuits in the static characteristics (<0.1 V difference in voltage swing) and trends of dynamic characteristics (timing) were accurately captured. By adopting complementary approaches in experiment and simulation, this work lays the foundation for the scaling-up of HT GaN-on-Si technology for mixed-signal applications of HT (>300 °C) electronics.

Circuits Session 6

High-Speed Links [Suzaku III]

Tuesday, June 13, 16:00-18:05

Chairpersons: T. Iwai, KIOXIA Corp.
P. Upadhyaya, Advanced Micro Devices, Inc. (AMD)

C6-1 - 16:00
A 112-Gb/s 58-mW PAM4 Transmitter in 28-nm CMOS Technology, M. Forghani, Y. Zhao, P. K. Khanna and B. Razavi, Univ. of California, Los Angeles, USA

A voltage-mode transmitter employs a resistorless output DAC, a 3-tap latchless FFE, a passive output skew compensation network, and a 56-GHz integer-*N* PLL. The prototype delivers an output swing of 0.8 $V_{pp,d}$ with a power efficiency of 0.52 pJ/bit, an rms clock jitter of 160 fs and RLM = 96%.

C6-2 - 16:25
A 256 Gbps Heterogeneously Integrated Silicon Photonic Microring-Based DWDM Receiver Suitable for In-Package Optical I/O, Z. Xuan, G. Balamurugan, D. Huang, R. Kumar, J. Sharma, C. Levy, J. Kim, C. Ma, G.-l. Su, S. Liu, X. Wu, T. Acikalin, H. Rong and J. Jaussi, Intel Corp., USA

We present a 256 Gb/s (8 wavelength * 32 Gb/s/wavelength) 3D-integrated silicon photonic (SiPh) receiver suitable for integration in XPU/switch packages. The photonic IC (PIC) integrates a multi-wavelength laser, optical amplifier, and cascaded micro-ring resonators (MRRs) to implement dense wavelength division multiplexing (DWDM) with minimal footprint. The 28nm CMOS electronic IC includes eight SerDes channels, and PIC interface/control electronics. A dither-based thermal control unit tunes MRRs in the optical demux to align with the laser grid with sub-pm resolution. Measured results demonstrate BER<1e-12 when receiving 256 Gb/s DWDM input generated by MRRs modulating eight 200 GHz-spaced wavelengths. This is 2X higher aggregate bandwidth than previously published SiPh MRR-based receivers, with higher level of photonic integration.

C6-3 - 16:50
A 0.32pJ/b 90Gbps PAM4 Optical Receiver Front-End with Automatic Gain Control in 12nm CMOS FinFET, M. Haghi Kashani*, H. Shakiba** and A. Sheikholeslami*, *Univ. of Toronto and **Huawei Technologies Canada, Canada

This work presents a 0.32pJ/b 90Gbps PAM4 optical receiver (RX) front-end with a 13.4pA/sqrt(Hz) noise density. The proposed design employs a new transimpedance amplifier (TIA) and a single-ended-to-differential (S2D) block providing a large gain-bandwidth product with less power and area overhead compared to the conventional designs. The proposed RX is implemented in 12nm CMOS FinFET process and co-packaged with a commercial photodiode (PD), offering the best power efficiency, input-referred noise, and figure-of-merit (FOM) amongst the previous state-of-the-art designs [1-5].

C6-4 - 17:15
A 64-Gb/s Reference-Less PAM4 CDR with Asymmetrical Linear Phase Detector Soring 231.5-fs_{rms} Clock Jitter and 0.21-pJ/Bit Energy Efficiency in 40-nm CMOS, Z. Zhang*, **, Z. Zhang*, Y. Chen***, N. Qi*, **, J. Liu*, **, N. Wu*, ** and L. Liu*, **, *Institute of Semiconductors, Chinese Academy of Sciences, **Univ. of Chinese Academy of Sciences and ***Univ. of Macau, China

This paper reports a quarter-rate reference-less PAM4 clock and data recovery (CDR) circuit. Our proposed asymmetrical linear phase detector (A-LPD) can simultaneously detect frequency and phase difference for the PAM4 input, thus, fully eliminating the external reference clock or frequency-locked loop. Meanwhile, the presented A-LPD can sense all 12-type PAM4 transitions to reduce the RMS jitter of the recovered clock. An exclusive-OR ring phase-locked loop (XOR-RPLL) is devised for low-power and low-jitter 8-phase clock generation. Fabricated in a 40-nm CMOS, our prototype CDR achieves 231.5-fs_{rms} clock jitter, 0.21-pJ-per-bit energy efficiency, $<10^{-12}$ bit error rate at 64 Gbps, and a capture range of 57.2-to-65 Gbps.

C6-5 - 17:40
A 50Gb/s DAC-Based Multicarrier Polar Transmitter in 22nm FinFET, I.-M. Yi*, **, S. K. Kaile*, Y. Zhu*, J. C. Gomez Diaz*, S. Hoyos* and S. Palermo*, *Texas A&M Univ., USA and **Gwangju Institute of Science and Technology, Korea

A DAC-based polar transmitter (TX) for wireline applications efficiently implements jitter-robust multicarrier signaling with arbitrary modulation formats. 50Gb/s total data rate is supported by three parallel 5GS/s output drivers operating with baseband PAM-4 and mid-band (MB) and high-band (HB) 16-state complex modulation on 5 and 10GHz orthogonal carriers. DAC amplitude resolution is 7b plus 2b predistortion for all drivers, while the polar MB and HB drivers also have 7b phase resolution. The TX DSP implements 8-tap FIR filtering on all bands. Fabricated in 22nm FinFET, the TX has 1.2V_{ppd} swing and achieves 50Gb/s BER<10^{-4} with both QAM-16 and APSK-4+12 modulations at 1.68pJ/b.

Circuits Session 7

Digital Systems [Suzaku II]

Tuesday, June 13, 16:00-18:05

Chairpersons: C. H. Yang, National Taiwan Univ.
P. Whatmough, Qualcomm AI Research

C7-1 - 16:00
Arvon: A Heterogeneous SiP Integrating a 14nm FPGA and Two 22nm 1.8TFLOPS/W DSPs with 1.7Tbps/mm² AIB 2.0 Interface to Provide Versatile Workload Acceleration, W. Tang*, S.-G. Cho**, T. T. Hoang**, J. Botimer*, W. Q. Zhu**, C.-C. Chang**, C.-H. Lu*, J. Zhu*, Y. Tao*, T. Wei*, N. K. Motwani*, M. Yalamanchi**, R. Yarlagadda**, S. Kale**, M. Flanigan**, A. Chan**, T. Tran**, S. Shumarayev** and Z. Zhang*, *Univ. of Michigan and **Intel Corp., USA

Arvon is a heterogeneous system in a package (SiP) that integrates a 14nm FPGA chiplet with two dense and efficient 22nm DSP chiplets through Embedded Multi-die Interconnect Bridges (EMIBs). The chiplets communicate via a 1.536Tbps Advanced Interface Bus (AIB) 1.0 interface and a 7.68Tbps AIB 2.0 interface. We demonstrate the first-ever AIB 2.0 I/O prototype using 36um-pitch microbumps, achieving 4Gbps/pin at 0.10pJ/b (0.46pJ/b including adapter), and a bandwidth density of 1.024Tbps/mm-shoreline and 1.705Tbps/mm²-area. Arvon is programmable, supporting workloads from neural network (NN) to communication processing (comm) and providing a peak performance of 4.14TFLOPS (FP16, half-precision floating-point) by each DSP chiplet at 1.8TFLOPS/W. A compilation flow is developed to map workloads across FPGA and DSPs to optimize performance and utilization.

C7-2 - 16:25
A 4.8mW, 800Mbps Hybrid Crypto SoC for Post-Quantum Secure Neural Interfacing, L.-H. Lin*, Z.-S. Fu*, P.-S. Chen*, B.-Y. Yang** and C.-H. Yang*, *National Taiwan Univ. and **Academia Sinica, Taiwan

This work presents the world's first post-quantum hybrid crypto SoC that achieves an 800Mpbs throughput and consumes only 4.8mW for remote neural interfacing. The chip dissipates 0.70uJ/OP for the handshake and 48pJ/B for data encryption in 40nm CMOS. Flexible authenticated encryption is supported. This work achieves 3-175x higher area efficiency with 16-41x less energy than state-of-the-art designs.

C7-3 - 16:50
A Bit-Serial Computing Accelerator for Solving Coupled Partial Differential Equations, J. Mu*, C. Yu*, **, T. T.-H. Kim* and B. Kim***, *Nanyang Technological Univ., **Institute of Microelectronics, A*STAR, Singapore and ***Univ. of California, Santa Barbara, USA

This work presents a bit-serial computing hardware accelerator with a 20x10 fully-parallel processing element (PE) array for solving 1D/2D coupled partial differential equations (PDEs) with three key highlights. First, a reconfigurable 2D bit-serial PE array is implemented to process 1D/2D coupled PDEs, addressing the limited reconfigurability of the prior analog solvers. Second, bit-serial and in-memory computing regimes are adopted for minimizing energy- and area-overhead due to communications between PEs and with external memory. In addition, multiple variables are merged into a unified PE, saving the overall area by 53.1% by sharing bit-serial computing units. Finally, massive parallelism is enabled by operating all PEs simultaneously, minimizing latency to find numerical solutions. The test chip is fabricated with a 65nm technology, occupying a core area of 0.458mm² and consuming 107.8pJ and 110.8pJ, respectively, for solving 1D and 2D coupled PDEs at 1V and 25.6MHz.

C7-4 - 17:15
A 2.35 Gb/s/mm² (7440, 6696) NB-LDPC Decoder Over GF(32) Using Memory-Reduced Column-Wise Trellis Min-Max Algorithm in 28nm CMOS Technology, J. Choe and Y. Lee, POSTECH, Korea

For the cost-efficient non-binary low-density parity-check (NB-LDPC) decoder realization, this paper presents a column-wise trellis min-max (CW-TMM) algorithm, greatly relaxing the sorter costs of the previous TMM method without lowering the error-correcting capability. The message compression is used to the trellis-based decoder for the first time, minimizing the memory requirements even for long NB-LDPC codes. In addition, novel circuit-level optimizations are developed to further remove the redundant computing units in the previous works. As a result, the prototype (7440, 6696) decoder over GF(32) in 28 nm CMOS process achieves the normalized area-efficiency of 2.35 Gb/s/mm², saving the decoding complexity and the on-chip memory size by 63% and 54%, respectively.

C7-5 - 17:40
A 65nm 60mW Dual-Loop Adaptive Digital Beamformer with Optimized Sidelobe Cancellation and On-Chip DOA Estimation for mm-Wave Applications, S. Ryu, A. Sangbone Assoa, S. Konno and A. Raychowdhury, Georgia Institute of Technology, USA

This paper demonstrates an mm-wave baseband digital beamformer that fully integrates an adaptive sidelobe canceller and on-chip direction of arrival (DOA) estimation. To achieve high energy-efficiency, the DOA estimation loop preemptively adjusts the weights of the phase rotators at the front of the SAR-ADCs, which enables the sidelobe cancellation loop to be implemented with a straightforward structure. For efficient ESPRIT DOA estimation, CORDIC-based QR-iteration is employed to solve eigenvalue decomposition, thus circumventing the need for complex matrix computation. The adaptive beamformer implemented in 65nm CMOS dissipates 60mW at 100MHz while occupying 0.64mm² on-chip area. The energy efficiency is 600 (330) pJ/symbol with (without) DOA estimation.

Circuits Session 8

Biomedical Circuit and Systems [Suzaku I]

Tuesday, June 13, 16:00-18:05

Chairpersons: K. Matsunaga, NTT Corp.
P. Nadeau, Analog Devices, Inc.

C8-1 - 16:00
Wireless Body-Area Network Transceiver ICs with Concurrent Body-Coupled Powering and Communication Using Single Electrode, J. Li*, Y. Dong**, L. Lin*, J. S. Y. Tan**, J. Y. Fong** and J. Yoo**,***, *Southern Univ. of Science and Technology, China, **National Univ. of Singapore and ***The N.1 Institute for Health, Singapore, Singapore

We propose the wireless body-coupled power (BCP) transfer ICs with concurrent body-coupled communication (BCC) via a single electrode. Base Station (BS) IC employs the adaptive Self-Interference Cancellation for >40dB signal suppression and a Charge Replenishing HV driver for 31% power saving. Sensor Node (SN) IC adopts ground-domain separation with 89.1% cross-ground-domain power efficiency. The ICs in 40nm standard CMOS deliver power with concurrent data uplink and downlink to the entire body area.

C8-2 - 16:25
A Fingertip-Mimicking 12×16 200μm-Resolution *e*-skin Taxel Readout Chip with Per-Taxel Spiking Readout and Embedded Receptive Field Processing, M. D. Alea*, A. Safa*,**, F. Giacomozzi***, A. Adami***, I. R. Temel***, L. Lorenzelli*** and G. Gielen*,**, *KU Leuven, **imec, Belgium and ***Fondazione Bruno Kessler, Italy

This work describes an electronic skin (*e*-skin) taxel readout chip in 0.18μm CMOS technology, achieving the highest reported spatial resolution of 200μm, comparable to human fingertips. A key innovation is the integration on chip of a 12x16 taxel array with per-taxel signal conditioning frontend and spiking readout combined with embedded neuromorphic first-order processing through complex receptive fields (CRFs). The chip has been designed to incorporate a polyvinylidene fluoride (PVDF)-based piezoelectric sensor layer. Experimental results show that spiking neural network (SNN)-based classification of the chip's spatiotemporal spiking output for input tactile stimuli such as texture and flutter frequency achieves excellent accuracies up to 97.1% and 99.2% of classification accuracy, respectively. This is despite using only a small 256-neuron SNN classifier, a low equivalent spike encoding resolution of 3-4 bits, a sub-Nyquist 2.2kHz population spiking rate, and a state-of-the-art per-taxel (12.33nW) and system (75μW-5mW) power consumption.

C8-3 - 16:50
A 110dB-TCMRR TDM-based 8-Channel Noncontact ECG Recording IC with Suppression of Motion-Induced Coupling in < 0.3s and CMI Cancellation Up to 22V_{PP}, K.-J. Choi*, S. Choi** and J.-Y. Sim*, *POSTECH and **Samsung Electronics Co., Ltd., Korea

This paper presents the first noncontact electrocardiogram (ECG) recording IC that suppresses the effects of common-mode interference (CMI), motion artifacts, and extra common-mode to differential-mode (CM-DM) conversions induced by the motion artifacts. Implemented in an 8-channel ECG recording with a digitally-assisted time-division multiplexing (TDM) architecture, the IC achieves a total CMRR (TCMRR) of 110dB and an adaptation in response to electrode-tissue impedance (ETI) variations in less than 0.3s.

C8-4 - 17:15
A Pitch-Matched Transceiver ASIC for 3D Ultrasonography with Micro-Beamforming ADCs Based on Passive Boxcar Integration and a Multi-Level Datalink, P. Guo*, Z.-Y. Chang*, E. Noothout*, H. Vos*,**, J. Bosch**, N. de Jong*,**, M. Verweij*,** and M. Pertijs*, *Delft Univ. of Technology and **Erasmus MC, Netherlands

This paper presents a pitch-matched transceiver ASIC integrated with a 2-D transducer array for a wearable ultrasound device for transfontanelle ultrasonography. The ASIC combines 8-fold multiplexing, 4-channel micro-beamforming and sub-array-level digitization to achieve a 128-fold channel-count reduction. The micro-beamforming is based on passive boxcar integration and interfaces with a 10-bit 40 MS/s SAR ADC in the charge domain, thus obviating the need for explicit anti-alias filtering and power-hungry ADC drivers. A compact and low-power reference generator employs an area-efficient MOS capacitor as a reservoir to quickly set a reference for the ADC in the charge domain. A low-power multi-level data link concatenates outputs of four ADCs, leading to an aggregate 3.84 Gb/s data rate. Per channel, the RX circuit consumes 2.06 mW and occupies 0.05 mm^2.

C8-5 - 17:40
A CMOS/Microfluidics Point-of-Care SoC Employing Square-Wave Voltcoulometry for Biosensing with Aptamers and CRISPR-Cas12a Enzymes, Y.-T. Hsiao*, S.-Y. Chuang*, H.-Y. Hou*, Y.-C. Su*, H.-C. Yeh*, H.-T. Song*, Y.-J. Chang*, W.-Y. Weng*, Y.-C. Tsai*, P.-Y. Lin*, S.-Y. Chen*, Y.-J. Lin***, M.-W. Lin*** and J.-C. Chien*,**, *National Taiwan Univ., Taiwan, **Univ. of California, Berkeley, USA and ***Industrial Technology Research Institute of Taiwan, Taiwan

This paper presents a CMOS/microfluidics point-of-care (PoC) SoC for molecular detection using DNA aptamers and CRISPR-associated enzymes (Cas). We take advantage of the signaling property from the electron transfers of the redox reporters and present a square-wave volt-coulometry (SWVC) electrochemical readout circuit to achieve >100x signal enhancement. The SoC is implemented in 180-nm CMOS technology, integrated with pH and temperature sensors, and consumes a total power of 2.4mW.

Technology / Circuits Joint Focus Session 1

New Computing [Suzaku III]

June 13, 2023, 16:00-18:05

Chairpersons: M. Tada, NanoBridge Semiconductor, Inc.
I. Arsovski, Groq, Inc.

JFS1-1 - 16:00 (Invited)
Exploring Power Savings of Gate-All-Around Cryogenic Technology, M. Victor, Synopsys, USA

JFS1-2 - 16:25 (Invited)
Circuit Designs for Practical-Scale Fault-Tolerant Quantum Computing, Y. Suzuki*, **, Y. Ueno***, ****, ******, W. Liao****, M. Tanaka***** and T. Tanimoto**, ******, *NTT Computer & Data Science Laboratories, **JST RESTO, ***Keio Univ., ****The Univ. of Tokyo, *****Nagoya Univ. and ******Kyushu Univ., Japan

To demonstrate reliable and scalable quantum computation, we need quantum error correction to reduce its error rates. One of the most challenging parts of implementing quantum error correction is to design error-decoding units, which estimate errors during computation. We estimate the required performances of error-decoding units to run practical-scale quantum algorithms and discuss the directions to satisfy them.

JFS1-3 - 16:50
Long-Time-Constant Leaky-Integrating Oxygen-Vacancy Drift-Diffusion FET for Human-Interactive Spiking Reservoir Computingcomputing, H. Inoue*, H. Tamura**, A. Kitoh*, X. Chen**, Z. Byambadorj**, T. Yajima***, Y. Hotta****, T. Iizuka**, G. Tanaka** and I. H. Inoue*, *AIST, **The Univ. of Tokyo, ***Kyushu Univ. and ****Univ. of Hyogo, Japan

Reservoir computing is one of the best feasible means of information processing that does not require substantial computation, such as backpropagation. Implementation using spiking neural networks is promising for real-time and low-energy computation that can be completed by edge devices alone. The key parameter is a time constant τ_n of the neurons, which should be close to that of external stimuli and can be on the order of milliseconds for human-interactive reservoir computing. Here, we present a slow spiking neuron based on an oxygen-vacancy drift-diffusion field-effect transistor (ODD-FET). In these transistors, the slow migration of oxygen vacancies mimics a leaky integration with τ_n on the order of 10 to 100 ms. The feasibility of the proposed ODD-FET on the human-interactive application is demonstrated by a spiking reservoir composed of these neurons, which can accurately detect handwriting anomalies.

JFS1-4 - 17:15
Experimental Demonstration of Probabilistic-Bit (p-bit) Utilizing Stochastic Oscillation of Threshold Switch Device, S. Heo, D. Kim, W. Choi, S. Ban, O. Kwon and H. Hwang, POSTECH, Korea

To realize p-bits that fluctuate between 0 and 1 with precisely controlled probabilities, stochastic oscillation behavior of threshold switch (TS) device was induced by applying supply voltage (V_{DD}) near-threshold voltage (V_{TH}). Insulator-metal transition (IMT) device and ovonic threshold switch (OTS) device were investigated as a source of p-bit generation. It was confirmed that a small voltage change of mV-scale in the near-threshold region can give a high degree of stochasticity to the oscillation frequency. Also, the probability was controlled by a comparator and shift of a compare-voltage (V_{comp}) with excellent controllability. Finally, a simple probabilistic Boolean logic operation was tested by 100 p-bits generated from IMT devices.

JFS1-5 - 17:40
Accelerating Adaptive Parallel Tempering with FPGA-Based p-bits, N. A. Aadit*, M. Mohseni** and K. Y. Camsari*, *Univ. of California, Santa Barbara and **Google LLC, USA

Special-purpose hardware to solve optimization problems formulated as Ising models has generated great excitement recently. Despite a large diversity in hardware, most solvers employ standard variations of the classical (simulated) annealing (CA) algorithm. Here, we show how powerful replica-based Parallel Tempering (PT) algorithms can significantly outperform CA, using FPGA-based probabilistic computers. Using a massively parallel (graph-colored) architecture, we implement the Adaptive PT (APT) algorithm, generating problem-dependent temperature profiles to equalize replica swap probabilities. We benchmark our p-computer against analytical results from classical Ising theory and use our machine to solve spin-glass instances formulated as hard optimization problems. APT outperforms heuristic choices of temperature profiles used in conventional PT and a replica-based version of CA. Our machine provides 6,000X speedup over optimized CPU, with orders of magnitude further speedup projected for scaled implementations. The developed co-design techniques may be useful for a broad range of Ising machines beyond p-computers.

Technology Session 5

Ferroelectric 1: FeFETs [Shunju II]

Tuesday, June 13, 16:00-18:05

Chairpersons: K. Tomida, Rapidus Corp.
S. Datta, Georgia Institute of Technology

T5-1 - 16:00
Strategy for 3D Ferroelectric Transistor: Critical Surface Orientation Dependence of $HfZrO_x$ on Si, S.-H. Kuk*, J.-H. Han**, B. H. Kim*, J. P. Kim* and S.-H. Kim*, *KAIST and **Korea Institute of Science and Technology (KIST), Korea

Si surface orientation is one of the important factors to determine the performance of 3D-structured devices such as fin-, nanosheet- and vertical-field-effect transistors. We reveal that the crystallization annealing temperature, remnant polarization (P_r), and coercive field (E_c) of the ferroelectric $HfZrO_x$ stack on Si show strong surface orientation dependence. We evaluate $HfZrO_x$-based ferroelectric field-effect-transistor (FEFET) on Si with different orientations for both memory and logic applications. Based on the findings, the impact of surface orientation in SOI FE FinFET is shown. Finally, we suggest a strategy for 3D-structured FEFET with targeted applications.

T5-2 - 16:25
HZO Scaling and Fatigue Recovery in FeFET with Low Voltage Operation: Evidence of Transition from Interface Degradation to Ferroelectric Fatigue, Z. Cai, K. Toprasertpong, M. Takenaka and S. Takagi, The Univ. of Tokyo, Japan

Thickness scaling of FeFETs with $Hf_{0.5}Zr_{0.5}O_2$ (HZO) from 11 down to 4.6 nm is systematically studied in this work in terms of the memory characteristics and the memory window (MW) narrowing mechanism. The HZO thickness scaling leads to low-voltage operation, higher Ion/Ioff ratio, lower S.S., and better endurance. It is also found, for the first time, that with reducing cycling voltage the dominant narrowing mechanism changes from MOS interface degradation to ferroelectric fatigue, which can be recovered by a high-voltage pulse. Based on this finding, we propose and demonstrate a method to improve endurance by utilizing this recovery, which is more effective in thinner HZO FeFETs.

T5-3 - 16:50
First Stacked Nanosheet FeFET Featuring Memory Window of 1.8V at Record Low Write Voltage of 2V and Endurance >1E11 Cycles, Y.-R. Chen, Y.-C. Liu, Z. Zhao, W.-H. Hsieh, J.-Y. Lee, C.-T. Tu, B.-W. Huang, J.-F. Wang, S.-J. Chueh, Y. Xing, G.-H. Chen, H.-C. Chou, D. S. Woo, M. H. Lee and C. W. Liu, National Taiwan Univ., Taiwan

The large memory window of 1.8V at the low write voltage of 2V is achieved by stacked two nanosheet (NS) gate-all-around (GAA) $Ge_{0.98}Si_{0.02}$ FeFETs with the channel phosphorus concentration larger than $1E18cm^{-3}$, enabling the erase of GAA FeFET. Isotropic wet etching was used in channel release process. Stacked two NSs have the advantages of reducing cell variation and 2X read current. The stable storage with data retention of >1E4 seconds, linearly extrapolated 10 years, and high endurance >1E11 cycles are also demonstrated. The thermal budget is as low as 400°C. The stacked NS architecture with high mobility channels makes FeFETs to be compatible with the 2nm node and beyond.

T5-4 - 17:15
First Demonstration of BEOL-Compatible MFMIS Fe-FETs with 3D Multi-Fin Floating Gate: In-Situ ALD-Deposited MFM, L_{CH} of 50 nm, > 2×10^9 Endurance, and 58.3% Area Saving, X. Wang, Z. Zheng, Q. Kong, L. Jiao, K. Han, C. Sun, Z. Zhou, L. Liu, Y. Kang, G. Liu, D. Zhang and X. Gong, National Univ. of Singapore, Singapore

Addressing the major concern of area-inefficiency for metal-ferroelectric-metal-insulator-semiconductor (MFMIS) ferroelectric FETs (Fe-FETs), for the first time, we demonstrate 3D MFMIS Fe-FETs employing Multi-Fin floating gate (FG) that enlarges the channel area and realizes desired area ratio (AR) at a fixed device footprint. Such novel device architecture realizes an AR of 1:2.4 with ~58.3% area saving as compared with the conventional planar structure. Together with the incorporation of an in-situ ALD deposited ferroelectric layer and TiN electrodes,as well as the ALD-enabled conformal growth of HfO2 dielectric layer and ZnO channel without breaking the vacuum for enhanced gate stack quality, the device with a channel length (L_{CH}) of 50 nm achieves a memory window (MW) of 1.5 V and endurance over 2E9.

T5-5 - 17:40
Cold-FeFET as Embedded Non-Volatile Memory with Unlimited Cycling Endurance, S. G. Kirtania, K. A. Aabrar, A. I. Khan, S. Yu and S. Datta, Georgia Institute of Technology, USA

We demonstrate a 1.2x reduction in write voltage, 20x improvement in write speed and unlimited cycling endurance on a BEOL compatible Ferroelectric FET (FeFET) at 77K (Cold FeFET), justifying the potential of Cold-FEFET as a candidate for last-level cache memory in cryogenic high-performance computing (HPC) applications. Highly stable and tight threshold voltage distribution characteristics for both programmed and erased states in Cold-FeFET (pre and post cycling) is leveraged to reduce the read-current window specs and lower the write voltage amplitude and pulse compared to room temperature operation. In conjunction with logic CMOS operating at 77K, monolithic 3D integrated Cold-FeFET with unlimited write endurance provides an effective solution for future cryogenic HPC applications.

Technology Session 6

Logic Technology 1: Advanced Platforms and Device Structures [Shunju I]

Tuesday, June 13, 16:00-18:05

Chairpersons: Y. Masuoka, Samsung Electronics Co., Ltd.
S. C. Song, Google

T6-1 - 16:00
Intel PowerVia Technology: Backside Power Delivery for High Density and High-Performance Computing, W. Hafez, P. Agnihotri, M. Asoro, M. Aykol, B. Bains, R. Bambery, M. Bapna, A. Barik, A. Chatterjee, P. C. Chiu, T. Chu, C. Firby, K. Fischer, M. Fradkin, H. Greve, G. Alok, E. Haralson, M. Haran, J. Hicks, A. Illa, M. Jang, S. Klopcic, M. Kobrinsky, B. Kuns, H.-h. Lai, L. Lanni, S.-h. Lee, N. Lindert, C.-l. Lo, Y. Luo, G. Malyavanatham, B. Marinkovic, Y. Maymon, M. Nabors, J. Neirynck, P. Packan, A. Paliwal, L. Pantisano, L. Paulson, P. Penmatsa, C. Prasad, C. Puls, T. Rahman, R. Ramaswamy, S. Samant, B. Sell, K. Sethi, F. Shah, M. Shamanna, K. Shang, Q. Li, M. Sibakoti, J. Stoeger, N. Strutt, R. Thirugnanasambandam, C. Tsai, X. Wang, A. Wang, S.-j. Wu, Q. Xu, X.-h. Zhong and S. Natarajan, Intel Corp., USA

This paper presents a high-yielding backside power delivery (BPD) technology, PowerVia, implemented on Intel 4 finFET process. PowerVia more directly integrates power delivery to the transistor as compared to published buried power rail schemes, enabling additional wiring resources on front side for signal routing. A fabricated Atom core with >90% cell utilization showed >30% platform voltage droop improvement and 6% frequency benefit compared to a similar design without PowerVia. Transistor performance, reliability, and fault isolation capability is detailed.

T6-2 - 16:25
High Performance 5G Mobile SOC Productization with 4nm EUV Fin-FET Technology, J. Yuan, J. Deng, V. Lin, Y. Chen, J. Chiu, M. Lin, J. Chen, D. Zhang, Y. Chen, D. Liu, B. Yu, H. Wang, G. Nallapati, V. Mohan, V. Sanaka, B. Baran, F. Dahan, P. Bhadri, R. Geol,V. Boynapalli, S. Bazarjani, P. Penzes, P. Agashe and P. R. Chidambaram, Qualcomm Technologies, Inc., USA

We report Snapdragon 8 Gen 2, the latest Qualcomm 5G integrated mobile SoC flagship platform, in mass production with the most advanced 4nm EUV FinFET technology. Snap-dragon 8 Gen 2 w 4nm process had ~20% chip area scaling and ~20% RO performance gain vs previous 5nm process used in Snapdragon® 888 production. Snapdragon® 8 Gen 2 exhibits 25% & 100% performance gain @power in CPU & GPU respectively and >20% better battery life over Snapdragon® 888 driven by both process improvements and design optimization. This high performance and low power SOC platform enable its application in both mobile and computing/gaming/AI. The 2nd year 4nm process demonstrated RO performance +4% gain and BEOL Via Rc >20% reduction, no yield degradation confirmed its readiness for next generation Snapdragon productization

T6-3 - 16:50
Molybdenum Nitride as a Scalable and Thermally Stable pWFM for CFET, H. Arimura*, S. Brus*, J. Franco*, Y. Oniki*, A. Vandooren*, T. Conard*, BT. Chan*, B. Kannan**, M. Samiee**, W. Li**, P. Deminskyi***, E. Shero**, J. Bakke**, N. Jourdan*, G. A. Verni***, J. W. Maes****, M. Givens****, L.-A. Ragnarsson*, J. Mitard*, E. D. Litta* and N. Horiguchi*, *imec, Belgium, **ASM America, USA, ***ASM Microchemistry Oy, Finland and ****ASM Belgium, Belgium

ALD MoN is proposed as a scalable and thermally stable p-type WFM for CFET. The early film closure and high WF of the ALD MoN make it as a promising scalable pWFM applicable to a wide-tunable multi-Vt nanosheet gate stack. The high EWF of MoN pMOS is also thermally stable as compared to the reference TiN, which makes it suitable for CFET. On planar RMG pFETs, Vt reduction by up to 220 mV was achieved with MoN barrier compared to the TiN for the same physical thickness, without affecting long channel hole mobility and NBTI reliability.

T6-4 - 17:15
Integration of a Stacked Contact MOL for Monolithic CFET, V. Vega-Gonzalez, D. Radisic, BT. Chan, S. Choudhury, S. Wang, A. Mingardi, Q. Toan Le, H. De Coster, Y. Oniki, P. Puttarame Gowda, K. Vandersmissen, J.-P. Soulie, A. Sepulveda Marquez, A. Peter, D. Batuk, G. T. Martinez Alanis, O. Richard, J. Boemmels, S. Biesemans, E. Dentoni Litta, N. Horiguchi, S. Park and Z. Tokei, imec, Belgium

Complementary FET (CFET) is a device architecture where n- and p-MOS transistors are stacked. As a result, the source and drain contact metals also need to be stacked. In this work, we tackle the high aspect-ratio (AR) patterning and metallization required for the monolithic CFET integration scheme. The bottom contact is formed by filling trenches with W up to AR = 16 and CD=12nm, followed by CMP and metal etch back at 45, 50 and 60 nm pitch printed by EUV lithography. We study the accuracy of the metal EB process using scatterometry, TEM and a new CDSEM technique, and observed a global Vertical Edge Placement Error (VEPE) as small as 2% for etch amounts ranging from 60 to 100 nm. Excellent correlation with electrical data was obtained. The top contact is separated from the bottom contact by an oxide fabricated in similar way (deposition, CMP and EB).

T6-5 - 17:40
Front-side and Back-Side Power Delivery Network Guidelines for 2nm Node High Perf Computing and Mobile SoC Applications, J. Lee*, J. Jeong*, S. Lee*, S. Lee*, J. Lim*, S.-C. Song**, S. Ekbote**, N. Stevens-Yu**, D. Greenlaw** and R.-H. Baek*, *POSTECH, Korea and **Google LLC, USA

For the first time, we propose selection guidelines for using the front-side (FS) or back-side (BS) power delivery network (PDN) in a 2nm node. IR drop of various FS and BS-PDN structures have been analyzed for high-performance computing (HPC) and mobile SoC applications. Added process cost (PC) of BS-PDN should be <5.9% of nanosheet FET (NSFET) based front-side cost for mobile SoCs, but much higher <10.9% for HPCs, to be cost-effective at similar IR drop.

Evening Panel Discussion 1

What is Scalable & Sustainable in the Next 25 Years? [Shunju I]

Tuesday, June 13, 20:00-21:30

Organizers: M. Tada, NanoBridge Semiconductor, Inc.
S-C. Song, Google

Moderator: T. Yamamoto, Tokyo Electron Ltd.

Panelists: A. Goda, Micron Memory Japan, K.K.
D. Greenlaw, Google
G. Yeap, TSMC
M. Chudzik, Applied Materials, Inc.
M. Na, SK hynix Inc.
S. Samavedam, imec

Evening Panel Discussion 2

Can Universities Help to Revitalize the IC Design Industry? If So, How? [Suzaku I]

Tuesday, June 13, 20:00-21:30

Organizers: T. Nezuka, MIRISE Technologies Corp.
S. Ho, MediaTek Inc.

Moderator: A. Abidi, Univ. of California, Los Angeles

Panelists: A. Matsuzawa, Tokyo Institute of Technology / Tech Idea
D. Friedman, IBM
Kenneth K. O, Univ. of Texas at Dallas
M. Choi, Samsung Electronics Co., Ltd.
M. Shulaker, MIT / ADI
M-F. Chang, TSMC / NTHU

SSCS & EDS Young Professionals and Students Micro-Mentoring & Career Coaching Session [Le Cygne]

Tuesday, June 13, 18:15-19:15

Award and Plenary Session 2 [Suzaku I+II+III]

Wednesday, June 14, 8:00-10:00

8:00-
Award Ceremony

8:40-
Plenary Session 2

Chairperson: M. Hamada, The Univ. of Tokyo

PL2-1 - 8:40 (Plenary)
Quantum Computing from Hype to Game Changer, H. Mizuno, Hitachi, Ltd., Japan

This paper describes the current state of quantum computer development in the world (including the hype) from three perspectives and introduces our research and development of quantum computers. The first is the complex market structure. While investments in quantum computers are increasing, these investments do not always immediately bring value to consumers, and this delay results in hype. CMOS annealing technology to fill this delay is described. The second is the accountability of the impact produced by a quantum computer that does not yet exist. This paper discusses why so many people continue to question the value of quantum computers despite their clear applications, and our struggles. The third is technology development, which includes many research aspects. This paper introduces our top-down approach that takes full advantage of semiconductor technologies. Some of our activities including “Shuttling qubit” for the next milestone in the development of silicon quantum computers, which is qubit operation in a scalable qubit array structure, are also described.

Chairperson: V. Narayanan, IBM T. J. Watson Research Center

PL2-2 - 9:20 (Plenary)
Searching for Nonlinearity: Scaling Limits in NAND Flash, S. Sivaram and A. Ilkbahar, Western Digital, USA

Data generation is growing at an exponential rate and the market opportunity for data storage is vast. However, there is still a substantial difference in the amount of data created versus data stored, driven by price elasticity of demand in the storage media. Pricing lies in the balance of supply and demand, but for NAND manufacturers to be profitable, cost is the driver for consistent price decline and will ultimately determine the amount of data stored. In this talk, we show that as NAND Flash moves into a mature era of 3D scaling using only increasing layer count results in a sub-linear cost reduction while producing higher bit growth. This breaks the virtuous cycle of growth, producing more bits than the market can absorb at a given price point and challenges the affordability of future investments. NAND scaling needs to move away from solely increasing layer count and instead seeking new avenues for reducing cost and complexity. Equipment productivity and reduction in consumables remain critical focus areas for the supply chain to contribute to cost reduction. Wafer bonding technology can be an enabler for new opportunities. It allows for decoupling the memory array from complex logic circuits, allowing new high speed logic integration with the memory layers, and simplifying manufacturing cycle times. This technology also allows the industry to move away from a one-size-fits-all NAND die to customized solutions for various applications and system level savings. Despite such breakthroughs, ultimately the health of the storage industry will be determined by fair distribution of the profit pool across the value chain commensurate with the R&D and capital spending by the different players.

Circuits Session 9

Advanced SRAM Design [Suzaku III]

Wednesday, June 14, 10:30-12:35

Chairpersons: K. Miyano, Micron Memory Japan K.K.
J. Wuu, Advanced Micro Devices, Inc. (AMD)

C9-1 - 10:30
A 3nm 256Mb SRAM in FinFET Technology with New Array Banking Architecture and Write-Assist Circuitry Scheme for High-Density and Low-V_{MIN} Applications, J. Chang, Y.-H. Chen, G. Chan, K.-C. Lin, P.-S. Wang, Y. Lin, S. Chen, P. Lin, C.-W. Wu, C.-Y. Lin, Y.-H. Nien, H. Fujiwara, A. Katoch, R. Lee, H.-J. Liao, J.-J. Liaw, S.-Y. M. Wu and Q. Li, TSMC Design Technology, Taiwan

This paper presents a 3nm 256Mb SRAM in FinFET technology with interleaved triple WL scheme and new array banking architecture for low VMIN applications.

C9-2 - 10:55
A 1.9GHz 0.57V Vmin 576Kb Embedded Product-Ready L2 Cache in 5nm FinFET Technology, N. Jungmann*, R. Joshi**, E. Kachir*, K. Shimanovich*, B. He***, T. Cohen*, T. Miller***, D. Leu***, D. Kannambadi***, I. Wagner*, K. Reyer***, H. Konen*, M. Suleiman*, V. Sindhe*** and Y. Freiman*, *IBM Systems and technology, Israel, **IBM T. J. Watson Research Center and ***IBM Systems and technology, USA

A product ready L2 cache (L2C) design based on 6T ultra dense SRAM cells with novel circuits capable of boosting word line, cell, and, bit-line supplies independently using single supply and metal coupling capacitance is demonstrated for the first time in 5nm technology. A metal short detection circuit is provided to increase the robustness of the design. Hardware data shows that L2C operates with a minimum supply of 0.57V and reaches a maximum operating frequency of 1.9GHz at 1.1V.
Introduction: Conventional large size L2C and

C9-3 - 11:20
A 4.0GHz UHS Pseudo Two-Port SRAM with BL Charge Time Reduction and Flying Word-Line for HPC Applications in 4nm FinFET Technology, J. Kim, B. Yook, T. Choi, K. Choi, C. Lee, Y. Li, Y. Lee, S. Yun, C. Do, H. Tang, I. Lee, D. Seo and S. Baeck, Samsung Electronics Co., Ltd., Korea

To implement ultra-high-speed (UHS) SRAM is a major challenge for high performance computing (HPC) chip. This paper presents BL Charge Time Reduction (BLCTR) with Clamped BL Discharge (CBLD) and Flying Word-Line (FWL) to maximize the SRAM speed. BLCTR with CBLD improves cycle time by decreasing the BL pre-charge time and write time. FWL architecture removes gate loading and accelerates the performance. A test-chip using BLCTR and FWL is fabricated in 4nm FinFET process and demonstrates UHS pseudo two-port SRAM (P2P-SRAM) operating at 4.0GHz

C9-4 - 11:45
A 4.24GHz 128X256 SRAM Operating Double Pump Read Write Same Cycle in 5nm Technology, Z. N. Zhang, Y. S. Kim, P. Hsu, S. Kim, D. Tao, H.-J. Liao, P. W. Wang, G. Yeap, Q. Li and T.-Y. J. Chang, TSMC, Taiwan

A high speed 1R1W two port 32Kbit (128X256) SRAM with single port 6T bitcell macro is proposed. A Read-Then-Write (RTW) double pump CLK generation circuit with TRKBL bypassing is proposed to enhance read performance. Double metal scheme is applied to improve signal integrity and overall operating cycle time. A Local Interlock Circuit (LIC) is introduced in Sense-Amp to reduce active power and push Fmax further. The silicon results show that the slow corner wafer was able to achieve 4.24GHz at 1.0V and 100 degree Celsius in 5nm FinFET technology.

C9-5 - 12:10
A 3-nm 27.6-Mbit/mm² Self-Timed SRAM Enabling 0.48 - 1.2 V Wide Operating Range with Far-End Pre-Charge and Weak-Bit Tracking, Y. Aoyagi*, M. Yabuuchi*, T. Tanaka*, Y. Ishii*, Y. Osada*, T. Nakazato*, K. Nii*, I. Wang**, Y.-H. Hsu**, H.-C. Cheng**, H.-J. Liao** and J. T.-Y. Chang**, *TSMC Design Technology Japan, Japan and **TSMC, Taiwan

A 3-nm single-port (SP) 6T SRAM macro has been proposed using far-end pre-charge (FPC) circuit and weak-bit (WB) tracking circuit. These circuit can reduce write cycle time to boost the pre-charge time and read cycle time to improve the trackability of supply voltage. We designed and fabricated a 434-kbit SP SRAM macro on 3-nm FinFET technology. The bit density is 27.6-Mbit/mm² and achieved 1.9 GHz operation at 0.75 V which is 35% faster than conventional performance. It achieves 70.0 Freq.-Density / VDD product, being the world's highest Figure of Merit.

Circuits Session 10

Advanced Memories for AI [Suzaku I+II]

Wednesday, June 14, 10:30-12:35

Chairpersons: K. Sohn, Samsung Electronics Co., Ltd.
T. Mohsenin, Univ. of Maryland, Baltimore County

C10-1 - 10:30
A 2.38 MCells/mm² 9.81 - 350 TOPS/W RRAM Compute-in-Memory Macro in 40nm CMOS with Hybrid Offset/IOFF Cancellation and ICELLRBLSL Drop Mitigation, S. D. Spetalnick*, M. Chang*, S. Konno*, B. Crafton*, A. S. Lele*, W.-S. Khwa**, Y.-D. Chih**, M.-F. Chang** and A. Raychowdhury*, *Georgia Institute of Technology, USA and **TSMC, Taiwan

A dense compute-in-memory (CIM) macro using resistive random-access memory (RRAM) showing solutions to read channel mismatch, high I_{OFF}, ADC offset, IR drop, and cell resistance variation is presented. By combining a hybrid analog/mixed-signal offset cancellation scheme and IR drop mitigation with a low cell bias target voltage, the proposed macro demonstrates robust operation (post-ECC bit error rate (BER) < $5x10^{-8}$ for 8WL CIM) while maintaining an effective cell density 1.03 - 33.1x higher than prior art and achieving 1.74 - 13.35x improved average MAC efficiency relative to the previous highest-density RRAM CIM macro.

C10-2 - 10:55
A 28nm Nonvolatile AI Edge Processor using 4Mb Analog-Based Near-Memory- Compute ReRAM with 27.2 TOPS/W for Tiny AI Edge Devices, T.-H. Wen*, J.-M. Hung*, H.-H. Hsu*, Y. Wu*, F.-C. Chang*, C.-Y. Li*, C.-H. Chien*, C.-I. Su**, W.-S. Khwa**, J.-J. Wu**, C.-C. Lo*, R.-S. Liu*, C.-C. Hsieh*, K.-T. Tang*, M.-S. Ho***, Y.-D. Chih**, T.-Y. J. Chang** and M.-F. Chang*, **, *National Tsing Hua Univ., **TSMC and ***National Chung Hsing Univ., Taiwan

Tiny AI edge processors prefer using nvCIM to achieve low standby power, high energy efficiency (EF), and short wakeup-to-response latency (T_{WR}). Most nvCIMs use in-memory computing for MAC operations; however, this imposes a tradeoff between EF and accuracy, due to MAC accumulation-number (N_{ACU}) versus signal margin and readout quantization. To achieve high EF and high accuracy, we developed a system-level nvCIM-friendly control scheme and a nvCIM macro with two analog near-memory computing schemes. The proposed 28nm nonvolatile AI edge processor with 4Mb ReRAM-nvCIM achieved high EF (27.2 TOPS/W), short T_{WR} (3.19ms), and low accuracy loss (<0.5%) The EF of the ReRAM-nvCIM macro was 38.6 TOPS/W.

C10-3 - 11:20
Scaling-CIM: An eDRAM-Based In-Memory-Computing Accelerator with Dynamic-Scaling ADC for SQNR-Boosting and Layer-Wise Adaptive Bit-Truncation, S. Kim, S. Um, W. Jo, J. Lee, S. Ha, Z. Li and H.-J. Yoo, KAIST, Korea

This paper presents Scaling-CIM, an energy-efficient eDRAM-IMC with the dynamic-scaling readout for SQNR boosting and ADC overhead reduction. Dynamic Scaling ADC boosts SQNR of multi-bit operation even with low-bit ADC. Adaptive analog bit-parallel accumulation reduces the redundant ADC operation. Also, layer-wise adaptive bit-truncation search further enhances efficiency on benchmarks. The accelerator is fabricated in 28nm CMOS technology and occupies 2.03mm² die area. It achieves 39.7 TOPS/W energy efficiency on ResNet-18 benchmark and 6.8 times higher efficiency FoM compared to the previous IMC-based accelerator.

C10-4 - 11:45
A 12nm 137 TOPS/W Digital Compute-In-Memory Using Foundry 8T SRAM Bitcell Supporting 16 Kernel Weight Sets for AI Edge Applications, G. Jedhe, C. Deshpande, S. Kumar, C.-X. Xue, Z. Guo, R. Garg, K. S. Jway, E.-J. Chang, J. Liang, Z. Wan and Z. Pan, MediaTek Inc., USA

This paper presents a Digital Compute-In-Memory design in 12nm FinFET technology with capacity to store weights for 16 kernels per input channel. This macro is designed using an 8T SRAM push-rule foundry bitcell with integrated kernel selection and multiplication for an AI Edge application that achieves 30% better TOPS/mm^2 without loss of TOPS/W than a comparable logic-rule custom bitcell based architecture on the same silicon. We present novel power saving architectures, Activation Based Precharge and Folded Kernel Selector that achieves 11.2 TOPS/mm^2 and 137 TOPS/W with highest reported 16 kernels per input channel. Further, we showcase novel design circuitry to reduce peak current by 69.1% using a new Precharge During Write scheme.

C10-5 - 12:10
SP-PIM: A 22.41TFLOPS/W, 8.81Epochs/Sec Super-Pipelined Processing-In-Memory Accelerator with Local Error Prediction for On-Device Learning, J.-H. Kim, J. Heo, W. Han, J. Kim and J.-Y. Kim, KAIST, Korea

This paper presents SP-PIM that demonstrates real-time on-device learning based on the holistic, multi-level pipelining scheme enabled by local error prediction. It introduces the local error prediction unit to make the training algorithm pipelineable, while reducing computation overhead and overall external memory access based on power-of-two arithmetic operations and random weights. Its double-buffered PIM macro is designed for performing both forward propagation and gradient calculation, while the dual-sparsity-aware circuits exploit sparsity in activation and error. Finally, the 5.76mm^2 SP-PIM chip fabricated in 28nm process achieves 8.81Epochs/Sec model training on chip with the state-of-the-art 560.6GFLOPS/mm^2 area efficiency and 22.4TFLOPS/W power efficiency.

Technology Session 7

Highlight 2 [Shunju I+II+III]

Wednesday, June 14, 10:30-12:35

Chairpersons M. Kobayashi, The Univ. of Tokyo
F. Arnaud, STMicroelectronics N.V.

T7-1 - 10:30
Highly Scalable Metal Induced Lateral Crystallization (MILC) Techniques for Vertical Si Channel in Ultra-High (> 300 Layers) 3D Flash Memory, N. Ishihara*, Y. Shimada*, T. Ochi*, S. Seto*, H. Matsuo*, H. Yamashita*, S. Morita*, M. Ukishima*, K. Uejima*, Y. Arayashiki*, S. Kajiwara*, K. Nishiyama*, A. Murayama*, K. Sugimae*, S. Mori*, Y. Saito*, T. Shundo*, A. Maeda*, H. Kamiya**, Y. Uchiyama*, M. Fujiwara*, F. Aiso*, K. Sekine* and N. Ohtani*, *KIOXIA Corp. and **Western Digital Corp., Japan

State-of-the-art Metal Induced Lateral Crystallization (MILC) techniques have been demonstrated for 3D flash memory with ultra-high (over 300) layers. For the first time, 14-μm-long macaroni silicon (Si) channels in vertical memory hole are fully single-crystallized. Furthermore, by using newly developed Ni gettering technique, the 112 word-line-layer 3D flash memory exhibits cell array performances such as read noise reduction of 40% or more, and 10-times channel conductance without any degradations of cell reliability.

T7-2 - 10:55
QLC Programmable 3D Ferroelectric NAND Flash Memory by Memory Window Expansion Using Cell Stack Engineering, S. Yoon, S.-I. Hong, D. Kim, G. Choi, Y. M. Kim, K. Min, S. Kim, M.-H. Na and S. Cha, SK hynix Inc., Korea

3D ferroelectric NAND (Fe-NAND) Quad-level cell (QLC) operation has been demonstrated for the first time to our knowledge, using the 3D CTN NAND test vehicle for mass production. The 3D Fe-NAND is optimized by engineering the cell stack layers, enlarging a program/erase (PE) window up to 10.5 V. QLC operation is successfully verified with the minimum gap margin of 0.24 V. Endurance and data retention characteristics are also reported.

T7-3 - 11:20
First Observation of Ultra-high Polarization (~ 108 μC/cm^2) in Nanometer Scaled High Performance Ferroelectric HZO Capacitors with Mo Electrodes, F. Huang*, B. Saini*, L. Wan**, H. Lu***, X. He****, S. Qin*, W. Tsai*, A. Gruverman***, A. C. Meng****, H.-S. P. Wong*, P. C. McIntyre*, ***** and S. S. Wong*, *Stanford Univ., **Western Digital Corp., ***Univ. of Nebraska-Lincoln, ****Univ. of Missouri and *****SLAC National Accelerator Laboratory, USA

We demonstrate, for the first time, excellent ferroelectricity, and endurance of 4 nm-thick and 65 nm x 45 nm size $Hf_{0.5}Zr_{0.5}O_2$ (HZO) capacitors with Mo electrodes. We show 1) the crystallization temperature is as low as 400 °C, which is critical for BEOL FeRAM; 2) benefits from thickness scaling, low operation voltage (1.2 V) and high endurance (> 10^{10} cycles) are achieved; 3) the wake-up effect is further reduced to 20 % and the beginning of fatigue is delayed by an order of magnitude by adding a 1 nm CeO_2 stressor layer; and 4) direct measurements of ferroelectricity with ultra-high polarization switching (*~108 μC/cm^2*) in devices scaled down to 95 nm x 85 nm size. This study advances the understanding of scaling effect in HZO capacitors.

T7-4 - 11:45
Noise Performance Improvements of 2-Layer Transistor Pixel Stacked CMOS Image Sensor with Non-doped Pixel-FinFETs, Y. Kikuchi*, M. Tomita*, T. Hayashi*, H. Chiba*, T. Ogita*, T. Okawa*, K. Nishida*, M. Sugimoto*, D. Yoneyama**, T. Umeki**, H. Oishi*, S. Miyake*, K. Hiramatsu*, H. Kumano*, H. Kawashima**, N. Yamada**, M. Tamura**, H. Ohnuma* and K. Tatani*, *Sony Semiconductor Solutions Corp. and **Sony Semiconductor Manufacturing Corp., Japan

For the first time, 2-Fin non-doped Pixel-Fin field-effect-transistors (3D pixel transistors) are introduced into a 2-Layer Transistor Pixel stacked CMOS image sensor (0.6 um pixel size) to improve CMOS image sensor noise performance. In this device architecture, photo diode exists on the 1st layer while the pixel transistors exist on the 2nd layer, and this device architecture is ideal to form the non-doped channel for pixel transistors because of no unintentional impurity diffusion from photo diode into pixel transistors. The non-doped channel forms the carrier flow path, including a region away from the influence of an oxide trap and channel interface, and it should better improve noise characteristics than the doped channel. Additionally, 3D transistor can increase channel width under fixed footprint. Thanks to the non-doped channel and wider channel width, a 2.42-time transconductance improvement, 15% random noise and 99.3% random telegraph signal reductions are obtained.

T7-5 - 12:10
Cryogenic RF Transistors and Routing Circuits Based on 3D Stackable InGaAs HEMTs with Nb Superconductors for Large-Scale Quantum Signal Processing, J. Jaeyong*, K. Seong Kwang*, S. Yoon-Je*, L. Jisung**, C. Joonyoung***, P. Juhyuk*, K. Joon Pyo*, K. Bong Ho*, J. Younjung***, P. Seung-Young**, K. Jongmin**** and K. Sanghyeon*, *KAIST, **Korea Basic Science Institute (KBSI), ***Kyungpook National Univ. and ****Korea Advanced NanoFab Center (KANC), Korea

Cryogenic RF transistors and routing circuits operating with extremely low power are essential as control/readout electronics for future large-scale quantum computing (QC) systems. In this work, we demonstrate 3D stackable InGaAs HEMT-based cryogenic RF transistors and routing circuits integrated with Nb superconductors for ultra-low power operation. As a result, we achieve a record high unity current gain cutoff frequency (f_T) of 601 GHz and unity power gain cutoff frequency (f_{MAX}) of 593 GHz at 4 K with the smallest power dissipation among ever reported cryogenic RF transistors. Furthermore, using a novel structure with Nb superconductor and III-V heterostructure hybrid interconnect of the routing circuits, we achieve high-performance routing circuits with 41% lower power dissipation compared to the conventional structure.

Circuits Session 11

DC-DC Converter [Suzaku III]

Wednesday, June 14, 14:00-15:40

Chairpersons: P. H. Chen National Yang Ming Chiao Tung Univ.
M. Rose NXP Semiconductors N.V.

C11-1 - 14:00
A 0.05-to-3.1A 585mA/mm³ 97.3%-Efficiency Outphase Switched-Capacitor Hybrid Buck Converter with Relieved Capacitor Inrush Current and C_{OUT}-Free Operation, X. Zhang*, Q. Ma*, A. Zhao*, Y. Jiang*, M.-K. Law*, P.-I. Mak* and R. Martins*,**, *Univ. of Macau, Macau and **Univ. of Lisboa, Portugal

This work presents a hybrid buck converter with improved heavy-and-light load efficiency and enhanced power (current) density. The proposed converter uses outphase-interleaved switched-capacitor (OISC) cells to relieve the flying capacitor (C_F) inrush current under extreme duty-ratios (D). It can also operate without an output capacitor (C_{OUT}), improving the overall form factor. Besides, the intrinsic topological property realizes inductor-current recycling, which boosts the light-load efficiency without discontinuous-conduction mode (DCM) control. We also propose a self-hold gate driving scheme using a shared charge pump to eliminate the off-chip bootstrapping capacitors (C_{BST}). Fabricated in 180-nm BCD, the prototype supports a wide-range load current (I_{LOAD}) of 0.05-3.1A and converts a 1.8-3.3V input to a 0.8-1.8V output with a peak efficiency of 97.3%, and a peak current density of 585mA/mm³. With zero C_{OUT}, the measured output ripple is below 60mV at 1.8V_{OUT} and 3.1A I_{LOAD}.

C11-2 - 14:25
96.48% Peak-Efficiency Continuous-Current Step-Up Battery Charger (CC-SUBC) with Dual Energy-Harvesting Sources for Automotive Application, H.-J. Park, J.-M. Cho, H.-J. Choi, C.-H. Lee and S.-W. Hong, Sogang Univ., Korea

This paper proposes a continuous-current step-up battery charger (CC-SUBC) for electronic or hybrid vehicles. The proposed charger can simultaneously extract power from dual energy harvesting sources (V_{PV} and V_{TEG}), of which voltages are lower than the output battery voltage (V_{BAT}). In addition, the CC-SUBC charges the battery with a continuous output current (I_O) although it operates as a step-up converter. Peak efficiency was obtained as 96.48%, which is not only the highest peak efficiency but also the largest maximum output power among the state-of-the-art step-up converters.

C11-3 - 14:50
A 19.8W/29.6W Hybrid Step-Up/Down DC-DC Converter with 97.2% Peak Efficiency for 1-Cell/2-Cell Battery Charger Applications, S. Yeo*, U. Hyeon*, M. Kim*, J. Kim** and K. Cho*, *Kyungpook National Univ. and **Hanbat National Univ., Korea

This paper presents an inductor-first hybrid step-up/down DC-DC converter for one- and two-cell battery chargers. The proposed architecture can improve efficiency by lowering inductor current as well as less charge sharing loss of the flying capacitor. The battery can be isolated from the input without using extra reverse blocking device which is necessary for the charger application. The design also can replace the discrete inductor with the USB cable inductance and avoid heat loss from the mobile device. The proposed converter has been implemented in a 180nm BCDMOS process. The peak efficiency is 96.9% at 5V input for one-cell, and 97.2% at 9V input for two-cell battery. The measured maximum output power is 19.8W and 29.6W for one-cell and two-cell battery applications, respectively. The on-board peak efficiency is 96% employing the USB cable.

C11-4 - 15:15
A 4.1W/mm² Peak Power Density and 77% Peak Efficiency Fully Integrated DC-DC Converter Based on Electromagnetically Coupled Class-D LC Oscillators and a Resonant LC Flying Impedance in 22nm FDSOI CMOS, A. Novello, G. Atzeni, T. Keller and T. Jang, ETH Zurich, Switzerland

This paper presents a fully integrated DC-DC converter based on electromagnetically coupled class-D LC oscillators. The proposed converter features a hybrid LC flying impedance, Z_{FLY}, which lowers the converter output resistance ROUT by introducing a resonant charge exchange with the output capacitor CO. The improved ROUT provides a peak efficiency of 77% and a peak power density of 4.1W/mm^2, marking a significant improvement with respect the state-of-the-art. The output voltage regulation is obtained with a duty-cycling control scheme that maintains the efficiency loss <2% from 0.003W/mm^2 up to 2.1W/mm^2. The proposed DC-DC converter is fabricated in a 22nm FDSOI CMOS process with a total area of 0.33mm^2.

Circuits Session 12

Digital Building Blocks [Suzaku II]

Wednesday, June 14, 14:00-15:40

Chairpersons: N. Miura, Osaka Univ.
C. Tokunaga, Intel Corp.

C12-1 - 14:00
A Fully Synthesizable 100Mbps Edge-Chasing True Random Number Generator, Y. He and K. Yang, Rice Univ., USA

This paper presents a fully synthesizable True Random Number Generator (TRNG) based on edge chasing in even-stage ring oscillators (RO). The proposed configurable RO with an automatic self-calibration loop enables robust high-speed operations and high-quality outputs under -40 to 125°C and 0.7 to 1.2V conditions, digital layout mismatch and process variations, and power injection attacks. Ten 65nm prototypes designed in unmodified digital flow using only foundry standard cells demonstrate random bit generation at up to 100.8Mbps and pass all NIST tests without post-processing.

C12-2 - 14:25
218Kauth/S, 3nJ/Auth SCA/ML-Resistant Privacy-Preserving Mutual Authentication Accelerator with a Crypto-Double-Coupled PUF in 4nm Class CMOS, S. Taneja, V. Suresh, R. Kumar, V. De and S. Mathew, Intel Corp., USA

A SCA/ML-resistant secure PPMA accelerator is fabricated in 4nm class CMOS. Double-coupled crypto microarchitecture using a 128b strong PUF along with AES-128 round hardware achieves CRP space of 10^{28} with BER of 0.15%. Secure mote/server-authentication throughput of 218/435Kauth/s is demonstrated with no side-channel leakage detected after 2.5M authentications. Resistance to machine-learning attacks is demonstrated against 10M training CRPs.

C12-3 - 14:50
ECC-Less Multi-Level SRAM Physically Unclonable Function and 127% PUF-to- Memory Capacity Ratio with No Bitcell Modification in 28nm, J. Basu, S. Taneja, V. Konandur Rajanna, T. Wang and M. Alioto, National Univ. of Singapore, Singapore

A multi-level (2 bits/bitcell) SRAM PUF is introduced to uniquely enable ECC-less operation with PUF capacity exceeding storage capacity at no cell modification. The first PUF bit is generated from steady-state post-reset bitcell value with >4X higher stability than conventional power-up. The second is simultaneously extracted from the transient response. Above-storage capacity and improved stability eliminate ECC down to the SRAM V_{min} (0.6 V) at 75-fJ/bit energy and 3.3% area overhead in 28 nm.

C12-4 - 15:15
A Static Contention-Free Dual-Edge-Triggered Flip-Flop with Redundant Internal Node Transition Elimination for Ultra-Low-Power Applications, S. Kim*, K. Cho*, K. Baek*, H. Kim**, Y. Bae**, M. Kim**, D. Seo**, S. Baeck**, S. Lee** and S.-O. Jung*, *Yonsei Univ. and **Samsung Electronics Co., Ltd., Korea

This paper presents a dual-edge-triggered flip-flop (DET-FF) with redundant internal node transition elimination (RTEDET) to achieve minimal dynamic power consumption. The proposed RTEDET shows lower total power by 37%/39% than the recent low-power flip-flop/conventional DET-FF thanks to the halved CK frequency and the redundant internal node transition elimination. In addition, the proposed RTEDET can operate at supply voltage down to 0.35V in all chips with its static operation and contention-free feature.

Circuits Session 13

Millimeter-Wave Transceivers and Synthesizers [Suzaku I]

Wednesday, June 14, 14:00-15:40

Chairpersons: K. Okada, Tokyo Institute of Technology
N. Kocaman, Broadcom Limited, Inc.

C13-1 - 14:00
A Sub-THz Full-Duplex Phased-Array Transceiver with Self-Interference Cancellation and LO Feedthrough Suppression, C. Wang, I. Abdo, C. Liu, C. da Gomez, H. Herdian, W. Wang, X. Fu, D. You, A. Shehata, S. Park, Y. Wang, J. Pang, H. Sakai, A. Shirane and K. Okada, Tokyo Institute of Technology, Japan

This paper presents a sub-THz (88-136GHz) full-duplex phased-array transceiver integrating an RF self-interference canceller with differential-feeding full-duplex antennas. The LO phase generation chain controls differential transmitter outputs for the phased-array operation. In the over-the-air measurement, the proposed full-duplex transceiver achieves 6Gb/s in 8PSK and 4Gb/s in 16QAM. The self-interference suppression is improved by 20dB when the self-interference canceller is turned on. The transceiver also achieves a 112Gb/s data rate by wideband amplifiers and the neutralized mixer.

C13-2 - 14:25
An 11.4-to-16.4GHz FMCW Digital PLL with Cycle-Slipping Compensation and Back-Tracking DPD Achieving 0.034% RMS Frequency Error under 3.4-GHz Chirp Bandwidth and 960-MHz/μs Chirp Slope, A. Yan, W. Deng, H. Jia, S. Sun, C. Tang, B. Zhu, Y. Fu, H. Liu and B. Chi, Tsinghua Univ., China

This article introduces a digital FMCW PLL with cycle-slipping compensation scheme and wideband digital-to-time converter (DTC) gain calibration to break the limitation of the maximum trackable chirp slope for two-point modulation (TPM) FMCW PLLs. In addition, FM error is minimized by the proposed back-tracking digital-pre-distortion (DPD) scheme. As far as the authors are aware, the proposed FMCW PLL achieves the widest normalized chirp bandwidth and the fastest normalized chirp slope concurrently while retaining decent chirp linearity.

C13-3 - 14:50
An 18.8-to-23.3 GHz ADPLL Based on Charge-Steering-Sampling Technique Achieving 75.9 fs RMS Jitter and –252 dB FoM, W. Tao*, W. Zhao*, R. B. Staszewski**, F. Lin* and Y. Hu*, *Univ. of Science and Technology of China, China and **Univ. College Dublin, Ireland

We propose a mm-wave all-digital PLL (ADPLL) based on a new concept of a charge-steering-sampling (CSS) digital phase detection (PD). The CSS-PD operation is formed by first, presetting the input capacitors of a SAR-ADC to V_{DD}, then discharging them during a reference pulse via a pseudo-differential-pair (pseudo-diff-pair) directly driven by the oscillator. The differential-mode (DM) charge-residue, representing the phase error, is evaluated by the ADC for supporting the ADPLL operation. This new technique promotes a high PD gain, good isolation of the oscillator, and a multi-bit digital PD output simultaneously, fully benefiting from the advanced CMOS. Further, a digital loop filter (DLF) with a dead-zone (DZ) in the integral path is proposed to avoid any conflicts with the proportional path. Fabricated in 22-nm CMOS, the prototype achieves 75.9 fs RMS jitter, <-50 dBc spur, and -252.4 dB FoM from 18.8 to 23.3 GHz.

C13-4 - 15:15
A 24-30 GHz Cascaded QPLL Achieving 56.8-fs RMS Jitter and –248.6-dB FoMjitter, L. Wang, Z. Liu and C. P. Yue, Hong Kong Univ. of Science and Technology, China

This paper presents a 24-30 GHz quadrature phase-locked loop (QPLL) by cascading a 1st-stage low-jitter 7-GHz sub-sampling PLL (SSPLL) and a 2nd-stage wideband 28-GHz dual-path (DP) SSPLL. A wide dynamic range ac-coupled SS-charge pump (AC-SSCP) is proposed in the 1st-stage PLL to reduce the offset current in its output for lower jitter. The 2nd-stage SSPLL boosts SS-phase detector (SSPD) gain using a dual-path topology to attain a 100-MHz wide loop bandwidth for suppressing the QVCO contribution to the overall output phase noise. Fabricated in 40-nm CMOS, the prototype achieves 56.8-fs integrated rms jitter, -55.6-dBc reference spur, -248.6-dB FoMjitter, and < 7.0-fs jitter variation across the AC-SSCP output range (0.16-0.92 V) under a 1.1-V supply.

Technology / Circuits Joint Focus Session 2

AR/VR/MR Metaverse 1 [Shunju III]

Wednesday, June 14, 14:00-15:15

Chairpersons: K. Nii, TSMC Design Technology Japan, Inc.
T. Letavic, GLOBALFOUNDRIES Inc.

JFS2-1 - 14:00 (Invited)
(TBD), E. Beigne, Meta, USA

JFS2-2 - 14:25
A Back-Illuminated 6 μm SPAD Depth Sensor with PDE 36.5% at 940 nm via Combination of Dual Diffraction Structure and 2×2 On-Chip Lens, Y. Fujisaki*, H. Tsugawa*, K. Sakai*, H. Kumagai*, R. Nakamura*, T. Ogita*, S. Endo*, T. Iwase*, H. Takase*, K. Yokochi*, S. Yoshida*, S. Shimada*, Y. Otake*, T. Wakano*, H. Hiyama*, K. Hagiwara*, M. Arakawa*, S. Matsumoto*, H. Maeda**, K. Sugihara**, K. Takabayashi**, M. Ono**, K. Ishibashi** and K. Yamamoto**, *Sony Semiconductor Solutions Corp. and **Sony Semiconductor Manufacturing Corp., Japan

We present a back-illuminated 3D-stacked 6 um single-photon avalanche diode (SPAD) sensor with very high photon detection efficiency (PDE) performance. To enhance PDE, a dual diffraction structure was combined with 2x2 on-chip lens (OCL) for the first time. A dual diffraction structure comprises a pyramid surface for diffraction (PSD) and periodic uneven structures by shallow trench for diffraction formed on the Si surface of light-facing and opposite sides, respectively. Additionally, PSD pitch and SiO_2 film thickness buried in full trench isolation were optimized. Consequently, a PDE of 36.5% was achieved at wavelength of 940 nm, the world's highest value.

JFS2-3 - 14:50
Human Activity Recognition SoC for AR/VR with Integrated Neural Sensing, AI Classifier and Chained Infrared Communication for Multi-Chip Collaboration, Y. Wei, X. Chen and J. Gu, Northwestern Univ., USA

This paper presents a distributed multi-chip human activity recognition system for Virtual Reality (VR) and Augmented Reality (AR) applications. A comprehensive solution is delivered, including AI core for classification, analog sensing for neural activity detection, and infrared data communication for multi-chip collaboration. A 65nm test chip is fabricated and distributed across the body area to demonstrate the low power, low latency, and camera-free features of the target applications.

Technology Focus Session 1

Future Memory Directions [Shunju II]

Wednesday, June 14, 14:00-15:40

Chairpersons: H-T. Lue, Macronix International Co., Ltd.
S. Yu, Georgia Institute of Technology

TFS1-1 - 14:00 (Invited)
Ongoing Evolution of DRAM Scaling via Third Dimension - Vertically Stacked DRAM -, J.-W. Han, S. H. Park, M. Y. Jeong, K. S. Lee, K. N. Kim, H. J. Kim, J. C. Shin, S. M. Park, S. H. Shin, S. W. Park, K. S. Lee, J. H. Lee, S. H. Kim, B. C. Kim, M. H. Jung, I. Y. Yoon, H. Kim, S. U. Jang, K. J. Park, Y. K. Kim, I. G. Kim, J. H. Oh, S. Y. Han, B. S. Kim, B. J. Kuh and J. M. Park, Samsung R&D Center, Korea

For the past decades, the density of DRAM has been remarkably increased by making access transistors and capacitors smaller in size per unit area. However, shrinking devices far beyond the 10 nm process node increasingly poses process and reliability challenges. As Flash technology made a pivotal and successful innovation via 3D NAND, DRAM technology may also adopt vertical stacking memory cells. Vertically stacked DRAM (VS-DRAM) continues to increase bit density on a die by increasing the number of layers along with reducing the size of the transistor. In this paper, the opportunities and challenges of VS-DRAM are discussed.

TFS1-2 - 14:25 (Invited)
Phase Change Memory-based Hardware Accelerators for Deep Neural Networks, G. W. Burr*, P. Narayanan*, S. Ambrogio*, A. Okazaki**, H. Tsai*, K. Hosokawa**, C. Mackin*, A. Nomura**, T. Yasuda**, J. Demarest***, K. W. Brew***, V. Chan***, S. Choi***, T. Gordon***, T. M. Levin***, A. Friz*, M. Ishii**, Y. Kohda**, A. Chen*, A. Fasoli*, J. Luquin*, N. Saulnier***, S. Teehan***, I. Ahsan*** and V. Narayanan****, *IBM Research - Almaden, USA, **IBM Research - Tokyo, Japan, ***IBM Albany NanoTech and ****IBM T. J. Watson Research Center, USA

Analog non-volatile memory (NVM)-based accelerators for deep neural networks implement multiply-accumulate (MAC) operations – in parallel, on large arrays of resistive devices – by using Ohm's law and Kirchhoff's current law. By completely avoiding weight motion, such fully weight-stationary systems can offer a unique combination of low latency, high throughput, and high energy-efficiency (e.g., high TeraOPS/W). Yet since most Deep Neural Networks (DNNs) require only modest (e.g., 4-bit) precision in synaptic operations, such systems can still deliver "software-equivalent" accuracies on a wide range of models. We describe a 14-nm inference chip, comprising multiple 512512 arrays of Phase Change Memory (PCM) devices, which can deliver software-equivalent inference accuracy for MNIST handwritten-digit recognition and recurrent LSTM benchmarks, and discuss various PCM challenges such as conductance drift and noise.

TFS1-3 - 14:50
Non-Destructive-Read 1T1C Ferroelectric Capacitive Memory Cell with BEOL 3D Monolithically Integrated IGZO Access Transistor for 4F² High-Density Integration, Z. Zhou*, L. Jiao*, Q. Kong*, Z. Zheng*, K. Han*, Y. Chen*, C. Sun*, B.-Y. Nguyen** and X. Gong*, *National Univ. of Singapore, Singapore and **Soitec, France

For the first time, we experimentally demonstrate a 1T1C ferroelectric capacitive memory (FCM) cell by vertically stacking the high-performance inversion-type FCM with the back-end-of-line (BEOL) IGZO channel access transistor having SS of 70 mV/decade. Based on the 1T1C configuration, we design and demonstrate a reading scheme by charge sharing between FCM and bit line capacitor. Thanks to the low write current of FCM, IGZO FET can provide sufficient current for the effective write operation even in highly scaled cells. With the 3D monolithic integration capability of IGZO FETs, we further propose a 1T1C FCM array structure to realize the highest density with 4F² 1T1C cell size by stacking two layers of IGZO access transistors on top of the memory. We also validate the operation of the highly scaled 4F² 1T1C cell with experiment-calibrated TCAD and SPICE simulation and predict that the 1T1C configuration is able to improve the delay

TFS1-4 - 15:15
Foundry Monolithic 3D BEOL Transistor + Memory Stack: Iso-Performance and Iso-Footprint BEOL Carbon Nanotube FET+RRAM vs. FEOL Silicon FET+RRAM, T. Srimani*, A. C. Yu**, R. M. Radway*, D. T. Rich*, M. Nelson***, S. Wong*, D. Murphy****, S. Fuller****, G. Hills**, *****, S. Mitra* and M. M. Shulaker**, ****, *Stanford Univ., **MIT, ***SkyWater Technology Foundry, ****Analog Devices, Inc. and *****Harvard Univ., USA

We show, for the first time, a BEOL carbon nanotube FET (CNFET)+ Resistive RAM (RRAM) stack through monolithic 3D (M3D) integration, directly over silicon CMOS, that *achieves comparable performance* (read power, write energy/latency, endurance, retention, multiple bits-per-cell capability) *in the same footprint* as conventional RRAM stack using FEOL Si FET access transistors. This process is established within SkyWater Technology Foundry (90/130nm technology node on 200mm Si wafers). An apples-to-apples comparison is made versus FEOL Si FET+RRAM fabricated on the same wafers, from the same foundry, at the same node. Such BEOL CNFET+RRAM technology unlocks a large architecture design space with significant system-level energy-delay product (EDP) benefits vs. FEOL Si+RRAM-only designs, e.g., >5x EDP benefits for new iso-footprint, iso-memory-capacity M3D architectures uniquely enabled by our M3D physical design. Our BEOL CNFET+RRAM therefore creates a new and complementary integration path for dramatically improving system-level energy and delay, iso-node and iso-footprint.

Technology Session 8

Logic Technology 2: Advanced Processes [Shunju I]

Wednesday, June 14, 14:00-15:40

Chairpersons: T. Ohtou, Tokyo Electron Limited
A. Agrawal, Intel Corp.

T8-1 - 14:00
Building High Performance Transistors on Carbon Nanotube Channel, G. Pitner*, N. Safron*, T.-A. Chao**, S. Li***, S.-K. Su**, G. Zeevi***, Q. Lin***, H.-Y. Chiu**, M. Passlack*, Z. Zhang****, D. M. Sathaiya**, A. Wei**, C. Gilardi***, E. Chen**, S.-L. Liew**, V. D.-H. Hou**, C.-W. Wu**, J. Wu**, Z. Lin*****, J. Fagan*****, M. Zheng*****, H. Wang*, S. Mitra***, H.-S. P. Wong**, *** and I. Radu**, *TSMC, USA, **TSMC, Taiwan, ***Stanford Univ., ****Univ. of California, San Diego and *****National Institute of Standard & Technology (NIST), USA

High-performance and scaled transistors on carbon nanotube (CNT) channel are enabled by the quality of device component modules. This paper advances each module by single-CNT control experiments reporting: (1) remarkable n-type contact resistance of 5.1 kΩ/CNT at 20 nm contact length, (2) tunable N- and P-doping of CNT with dielectric doping, (3) improvement in top-gate dielectric interface to CNT by channel cleaning, (4) demonstration of channel with dense CNT array with low bundle density, and (5) analysis of CNT bandgap tradeoffs with variability control strategy. The first component-complete pMOS FET is demonstrated on high-density CNTs with up to 680 μA/μm at -0.7V V_{ds}.

T8-2 - 14:25
Record High Active Boron Doping Using Low Temperature *In-situ* CVD: Enabling Sub-5×10^{-10} Ω-cm² ρ_c from Cryogenic (5 K) to Room Temperature, G. Zheng*, Y. Wang*, H. Xu*, R. Khazaka**, L. Muehlenbein**, S. Luo*, X. Chen*, R. Shao*, Z. Zheng*, G. Liang* and X. Gong*, *National Univ. of Singapore, Singapore and **ASM International, Belgium

We report the first demonstration of active boron (B) doping concentration (N_A) higher than 2.50e21 cm^{-3} in high Ge content (> 65%) Si1-xGex using in-situ growth technique with an ultra-low temperature lower than 400 oC. We achieve excellent uniformities of $Si_{1-x}Ge_x$ thickness and resistivity across the entire 300 mm wafer and obtain an ultra-low as-deposited specific contact resistivity (ρ_c) down to 2.9±2.8e-10 Ω-cm² on the sample with a high average active doping concentration (N_A) of 2.80e21 cm^{-3} and Ge composition of 65%. We further detail the progression of the selective growth of such $Si_{1-x}Ge_x$ film on advanced 3D structures. Using metal $Si_{1-x}Ge_x$ ladder TLM (LTLM) structures, we investigate the contact properties from room temperature to cryogenic temperatures as low as 5 K, disclosing for the first time the insignificant change of ρ_c at such ultra-low ρ_c regimes.

T8-3 - 14:50
L_g = 60 nm $In_{0.53}Ga_{0.47}As$ MBCFETs: From g_{m_max} = 13.7 mS/μm and Q = 180 to Virtual-Source Modeling, J.-H. Yoo*, H.-B. Jo*, I.-G. Lee*, S.-M. Choi*, J.-M. Baek*, S. T. Lee**, H.-C. Jang**, M. W. Kong**, H.-H. Kim*, H.-J. Lee*, H.-J. Kim*, H.-S. Jeong*, W.-S. Park*, D.-H. Ko***, S. H. Shin*****, H.-M. Kwon*****, S.-K. Kim******, J.-g. Kim******, J. Yun******, T. Kim******, K.-Y. Shin****, T.-W. Kim****, J.-K. Shin*, J.-H. Lee*, C.-S. Shin**, K.-S. Seo** and D.-H. Kim*, *Kyungpook National Univ., **Korea Advanced NanoFab Center (KANC), ***Yonsei Univ., ****Univ. of Ulsan, *****Korea Polytechnics and ******QSI, Korea

In this paper, we report scalable 5-level stacked gate-all-around (GAA) $In_{0.53}Ga_{0.47}As$ multi-bridge channel FETs (MBCFETs), with careful attention paid to fluorine migration. At its heart, we maintained temperature of all the unit process steps below 300°C and inserted an n-InP ledge into a top $In_{0.52}Al_{0.48}As$ sacrificial layer to suppress F^--induced donor passivation. In addition, we used a selectively regrown *n*+ $In_{0.53}Ga_{0.47}As$ contact formation by MOCVD and precision dry etching. The dry etching process resulted in a highly vertical etching slope along both the S/D and W_g directions. The fabricated L_g = 60 nm MBCFET showed a record combination of S = 76 mV/dec, g_{m_max} = 13.7 mS/μm, I_{ON} = 2.24 mA/μm and Q = 180 at V_{DS} = 0.5 V.

T8-4 - 15:15
High Performance 5 nm Si Nanowire FETs with a Record Small SS = 2.3 mV/dec and High Transconductance at 5.5 K Enabled by Dopant Segregated Silicide Source/Drain, Y. Han*, J. Sun*, J.-H. Bae*, D. Gruetzmacher*, J. Knoch** and Q.-T. Zhao*, *Forschungszentrum Jülich and **RWTH Aachen Univ., Germany

The effect of band edge states is the critical issue for cryogenic CMOS, which worsens the performance of conventional MOSFETs at cryogenic temperature with saturated subthreshold swing (SS), large transition region (inflection phenomenon) and limited mobility. To address these problems, we fabricated gate-all-around (GAA) Si nanowire (NW) MOSFETs using fully silicided source/drain and dopant segregation. The effect of band edge states is significantly suppressed using this technology. Thus, SS, the effective average SS_{th} and the transconductance (G_m) continuously improve as temperature decreases allowing us to achieve high performance NW FETs at 5.5 K with a record small SS of 2.3 mV/dec, ultra-small DIBL of 0.02 mV/V, and high G_m of 1.25mS/μm.

Circuits Session 14

Nyquist-Rate ADCs [Suzaku III]

Wednesday, June 14, 16:00-17:40

Chairpersons: M. Fukazawa, Renesas Electronics Corp.
V. Chen, Carnegie Mellon Univ.

C14-1 - 16:00
A 2GS/s 11b 8x Interleaved ADC with 9.2 ENOB and 69.9dB SFDR in 28nm CMOS, L. Ricci, L. Scaletti, G. Be, M. Rocco, L. Bertulessi, S. Levantino, A. Lacaita, C. Samori and A. Bonfanti, Politecnico di MIlano, Italy

A 2GS/s 11b 8x-interleaved ADC is presented where flipped-voltage-follower-based reference buffers attenuate channel interactions and a set of on-chip background digital calibrations mitigate channel mismatches. A high-linearity input buffer is included which does not degrade ADC performances. Implemented in a 28nm CMOS technology, the ADC achieves 57.3dB SNDR and 69.9dB SFDR close to the Nyquist frequency. The interleaved ADC maintains (within 1.2 dB) the same SNDR level of the individual channel over the 1GHz input bandwidth.

C14-2 - 16:25
A 79.5dB-SNDR Pipelined-SAR ADC with a Linearity-Shifting 32× Dynamic Amplifier and Mounted-Over-Die Bypass Capacitors, M. Zhang*, Y. Cao*, Y. Zhu*, C.-H. Chan* and R. P. Martins*, **, *Univ. of Macau, Macau and **Universidade de Lisboa, Portugal

This paper presents a 32x low-noise dynamic amplifier (DA) with a linearity-shifting technique, facilitating a 15b pipelined-SAR ADC with 80dB $SNR_{@DC}$. The linearity-shifted DA decouples the fundamental conflict between the noise and linearity in conventional DAs, rending a THD below -60dB at $0.8V_{pp,diff}$ output swing. Moreover, the reference voltages are stabilized by the cost-effective mounted-over-die bypass capacitors. The 60MS/s ADC achieves 95.8dB and 87.3dB SFDR with a DC and Nyquist input, respectively, and an input noise density of 10.2nV/√Hz.

C14-3 - 16:50
A 150-MS/s Fully Dynamic SAR-Assisted Pipeline ADC Using a Floating Ring Amplifier and Gain-Enhancing Miller Negative-C, S. Song*, T. Kang*, **, S. Lee*, ***, and M. P. Flynn*, *Univ. of Michigan, **Apple, Inc. and ***Qualcomm Technologies, Inc., USA

A 150-MS/s fully dynamic SAR-assisted pipeline ADC employs a dynamic, bias-free, floating ring amplifier. A Miller negative capacitance scheme overcomes the limited gain of the residue amplifier. Miller negative capacitance requires no extra circuitry and only needs a small capacitance. The measured SNDR and SFDR of the 28-nm CMOS prototype ADC with a 1 V supply are 67.9 dB and 84.3 dB, respectively. The ADC consumes 1.72 mW resulting in a Walden and a Schreier SNDR FoM of 5.7 fJ/conversion-step and 173 dB, respectively.

C14-4 - 17:15
A 0.75V 0.016mm² 12ENOB 7nm CMOS Cyclic ADC with 1.5bit Passive Amplification Stage and Dynamic Capacitance Scaling, T. Oshima, K. Yamamoto and G. Ono, Hitachi, Ltd., Japan

A tiny but high-resolution cyclic ADC is presented with 7nm CMOS process. The 1.5bit/stage cyclic ADC performs fully differential sampling and passive residue amplification for small size and power. Proposed dynamic capacitance scaling overcomes limited power efficiency and input bandwidth of traditional cyclic ADCs. A time-assisted comparator makes ternary decision with minimal overhead. Measurement results of the 7nm CMOS prototype proved 4MS/s conversion rate and 74.0dB SNDR with 0.016mm² and 0.86mW under 0.75V supply. This ADC advances the state of the art in design of high-resolution FinFET ADCs and cyclic ADCs.

Circuits Session 15

Images for Emerging Applications [Suzaku II]

Wednesday, June 14, 16:00-17:40

Chairpersons: T. Tokuda, Tokyo Institute of Technology
Q. Fan, Delft Univ. of Technology

C15-1 - 16:00
An Indirect Time-of-Flight CMOS Image Sensor Achieving Sub-Ms Motion Lagging and 60fps Depth Image from On-Chip ISP, P. Jiheon, K. Daeyun, L. Hoyong, S. Seung-Chul and K. Myoungoh, Samsung Electronics Co., Ltd., Korea

This paper presents an indirect time-of-flight image sensor featuring sub-ms motion lagging and depth image output in 60fps using on-chip ISP. Sub-ms motion lagging is achieved as the sensor operates in the global-shutter mode, tap and optical mismatches are suppressed using a dynamic element matching applied demodulation signal to a XY-symmetric 4-tap pixel. This sensor also supports fully-featured on-chip ISP generating real-time depth image to be more easily adopted in AR/VR devices. Fabricated using 2-stack (top: 65nm BSI, bottom: 28nm CMOS) process technology, this sensor dissipates 188mW of power while generating 60fps depth with < 0.87% depth error up to 5 m.

C15-2 - 16:25
A 3.36 μm-Pitch SPAD Photon-Counting Image Sensor Using Clustered Multi-Cycle Clocked Recharging Technique with Intermediate Most-Significant-Bit Readout, T. Takatsuka*, J. Ogi*, Y. Ikeda*, K. Hizu*, Y. Inaoka*, S. Sakama*, I. Watanabe*, T. Ishikawa*, S. Shimada*, J. Suzuki*, H. Maeda**, K. Toshima**, Y. Nonaka*, A. Yamamura*, H. Ozawa*, F. Koga* and Y. Oike*, *Sony Semiconductor Solutions Corp. and **Sony Semiconductor Manufacturing Corp., Japan

This paper presents a photon-counting image sensor with 3.36 μm-pitch pixel front-end circuits and single-photon avalanche diodes (SPADs). A clustered multi-cycle clocked recharging technique with intermediate most-significant-bit readout achieves 120-dB high dynamic range (HDR) at 150-fps imaging with 748 times 448 pixels, while reducing the pixel front-end circuit to a 3.36 mircometre pitch. The power consumption is suppressed to 104 mW, even with 1.2 million incident photons per pixel. A prototype demonstrates HDR global-shutter photon-count imaging with motion artifact suppression and no analog readout noise.

C15-3 - 16:50
A Monolithic Amorphous-Selenium/CMOS Small-Pixel-Effect-Enhanced X-Ray-Energy-Discriminating Quantum-Counting Pixel for Biomedical Imaging, R. Mohammadi*, P. M. Levine* and K. S. Karim*, **, *Univ. of Waterloo and **KA Imaging, Canada

We demonstrate the first dual-energy-discriminating quantum-counting-detector (ED-QCD) pixel with an amorphous X-ray-sensitive semiconductor, amorphous selenium (a-Se), monolithically integrated with a custom CMOS readout IC (ROIC). Our 92x92μm^2 large-area scalable pixel is also the first to exploit the small pixel effect (SPE) in amorphous semiconductors for dual-X-ray-energy quantum counting. SPE enables 7.9keV energy resolution and 35Mcps/mm^2 count rate density that can satisfy even demanding medical-imaging applications like dedicated breast computed tomography (DBCT). Our novel pixel architecture achieves the design objectives by leveraging (1) area-efficient SPE-enhanced sub-pixels with shared counters, and (2) a partially-shared foreground input-offset-correction circuit employing a (3) new area-efficient current-steering calibration DAC.

C15-4 - 17:15
A -20°C~+107°C 52mk-NETD Reference-Cell-Free 15-bits ROIC for 80x60 Microbolometer Thermal Imager, H. Yu, J. C. J. S. Marquez and C.-C. Hsieh, National Tsing Hua Univ., Taiwan

A 52mk NETD reference-cell-free wide-temperature-sensing-range readout IC (ROIC) for micro-bolometer with 15-bits hybrid ADC consisting of the current-mode folding integration (CMFI) and single-slope (SS) operations is realized. The proposed CMFI-SS operation effectively extends conversion range and successfully covers all the circuits PVT variation while provides great temperature sensing range. The prototype achieves a temperature sensing range of -20°C~+107°C while considering the +-15% chip-to-chip and +-3% cell-to-cell pixel variations with an INL/DNL of +-0.12°C/+-0.04°C.

Circuits Session 16

Advanced NNs [Suzaku I]

Wednesday, June 14, 16:00-18:05

Chairpersons: Y. Sasagawa, Socionext Inc.
D. Stark, Meta

C16-1 - 16:00
A 28 nm 66.8 TOPS/W Sparsity-Aware Dynamic-Precision Deep-Learning Processor, H. Mun*, H. Son**, S. Moon*, J. Park*, B. Kim* and J.-Y. Sim*, *POSTECH and **Gyeongsang National Univ., Korea

The required precision for deep neural network (DNN) models strongly depends on sparsity and compactness. This paper presents a heterogeneous DNN accelerator performing a dynamic-precision computing adapted to the sparsity. Simulation shows that the proposed dynamic precision computing successfully covers EfficientNets and Transformers with a negligible accuracy loss. The accelerator, fabricated in a 28nm LP CMOS, achieves a peak energy efficiency of 66.8 TOPS/W with a peak performance of 4.2 TOPS.

C16-2 - 16:25
ANP-G: A 28nm 1.04pJ/SOP Sub-mm² Spiking and Back-Propagation Hybrid Neural Network Asynchronous Olfactory Processor Enabling Few-Shot Class-Incremental On-Chip Learning, D. Huo*, J. Zhang*, X. Dai*, J. Zhang*, C. Qian*, K.-T. Tang** and H. Chen*, *Tsinghua Univ., China and **National Tsing Hua Univ., Taiwan

This paper presents a 28nm 1.04pJ per SOP sub-mm² spiking and back-propagation hybrid neural network asynchronous olfactory processor enabling few-shot class-incremental on-chip learning for the first time, showing <33.27μW training power budget at 0.55V with gas recognition, concentration estimation, and gas incremental learning tasks. This processor achieves 110.62 times and 4.09 times energy saving respectively over the state-of-the-art gas recognition and SNN chips.

C16-3 - 16:50
A Switched-Capacitor Integer Compute Unit with Decoupled Storage and Arithmetic for Cloud AI Inference in 5nm CMOS, A. Agrawal*, M. Kar*, K.-H. Kim*, S. Rylov*, J. Jung*, S. Munetoh**, K. Hosokawa**, X. Zhang*, B. Hekmatshoartabari*, F. Carta*, M. Cochet*, R. Casatuta****, M. Kang*, ***, S. Shukla*, *****, K. Gopalakrishnan*, ***** and L. Chang*, *IBM T. J. Watson Research Center, USA, **IBM Research - Tokyo, Japan, ***Univ. of California, San Diego, ****IBM Systems and technology and *****EnCharge AI, USA

This paper presents a switched-capacitor-based integer compute unit in 5nm CMOS that is designed as a drop-in replacement for an equivalent digital unit to improve power efficiency by 2.5X. Integer multiply-accumulate (MAC) oper-ations are recast as a scaled sum of 1-b MACs, where each 1-b MAC is performed using a population counter (PPCTR) circuit. Each PPCTR is an enhanced SAR ADC that per-forms 1-b multiplication, D-A conversion, accumulation, and A-D conversion with no loss of precision. The compute unit has 4864 PPCTRs arranged as 64 processing engines, with a total throughput of 104.9 TOPS and 650 TOPS/W power efficiency for 1-b MACs.

C16-4 - 17:15
***Pianissimo*: A Sub-mW Class DNN Accelerator with Progressive Bit-by-Bit Datapath Architecture for Adaptive Inference at Edge,** J. Suzuki*, J. Yu*, M. Yasunaga*, A. Lopez Garcia-Arias*, Y. Okoshi*, S. Kumazawa*, K. Ando**, K. Kawamura*, T. Van Chu* and M. Motomura*, *Tokyo Institute of Technology and **Hokkaido Univ., Japan

Pianissimo is a sub-mW class inference accelerator that adaptively responds to the changing edge environmental conditions with a progressive bit-by-bit datapath architecture. SW-HW cooperative control with the custom RISC and the HW counters allows *Pianissimo* adaptive/mixed precision and block skip, providing a better accuracy-computation tradeoff for low-power edge AI. The 40 nm chip, with 1104 KB memory, dissipates 793-1032 μW at 0.7 V on MobileNetV1, achieving 0.49-1.25 TOPS/W at this ultra-low power range.

C16-5 - 17:40
A 28nm 77.35TOPS/W Similar Vectors Traceable Transformer Processor with Principal-Component-Prior Speculating and Dynamic Bit-Wise Stationary Computing, Y. Wang, Y. Qin, D. Deng, X. Yang, Z. Zhao, R. Guo, Z. Yue, L. Liu, S. Wei, Y. Hu and S. Yin, Tsinghua Univ., China

This paper proposes an energy-efficient Transformer processor exploiting dynamic similarity in global attention computing. It has three features: 1) A principal-component-prior speculation unit (PCSU) removes 28.4 percents of of redundant computations. 2) A similar-vector tracked computing engine (STCE) saves 42.2 percents of multiplications. 3) A bit-wise stationary processing element (BSPE) reduces multiplication energy by 1.47 times. The proposed processor achieves a peak energy efficiency of 77.35TOPS per Watt. It reduces energy by 2.81 times and offers 3.71 times speedup compared with the state-of-the-art Transformer processor.

Technology Session 9

PCM, ReRAM and Threshold Switch [Shunju III]

Wednesday, June 14, 16:00-17:40

Chairpersons: T-H. Hou, National Yang Ming Chiao Tung Univ.
H. Tsai, IBM Corp.

T9-1 - 16:00
The Chalcogenide-Based Memory Technology Continues : Beyond 20nm 4-Deck 256Gb Cross-Point Memory, J. Yi, M. Kim, J. Seo, N. Park, S. Lee, J. Kim, G. Do, H. Jang, H. Koo, S. Cho, S. Chae, T. Kim, M.-h. Na and S. Cha, SK hynix Inc., Korea

We demonstrate a high performance and cost effective cross point memory (CPM) technology for storage class memory(SCM) which consists of 20nm 1S1M (one selector one memory) unit cell for four-deck 256 Gb density. Novel process integration was developed to make a uniform Vt distribution for a sufficient read window margin (RWM) and a corresponding low raw bit error rate (RBER). However, in spite of the successful integration and excellent performances, it is expected that the scalability of the CPM will face the inevitable drawbacks such as severe thermal disturbance (TDB) and smaller write program margin which is due to the scaling limit of phase change memory component in CPM. Therefore SOM (selector only memory) is suggested as the alternative device for the next generation SCM.

T9-2 - 16:25
Simple Binary In-Te OTS with Sub-nm HfO_x Buffer Layer for 3D Vertical X-point Memory Applications, S. Ban*, **, J. Lee**, T. Kim* and H. Hwang**, *SK hynix Inc. and **POSTECH, Korea

For the application of a high-density, low-cost 3D vertical X-point array (V-XPA), we report the characteristics of the atomic layer deposition (ALD) available simple In-Te binary ovonic threshold switch (OTS) and its combination with an HfO_x buffer layer. In-Te binary OTS exhibited a highly stable threshold voltage (V_{th}) and low delta firing voltage ($\Delta V_{ff} = V_{ff} - V_{th}$) with a low off-leakage current (I_{off}) of several nanoamperes, which are the essential requirements for a mega-array. To reduce the high I_{off} of the V-XPA, which originates from the perimeter shape selector area, a sub-nanometer ultrathin HfO_x buffer layer was successfully applied for the current confinement, yielding an excellent I_{off} of 1 nA when combined with the In-Te binary OTS.

T9-3 - 16:50
16-Layer 3D Vertical RRAM with Low Read Latency (18ns), High Nonlinearity (>5000) and Ultra-Low Leakage Current (~pA) Self-Selective Cells, Y. Ding*, **, Q. Luo*, K. Xue*** and M. Liu*, *Institute of Microelectronics, Chinese Academy of Sciences, **Univ. of Chinese Academy of Sciences and ***Huazhong Univ. of Science and Technology, China

On-current and nonlinearity of selector-less RRAM are essential for improving the sensing speed and suppressing sneak path leakage respectively in 3D vertical crossbar structure. In this work, by using an oxide in which oxygen vacancies do not readily accumulate (NbO_x) to prepare the memory layer, 50x on-state current density improvement is achieved with high nonlinearity of 5000. The maximum nonlinearity of this device is even higher ($8*10^4$ read @ 1.04 V). Furthermore, for the first time, we present a 16-layer 3D vertical RRAM. Other outstanding performances such as low off-current (~ pA), self-compliance and high endurance (>10^8) are also demonstrated.

T9-4 - 17:15
High Density Embedded 3D Stackable Via RRAM in Advanced MCU Applications, Y.-H. Huang*, Y.-C. Hsieh*, Y.-C. Lin*, Y.-D. Chih**, E. Wang**, J. Chang**, Y.-C. King* and C. J. Lin*, *National Tsing Hua Univ. and **TSMC, Taiwan

An innovative 3D stackable wing-shaped Via RRAM is firstly proposed, featuring logic embedded ultra-high memory density (>0.1Gb/mm^2) and full compatibility with TSMC's 16nm FinFET CMOS platform without extra mask and process steps. In this paper, the new backend Cu-layer stackable 3D RRAM cell structure, array operations, reliability, FinFET macro scalability are characterized and exhibiting the new 3D embedded RRAM is a very promising high density solution of high performance MCU in automotive and IoT applications.

Technology Session 10

Ferroelectric 2: FeRAM, FTJ and FMD [Shunju II]

Wednesday, June 14, 16:00-17:40

Chairpersons: S. Fujii, Kioxia Corp.
T. Mikolajick, NaMLab GmbH

T10-1 - 16:00
First Demonstration of a Design Methodology for Highly Reliable Operation at High Temperature on 128kb 1T1C FeRAM Chip, T. Gong*, **, X. Lihua*, **, W. Wei*, **, J. Pengfei*, **, Y. Peng*, **, N. Bowen*, **, H. Yuanquan*, **, W. Yuan*, **, Y. Yang*, **, G. Jianfeng*, **, L. Junfeng*, **, L. Jun*, **, W. Lingfei*, **, Y. Jianguo*, **, L. Qing*, **, L. Ling*, **, S. C. Steve*** and L. Ming*, **, *State Key Laboratory of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, **Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, China and ***National Yang Ming Chiao Tung Univ., Taiwan

In achieving a reliable operation of FRAM arrays at high temperature (300K~400K), we provide an optimized operation design methodology considering the temperature effect on 128kb 1T1C FRAM chip for the first time. Firstly, we found that the conventional voltage selection scheme in 1T1C FRAM array is not applicable at high temperature since the P_r value read by low voltage decreases at high temperature, leading to a poor yield. Then, the mechanism of P_r degradation under high temperature is systematically investigated through material characterizations and electrical measurements. It was found that the increase of the internal electric field (E_{bias}) caused by electron de-trapping mainly contributes to the P_r degradation. Moreover, a KMC model considering E_{bias} is developed, and the optimum voltage, which can mitigate the temperature effect from 300K~400K, is predicted. This predicted voltage is finally validated on 128kb 1T1C FeRAM chip, and excellent properties are also demonstrated.

T10-2 - 16:25
3D Stackable Vertical Ferroelectric Tunneling Junction (V-FTJ) with On/Off Ratio 1500x, Applicable Cell Current, Self-Rectifying Ratio 1000x, Robust Endurance of 10^9 Cycles, Multilevel and Demonstrated Macro Operation Toward High-Density BEOL NVMs, J.-Y. Lee*, **, F.-S. Chang*, K.-Y. Hsiang*, ***, P.-H. Chen*, Z.-F. Luo*, Z.-X. Li*, J.-H. Tsai*, C.-W. Liu** and M.-H. Lee*, *National Taiwan Normal Univ., **National Taiwan Univ. and ***National Yang Ming Chiao Tung Univ., Taiwan

A 1500x I_{LRS}/I_{HRS} with a high cell current of ~100 nA/cell (J = 83 A/cm^2) is achieved by antiferroelectric (AFE) vertical ferroelectric tunnel junctions (V-FTJs) that demonstrates multilevel, a self-rectifying rate > 1000x, and macro operation. The stackable 3D architecture integrating multiple layers of AFE V-FTJs with contact optimization further increases memory density. Robust endurance > 1e9 cycles at |4V| and stable nonvolatile data retention > 1e4 sec with extrapolation to 10 years are achieved. The proposed cell contact V-FTJ by AFE is a promising pathway toward BEOL NVMs by a NAND/NOR-based framework.

T10-3 - 16:50
Ultra-high Tunneling Electroresistance Ratio ($2×10^4$) & Endurance (10^8) in Oxide Semiconductor-Hafnia Self-rectifying ($1.5×10^3$) Ferroelectric Tunnel Junction, J. Hwang, C. Kim, H. Shin, H. Kim, S.-H. Ko Park and S. Jeon, KAIST, Korea

In this study, we present a remarkable improvement in the performance of hafnia-based ferroelectric tunnel junctions (FTJs) using oxygen scavenging technology and extremely low-damage (ELD) deposition, leading to a significant increase in the tunneling electroresistance ratio (TER) (>$2*10^4$), on-current density (>10^{-2}A/cm^2), and self-rectifying ratio (RR) (>$1.5*10^3$). First-principles DFT simulations were also used to evaluate how the asymmetric oxygen vacancy (V_O) distribution affected FTJs. As an array-level demonstration of the proposed approach, we experimentally built an FTJ-based XNOR synapse array and verified its operation for binary neural networks (BNN).

T10-4 - 17:15
First Demonstration of BEOL-Compatible Write-Enhanced Ferroelectric-Modulated Diode (FMD): New Possibility for Oxide Semiconductor Memory Devices, L. Jiao, K. Han, Z. Zhou, Z. Zheng, X. Wang, Q. Kong, Y. Kang, J. Zhang, L. Liu and X. Gong, National Univ. of Singapore, Singapore

For the first time, we propose and experimentally demonstrate a novel oxide semiconductor (OS) ferroelectric-modulated diode (FMD), addressing a grand challenge in realizing BEOL-compatible OS-based ferroelectric (FE) memories due to the lack of holes. We innovate in introducing a FE layer in the gate-controlled metal/oxide-semiconductor (M/OS) Schottky junction to realize ALD-deposited ZnO oxide semiconductor FE-modulated diode (OS-FMD), enabling more effective switching and reduced write voltage over its competitors, i.e. oxide semiconductor FeFETs (OS-FeFETs), as verified by both experiment and simulation. In addition, such novel structure separates the function of write-terminal (gate) from read-terminal (drain), enhancing the write operation of the FE layer at current-controlled region and eliminating the read disturbance at the drain of the device.

Technology Session 11

New Channel Material 1: InOx and ITO [Shunju I]

Wednesday, June 14, 16:00-17:40

Chairpersons: Y. Shiratori, NTT Corp.
S. Chowdhury, Stanford Univ.

T11-1 - 16:00
Ultrathin Atomic-Layer-Deposited In_2O_3 Radio-Frequency Transistors with Record High f_T of 36 GHz and BEOL Compatibility, D. Zheng, A. Charnas, J.-Y. Lin, J. Anderson, D. Weinstein and P. Ye, Purdue Univ., USA

In this work, we report back-end-of-line (BEOL) compatible In_2O_3 RF transistors with cut-off frequencies (f_T) up to 36 GHz, which is the highest among all metal oxide semiconductor channel RF transistors to date. Due to the outstanding transport properties and high scalability of In_2O_3, record-high f_T value can be achieved with V_{DS} at 0.8 V and V_{GS} at -0.8 V on 2-nm thick, 40 nm-long channel devices. This work demonstrates the first ever BEOL oxide RF transistor with mm-Wave band operation frequency. In addition to improve the performance at Si CMOS clock frequencies for 3D integrated circuits (IC), it also offers the possibility for potential applications in future energy-efficient 6G wireless communication devices.

T11-2 - 16:25
Thickness-Engineered Extremely-Thin Channel High Performance ITO TFTs with Raised S/D Architecture: Record-Low R_{SD}, Highest Moblity (Sub-4 nm T_{CH} Regime), and High V_{TH} Tunability, Y. Kang, K. Han, Y. Chen and X. Gong, National Univ. of Singapore, Singapore

Utilizing the strong thickness-dependent property of ITO film, we report high-performance ITO TFTs having extremely-thin channel (2 to 3.5 nm), a raised S/D structure, and channel length down to 50 nm. The combination of the extremely-thin channel and the RSD helps to achieve record-low S/D series resistance (R_{SD}) and record-high effective mobility (72 cm^2/Vs) at sub-4 nm channel thickness (T_{CH}) regime among all ITO TFTs. We perform systematic investigation on the impacts of T_{CH}, including mobility, subthreshold swing (*SS*), threshold voltage (V_{TH}), quantization effect, and temperature dependence, etc. The results highlight the T_{CH} engineering as a powerful knob to realize enhancement mode operation (V_{TH} > 0) while maintaining high performance and excellent control of short channel effects. The device with T_{CH} as small as 2 nm shows positive V_{TH} of 0.3 V, high peak G_m of 508 at V_{DS} of 1 V, and SS of 85 mV/decade .

T11-3 - 16:50
Ultrahigh Bias Stability of ALD In_2O_3 FETs Enabled by High Temperature O_2 Annealing, Z. Zhang, Z. Lin, C. Niu, M. Si, M. Alam and P. Ye, Purdue Univ., USA

In this work, we systematically studied the temperature dependent electrical performance of atomic-layer-deposited (ALD) indium oxide (In_2O_3) transistors. Both enhancement-mode (E-mode) and depletion-mode (D-mode) In_2O_3 FETs are demonstrated by high temperature O_2 annealing at 400 celsius degree with maximum drain current over 2 mA/μm, on/off ratio up to 10^9, highest mobility beyond 100 cm^2/Vs and lowest subthreshold swing (SS) of 70 mV/dec. High threshold voltage stability is achieved in both negative and positive bias stress conditions with minimum threshold voltage shift of -18 mV under gate bias stress of -2 V for 5000 s. Such ultrahigh bias stability can be attributed to the passivation of oxygen vacancies by O_2 annealing. Temperature dependent I-V characteristics as well as bias instability are also comprehensively investigated. The optimized reliability indicates the back-end-of-line (BEOL) compatible ALD In_2O_3 does offer the great potential as the novel competitive channel in monolithic 3D integration.

T11-4 - 17:15
Co-Designed Capacitive Coupling-Immune Sensing Scheme for Indium-Tin-Oxide (ITO) 2T Gain Cell Operating at Positive Voltage Below 2 V, K. Toprasertpong*, **, S. Liu*, J. Chen*, S. Wahid*, K. Jana*, W.-C. Chen*, S. Li*, E. Pop* and H.-S. P. Wong*, *Stanford Univ., USA and **The Univ. of Tokyo, Japan

We present a capacitive coupling immune 2T gain cell that operates on positive-Von ITO FETs. Co-designing materials, devices, and operating scheme, we demonstrate a gain cell with excellent properties: 1) zero-volt standby WWL with long retention (~8 s extrapolated for 1 fF storage node), 2) operating voltage of 1.9 V with sufficient write current for sub-ns write owing to ITO's notable mobility of 21 cm^2/Vs, 3) write and read scheme using current sensing that *fully* recovers the potential drop from capacitive coupling by WWL, solving a critical challenge known for 2T gain cell implementation.

Banquet [Suzaku I+II, Shunju I+II+III]

Wednesday, June 14, 19:15-21:15

Code-a-Chip Travel Award [Salon de Charme]

Wednesday, June 14, 17:00-19:00

Circuits Session 17

Power Management Circuit [Suzaku II]

Thursday, June 15, 8:30-10:10

Chairpersons: S. W. Hong, Sogang Univ.
S. Bandyopadhyay, Texas Instruments Inc.

C17-1 - 8:30
A Fully Integrated 230 V_{RMS}-to-12 V_{DC} AC-DC Converter Achieving 9 mW/mm², T. Van Daele and F. Tavernier, KU Leuven, Belgium

This work presents a fully integrated 230 V_{RMS}-to-12 V_{DC} AC-DC converter in 180 nm high-voltage CMOS SOI. The proposed AC-DC converter includes a multi-ratio switched-capacitor DC-DC converter (SCC). The reconfiguration is realized by parallelizing stages in the SCC using low-voltage configuration switches. Internally generated DC nodes are connected, resulting in low losses. The input control includes a resettable capacitive divider with >250x less losses than a resistive divider. The measured power density is 9 mW/mm² at 53.1% efficiency, advancing the power density of fully integrated state-of-the-art AC-DC converters by >5000x.

C17-2 - 8:55
5G NR RF PA Supply Modulator Supporting 179ns 0.5-to-5.5V Symbol Power Tracking and Envelope Tracking, J.-S. Bang*, D. Kim*, Y. Choo*, I.-H. Kim*, S. Park*, J. Lee*, S.-H. Lee*, Y.-H. Jung*, J.-Y. Ko*, S. Jung*, J. Han*, W. Kim*, J.-S. Paek** and J. Lee*, *Samsung Electronics Co., Ltd. and **Pusan National Univ., Korea

This paper presents a 5G NR RF PA supply modulator supporting envelope tracking and symbol power tracking. Wide-bandwidth envelope tracking architecture enables fast transition between two symbols with large Tx power difference, achieving 179ns transition time for 0.5 to 5.5V transition.

C17-3 - 9:20
A 93.5%-Efficiency 13.56-MHz-Bandwidth Optimal On/Off Tracking Active Rectifier with Fully Digital Feedback-Based Delay Control for Adaptive Efficiency Compensation, J. Ahn*, **, H.-S. Lee*, K. Eom*, W. Jung* and H.-M. Lee*, *Korea Univ. and **SK hynix Inc., Korea

This paper presents a high-efficiency adaptive active rectifier with fully digital feedback-based delay controllers (DFDC) to rapidly trace optimal on/off timing against input/load variations. Thanks to the real-time power-saving mode control, the proposed rectifier achieved high power conversion efficiency (PCE) of 93.5% and voltage conversion ratio (VCR) of 96.3%. The rectifier adaptively adjusts on/off timing with fast 13.56MHz tracking loop bandwidth.

C17-4 - 9:45
A 0.22mm² per Channel Data Link for Reinforced Isolation with >25kVpk Surge Tolerance and >295kV/µs Common Mode Transient Immunity, D. Ha, R. Yun and K. Wrenner, Analog Devices, Inc., USA

This paper presents an isolated data link for reinforced isolation (>10kV surge tolerance) that occupies merely 0.22mm² per channel, the smallest known to the authors. Based on back-to-back transformers, the link surpasses a surge tolerance of 25kV and provides excellent timing with 6.5ps rms jitter, high CM transient immunity (CMTI) exceeding 295kV/us and low EM susceptibility. The design leverages a coupled resonator architecture to boost the signaling efficiency of tiny transformers and optimized TX controls of a 3.2GHz OOK carrier to maximize timing performance. With its multiple advantages, our compact design advances both the performance and density of isolation systems.

Circuits Session 18

Data Conversion Techniques [Suzaku I]

Thursday, June 15, 8:30-10:10

Chairpersons: T. Iizuka, The Univ. of Tokyo
N. Markulic, imec

C18-1 - 8:30
A 3-320 fJ/Conv.step Continuous Time Level Crossing ADC with Dynamic Self-Biasing Comparators Achieving 61.4 dB-SNDR, M. Timmermans*, M. Fattori*, P. Harpe*, Y.-H. Liu** and E. Cantatore*, *Eindhoven Univ. of Technology and **imec, Netherlands

This paper presents a level crossing ADC (LC-ADC) for biomedical applications. The ADC uses dynamically biased comparators, which require minimal power when the input voltage is far away from a decision threshold. This results in >10x better power efficiency compared to prior LC-ADCs when converting sparse signals. In a 16 kHz bandwidth, the LC-ADC achieves a 61.4 dB SNDR resulting in an efficiency of 3 fJ/conv.step for sparse input signals.

C18-2 - 8:55
A 24-OSR to Simplify Anti-Aliasing Filter 2MHz-BW 83dB-DR 3rd-Order DT-DSM Using FIA-Based Integrator and Noise-Shaping SAR Combined Digital Noise-Coupling Quantizer, M. Fukazawa and T. Matsui, Renesas Electronics Corp., Japan

This paper proposes a dynamic circuits-based discrete-time (DT) delta-sigma modulator (DSM) with 2MHz bandwidth (BW) at an oversampling ratio of 24 to simplify anti-alias filter, flexible operating frequency, and power scalability. The proposed DSM consists of floating inverter amplifier based integrators and an asynchronous SAR quantizer that combines passive noise shaping and digital noise coupling to enhance total noise shaping effect equal to the 3rd-order DSM. This DT-DSM achieves 83.1dB dynamic range while consuming 1.04mW, resulting in 175.9dB DR-based Schreier FoM.

C18-3 - 9:20
A 2.5mW 12MHz-BW 69dB SNDR Passive Bandpass ΔΣ ADC with Highpass Noise-Shaping SAR Quantizers, S. Oh*, S. Park*, Y. Jung*, K. Jimin*, C. Donghee*, S. Ha** and J. Minkyu*, *KAIST, Korea and **New York Univ. Abu Dhabi, United Arab Emirates

A 4th-order passive bandpass ΔΣ modulator (BPDSM) using a 2-path transformation structure is presented. The proposed BPDSM replaces a power-hungry resonator with a z-to-z^2-transformed passive loop filter. The prototype bandpass ΔΣ ADC provides a wide intermediate frequency (IF) range of 1.25MHz to 60MHz. The measured SNDR is 69dB with a power consumption of 2.5mW at 12MHz bandwidth when its highest sampling rate is 240MS/s.

C18-4 - 9:45
A 187dB FoMS 46fJ/Conv. 2nd-order Highpass ΔΣ Capacitance-to-Digital Converter, Y. Jung*, S. Oh*, J. Koo*, S. Park*, J.-H. Suh*, D. Cho**, S. Ha*** and M. Je*, *KAIST, **Samsung Electronics Co., Ltd., Korea and ***New York Univ. Abu Dhabi, United Arab Emirates

The proposed capacitance-to-digital converter (CDC) achieves 187dB FoM_S, which is >2x improvement over the state-of-the-art, with FoM_W of 46fJ/Conv.-Step. We employ a highpass ΔΣ modulator in CDC applications for the first time while using loop filters based on power-efficient floating inverter amplifiers (FIAs).

Technology / Circuits Joint Focus Session 3

AR/VR/MR Metaverse 2 [Shunju III]

Thursday, June 15, 8:30-9:45

Chairpersons: R. Kuroda, Tohoku Univ.
B. Rae, STMicroelectronics N.V.

JFS3-1 - 8:30 (Invited)
216 fps 672 × 512 pixel 3 μm Indirect Time-of-Flight Image Sensor with 1-Frame Depth Acquisition for Motion Artifact Suppression, C. Okada*, S. Yokogawa*, Y. Yorikado*, K. Honda*, N. Okuno*, R. Ikeno*, M. Yamakoshi*, H. Ito*, S. Yoshitsune**, M. Desaki**, S. Hida**, A. Nose*, H. Wakabayashi* and F. Koga*, *Sony, Japan

A 216 fps, 672 × 512 pixel, 3 μm indirect time-of-flight image sensor with 1-frame depth acquisition for motion artifact suppression was developed for versatile applications. To suppress motion artifacts, we employed a floating diffusion sharing circuit, vertical gate technology for the transfer gate, and IQ mosaic pixel coding with demosaic processing. Consequently, a motion artifact-free depth map was obtained, with a 3.5 times faster frame rate, 50% lower power, and 71% lower readout noise compared to a conventional 4-frame sensor.

JFS3-2 - 8:55
A 3.96μm, 124dB Dynamic Range, 6.2mW Stacked Digital Pixel Sensor with Monochrome and Near-Infrared Dual-Channel Global Shutter Capture, S. Chen*, C. Liu*, L. Bainbridge*, Q. Chao*, R. Chilukuri*, W. Gao*, A. P. Hammond*, T.-H. Tsai*, K. Miyauchi**, I. Takayanagi**, M. Nagamatsu**, H. Abe**, K. Mori**, M. Uno**, T. Isozaki**, R. Ikeno**, H.-L. Chen***, C.-H. Lin***, W.-C. Fu*** and S.-G. Wuu***, *Meta, USA, ***Brillnics Japan Inc., Japan and ****Brillnics Inc., Taiwan

Keywords: indirect time of flight, single frame, motion artifact suppression

JFS3-3 - 9:20
Doping-Optimized Back-Illuminated Single-Photon Avalanche Diode in Stacked 40 nm CIS Technology Achieving 60% PDP at 905 nm, E. Park*,**, W.-Y. Ha****, D. Eom*,**, D.-H. Ahn*, H. An***, S. Yi***, K.-D. Kim***, J. Kim***, W.-Y. Choi** and M.-J. Lee*, *Korea Institute of Science and Technology (KIST), **Yonsei Univ., ***SK hynix Inc., Korea and ****École Polytechnique Fédérale de Lausanne (EPFL), Switzerland

We report on back-illuminated single-photon avalanche diodes (SPADs) based on 40 nm CIS technology. The SPAD performance is optimized with doping engineering, enabling the extension of the effective active area resulting in much higher efficiency. It achieves a dark count rate (DCR) of 15 cps/μm², timing jitter of 97 ps, and excellent photon detection probability (PDP) in near-infrared (NIR) wavelength of about 60% at 905 nm and 44% at 940 nm at the excess bias voltage (V_E) of 2.5 V.

Technology Session 12

Ferroelectric 3: Advanced Structures and Processes [Shunju II]

Thursday, June 15, 8:30-10:10

Chairpersons: M. Takenaka, The Univ. of Tokyo
G. Bronner, Rambus, Inc.

T12-1 - 8:30
Grain Size Reduction of Ferroelectric HZO Enabled by a Novel Solid Phase Epitaxy (SPE) Approach: Working Principle, Experimental Demonstration, and Theoretical Understanding, D. Zhang*, J. Wu**, X. Gong* and J. Chen**, *National Univ. of Singapore, Singapore and **Shandong Univ., China

Targeting to address one of the grandest challenges in HfO_2-based ferroelectric (FE) materials and devices, we invent a novel, effective, and versatile technique employing replacement electrode solid phase epitaxy (SPE), achieving a significant reduction in the grain size of the HZO layer by and enhanced remnant polarization (P_r) by 42 simultaneously, as compared with the conventional ALD growth technique. P_r (~25μC/cm^2) among the highest reported at sub-450°C was realized. We also propose the underlying mechanism of the grain size-dependent ferroelectric properties, guided by thermodynamics-included first-principal simulation for nucleation process and kinetics effects-included analysis for phase change. It was discovered that grain size reduction plays a key role in decrease of the m-phase and the enhancement in grain boundary effects, leading to giant P_r improvement.

T12-2 - 8:55
First Demonstration of Work Function-Engineered BEOL-Compatible IGZO Non-Volatile MFMIS AFeFETs and Their Co-Integration with Volatile-AFeFETs, Z. Zheng*, L. Jiao*, Z. Zhou*, Y. Wang*, L. Liu*, K. Han*, C. Sun*, Q. Kong*, D. Zhang*, X. Wang*, K. Ni** and X. Gong*, *National Univ. of Singapore, Singapore and **Rochester Institute of Technology, USA

For the first time, non-volatile antiferroelectric FETs (NV-AFeFETs) with a metal-AFe-metal-insulator-semiconductor (MFMIS) structure are realized employing a replaced floating gate (FG), showing ultra-high endurance over 2E9 cycles. A device with channel length of 41 nm achieves a memory window of 1.8 V. These are made possible through a comprehensive understanding of work function (WF)-engineered NV-AFe capacitors having various metals of Al, Pd, and Pt, including the first study of their temperature-dependent characteristics. The promise of our NV-AFeFETs and WF engineering is further highlighted by co-integrating synapses (NV-AFeFETs) and neurons (volatile-AFeFETs) using the same device architecture to enable hardware-implemented neuromorphic computing.

T12-3 - 9:20
Record Transconductance in L_{eff}~30 nm Self-Aligned Replacement Gate ETSOI nFETs Using Low EOT Negative Capacitance HfO_2-ZrO_2 Superlattice Gate Stack, L.-C. Wang, W. Li, N. Shanker, S. S. Cheema, S.-L. Hsu, S. K. Volkman, U. Sikder, C. Garg, J. Park, Y.-H. Liao, Y.-K. Lin, C. Hu and S. Salahuddin, Univ. of California, Berkeley, USA

We demonstrate short channel, extremely thin SOI (ETSOI, 6<nm), replacement gate nFETs down to effective gate length (L_{eff}) ~30 nm with low equivalent oxide thickness (EOT) negative capacitance (NC) HfO_2-ZrO_2 superlattice (HZH) gate stack. Inversion capacitance measurement shows an EOT of ~7 Å, which is ~2.5 Å lower than typical industry HfO_2 dielectrics. The transistors show record intrinsic transconductance ($g_{m,i}$), 2.11 mS/μm, rivaling what is achieved in much shorter channel length (18 nm) commercial devices such as 22FDX® technology. Importantly, the g_m-L_g scaling trends deviate from industry benchmarks, showing that much larger $g_{m,i}$ is achievable at the same channel length. Despite significantly worse series resistance, the devices show favorable performance in I_{on} *vs* I_{on}/I_{off} tradeoff, providing larger I_{on} and lower I_{off} compared to industrial benchmarks of similar channel length.

T12-4 - 9:45
Towards Epitaxial Ferroelectric HZO on n$^+$-Si/Ge Substrates Achieving Record $2P_r$ = 84 μC/cm^2 and Endurance > 1E11, Z. Zhao, Y.-R. Chen, Y.-W. Chen, W.-H. Hsieh, J.-F. Wang, J.-Y. Lee, Y. Xing, G.-H. Chen and C. W. Liu, National Taiwan Univ., Taiwan

Nearly epitaxially grown ferroelectric HZO films on (001) n$^+$Si(3E19/cm^3) and n$^+$-Ge(3E20/cm^3) substrates exhibit record remanent polarization ($2P_r$) of 84 and 73μC/cm^2, respectively, which are higher than on α-SiO_2 and TiN underlayers. HZO films on n$^+$-Si and n$^+$-Ge also show high $2E_c$ of 8.8 and 5.8MV/cm, respectively. Superlattice HZO films by PEALD show that c-axis is aligned well with the growth direction in STEM images, consistent with observed high $2P_r$ of epitaxial HZO films on n$^+$-Si(Ge). The density functional theory indicates o-phase is greatly stabilized in the HZO films on n$^+$-Si(Ge) substrates due to low interfacial energy at o-phase/Si(Ge) interfaces as compared to m-(t-)phase/Si(Ge). After 1E9 and 1E11 endurance cycles, the HZO on n$^+$-Si and n$^+$-Ge substrates have record finial $2P_r$ of 51 and 47 μC/cm^2, respectively. Our study demonstrates the way to achieve single crystalline ferroelectric HZO films by using small misfit substrates without interfacial layers.

Technology Session 13

Quantum Computing and Cryo-CMOS [Shunju I]

Thursday, June 15, 8:30-10:10

Chairpersons: R. Tsuchiya, Hitachi, Ltd.
R. McMullan, Advanced Micro Devices, Inc. (AMD)

T13-1 - 8:30
Comprehensive 300 mm Process for Silicon Spin Qubits with Modular Integration, A. Elsayed*, **, C. Godfrin*, N. I. Dumoulin Stuyck*, **, M. M. K. Shehata*, **, S. Kubicek*, S. Massar*, Y. Canvel*, J. Jussot*, A. Hikavyy*, R. Loo*, G. Simion*, M. Mongillo*, D. Wan*, B. Govoreanu*, R. Li*, I. P. Radu*, P. Van Dorpe*, ** and K. De Greve*, **, *imec and **KU Leuven, Belgium

We report a comprehensive 300 mm industrial silicon spin qubit integration process for large scale quantum processors. The process was designed to be modular to enable the identification and optimization of the key elements for qubit performance and upscaling. The devices can be fabricated on Si or SiGe substrates with PolySi or TiN metal for the gate electrodes. The modular approach is extended to qubit control structures enabling both ESR antennas and EDSR micromagnets. Various quantum dots and sensors, on both platforms, are measured in a dilution refrigerator at temperatures ~ 10 mK. Electrical characterization of the quantum dots demonstrates low disorder and excellent charge stability down to the last electron. Finally, we demonstrate coherent spin manipulation using an ESR antenna. These low-disorder, high performance qubits mark CMOS manufactured spin qubits as a mature platform for large scale quantum computing.

T13-2 - 8:55
Quantum Dots Array on Ultra-Thin SOI Nanowires with Ferromagnetic Cobalt Barrier Gates for Enhanced Spin Qubit Control, F. Bersano*, M. Aldeghi**, E. Collette*, M. Ghini*, F. De Palma*, F. Oppliger*, P. Scarlino*, F. Braakman***, M. Poggio***, H. Riel**, G. Salis**, R. Allenspach** and A. M. Ionescu*, *Swiss Federal Institute of Technology in Lausanne (EPFL),**IBM Research - Zurich and ***Univ. of Basel, Switzerland

In this work we propose and demonstrate the integration of ferromagnetic nanosized cobalt barrier gates in quantum dots arrays on FD-SOI nanowires. This innovative structure enhances both driving and addressability, while minimizing decoherence fields for electron spin qubits. Charge noise spectra show sub-10^{-6} e^2Hz^{-1} values at 1Hz, demonstrating a low-noise impact from Co gates. Our double dot experimental data show stable quantum confinement at 10mK and full multi-gate FET functionality. Based on calibrated magnetic simulations, we investigate and discuss the advantages of exploiting simultaneously electrical and ferromagnetic properties of gates. The record small achieved dot-magnet distance is below 10nm, with a footprint of the magnetic gates of 30x70nm^2 on dots area, the smallest reported to date on a qubit structure, with a Rabi frequency of 282MHz and qubit addressability of 1.069GHz. This novel architecture paves the way to large-scale integration of qubits arrays with unprecedented magnetic control.

T13-3 - 9:20
How Fault-Tolerant Quantum Computing Benefits from Cryo-CMOS Technology, H.-L. Chiang*, R. A. Hadi**, J.-F. Wang*, H.-C. Han***, J.-J. Wu*, H.-H. Hsieh*, J.-J. Horng*, W.-S. Chou*, B.-S. Lien*, C.-H. Chang*, Y.-H. Wang**, T.-C. Chen*, J.-C. Liu*, L. Y.-C.****, M.-H. Chiang****, K.-H. Kao****, B. Pulicherla*, C.-S. Chang*, J. Cai*, T.-J. Yeh*, Y.-C. Peng*, C. Enz***, M.-C. F. Chang**, M.-F. Chang*, H.-S. P. Wong* and I. P. Radu*, *TSMC, Taiwan, **Univ. of California, Los Angeles, USA, ***École Polytechnique Fédérale de Lausanne, Switzerland and ****National Cheng Kung Univ., Taiwan

Given the limited space and cooling capacity in dilution refrigerators, it is challenging to scale the number of qubits for a fault-tolerant quantum computer (QC). In this paper, we investigate custom CMOS technologies to overcome these constraints. With Cryo-Design/ Technology Co-Optimization (Cryo-DTCO) in advanced nodes, one can then reduce the control power from 24.8 mW/ qubit to 6.4 mW/ qubit (~0.26x). Projections suggest this may be sufficient to enable error corrections via surface codes for fault-tolerant computing.

T13-4 - 9:45
Determining the Low-Frequency Noise Source in Cryogenic Operation of Short-Channel Bulk MosFETs, T. Inaba, H. Oka, H. Asai, H. Fuketa, S. Iizuka, K. Kato, S. Shitakata, K. Fukuda and T. Mori, Advanced Industrial Science and Technology, Japan

For the first time, we clarified the low-frequency noise source of short-channel bulk MOSFETs at cryogenic temperature. We experimentally revealed that, with decreasing temperature, noise sources transition from inner-oxide traps to interface traps and then to band-edge localized states that have energy levels within few tenths of meV from conduction band-edge.This transition occurs because the Fermi level at the interface shifts to near the conduction band, resulting in charge traps responsible for the noise being filled and shallower energy traps contributing to the noise. Determining the noise sources is a critical step in increasing the coherence time of qubits and realizing practical quantum computers with silicon.

Circuits Session 19

Analog Circuit Techniques [Suzaku III]

Thursday, June 15, 10:30-12:35

Chairpersons: T. Nezuka, MIRISE Technologies Corp.
A. Thomsen, Cirrus Logic, Inc.

C19-1 - 10:30
A Reconfigurable Analog FIR Filter Achieving -70dB Rejection with Sharp Transition for Narrowband Receivers, C.-W. Tseng, Z. Feng, Z. Fan, H. An, Y. Wang, H.-S. Kim and D. Blaauw, Univ. of Michigan, USA

We present a compact, highly reconfigurable charge-domain analog-FIR (AFIR) filter for high channel selectivity receivers such as BLE, Zigbee, and IoT applications. This architecture demonstrates excellent power-scaling with reconfigurability to different bandwidth and desired stopband rejection. The charge-domain FIR filter modulates both pulse width and transconductance which multiply to generate the charges of the FIR coefficient. Varying both time and transconductance achieves high programmability enabling a wide range of bit-resolution and FIR tap number combinations to achieve a customizable filter response at optimal power. Fabricated in 28nm CMOS, the filter achieves -70dB stopband rejection with sharp transition and a low power consumption of 0.356mW.

C19-2 - 10:55
An Energy-Efficient Impedance-Boosted Discrete-Time Amplifier Achieving 0.34 Noise Efficiency Factor and 389 MΩ Input Impedance, G. Atzeni, C. Livanelioglu, L. Recchioni, S. Arjmandpour and T. Jang, ETH Zurich, Switzerland

This paper presents a noise-efficient analog front end (AFE) for ultra-low power sensor nodes. The proposed AFE employs a low-noise input stage based on series-parallel converters, and the input impedance is boosted to 389 MΩ (39x improvement compared to prior work) using an input-resistance boosting loop and a capacitive positive feedback loop. The AFE achieves the lowest reported noise efficiency factor (NEF) and power efficiency factor (PEF) of 0.34 and 0.1, respectively, while consuming 370 nW.

C19-3 - 11:20
A 1V 20.7μW Four-Stage Amplifier Capable of Driving a 4-to-12nF Capacitive Load with >1.07MHz GBW with an Improved Active Zero, C.-H. Lee, H.-J. Park, J.-M. Cho, H.-J. Choi, Y.-J. Jeon and S.-W. Hong, Sogang Univ., Korea

This paper proposes a four-stage amplifier with a wider gain bandwidth (GBW) and less sensitivity to gain reduction caused by process scale down. To widen GBW, the proposed amplifier uses a passive zero in the main path and an improved active zero in the feed-forward path. The amplifier achieves DC gain > 120 dB, GBW of 1.25 MHz and 1.07 MHz, and 68.5° and 52°, at C_L of 4 nF and 12 nF, respectively. The chip is implemented in a 0.18-μm CMOS process.

C19-4 - 11:45
A Class-D Piezoelectric Speaker Driver Using A Quadrature Feedback Chopping Scheme Achieving 29dB Large-Signal THD+N Improvement, S. Karmakar*, H. Zhang*, M. Berkhout** and Q. Fan*, *Delft Univ. of Technology and **Goodix Technology, Netherlands

This paper presents a Class-D piezoelectric speaker driver that employs a quadrature feedback chopping scheme (QCS). Compared to a conventional single feedback chopping scheme (SCS), the use of QCS can eliminate the timing skew between low-voltage (LV) and high-voltage (HV) choppers, greatly improving large-signal linearity. A prototype implemented in a 180nm BCD process achieves a peak THD+N of -88dB/ 92.5dB for a 1kHz/ 6kHz input frequency and 37μV_{RMS} output noise (A-weighted) while driving a 4μF load. Thanks to QCS, the large-signal THD+N has been improved by 29 dB, while the output voltage swing achieving -60dB THD+N has been extended from 86.9% to 99.5% of the full-scale (FS).

C19-5 - 12:10
A Compact 0.9uW Direct-Conversion Frequency Analyzer for Speech Recognition with Wide-Range Q-Controlable Bandpass Rectifier, S. Dosho, L. Minati, K. Maari and Hiroyuki Ito, Tokyo Institute of Technology, Japan

We have developed an ultra-low power frequency analyzer for speech recognition that operates at 0.9μW using direct conversion. The use of direct conversion eliminates the frequency selection uncertainty of conventional front ends and provides highly accurate frequency analysis capability, thereby reducing test costs during AI recognition.
Since this circuit can control the bandpass frequency with the frequency of the local oscillator, it is digitally controllable and easy to improve accuracy. Furthermore, Q-value control only requires control of the LPF cutoff frequency independently of the center frequency control.
This frequency analyzer has a new compact configuration that integrates a multiplier, a full-wave rectifier circuit, and a harmonic rejection filter, and each unit consumes only 43 nW of power. The equivalent Q-value of the developed circuit ranges from 3.6 to 36 and is capable of measuring power at 11 frequencies from 500 Hz to 5 KHz.

Circuits Session 20

Circuit Designs for Optical Systems [Suzaku II]

Thursday, June 15, 10:30-12:35

Chairpersons: K. Yoshioka, Keio Univ.
E. Quevy, ProbiusDx Inc.

C20-1 - 10:30
A Mobile OLED Source-Driver IC Featuring Ultra-Compact 3-Stage-Cascaded 10-Bit DAC and 42V/μs-Slew-Rate True-DC-Interpolative Super-OTA Buffer, S. Shin, G.-G. Kang, G.-W. Lim and H.-S. Kim, KAIST, Korea

This paper presents a source-driver IC (SD-IC) for mobile OLED displays. The proposed 3-stage-cascaded 10-bit DAC fully exploits compactness benefit of multi-step interpolation. The overlap-switch merging (OSM) method allows for a 47% size-reduction in the 2-output R-DAC. The SAR-interpolating SC (SI-SC) DAC with bit-adaptive switch size (BASS) modulation is designed to obtain 2-output without switching errors. The proposed super-OTA buffer not only offers a fast slew-rate, but it also performs accurate 1-bit true-DC interpolation. The SD-IC fabricated in 180nm shows the smallest area (132.4x16.7 μm^2/Ch) and the best slew-rate FoM (2470.6) reported to date.

C20-2 - 10:55
A 16-Channel Active-Matrix Mini-LED Driver with an USI-B for EMI Noise Reduction, Y. Kwon, Y. Kwak, Y. Choi, K. Kim, S. Kim, W. Jang, J. Park, K. Ryu, S. Yoo, H. Lim and J. Lee, Samsung Electronics Co., Ltd., Korea

It is presented the first active-matrix (AM) mini light-emitting diode (LED) driver system for a back-light unit (BLU) that uses a newly proposed 1-pair clock-embedding unified standard interface (USI-B) to reduce EMI and power consumption. The system consists of a pixel driver IC (PDIC) and a pixel IC (PIC). The PDIC transmits 20-bit brightness data to the PIC to control the mini-LEDs. The USI-B, based on clock and data recovery (CDR), has been applied to enhance high-level noise tolerance, long-distance transmission, and EMI reduction. Self-current calibration and offset cancellation in the PIC allow for current accuracy of up to ±1% between PICs. This system can support 16,128 LED local-dimming zones (LDZ) using two PDIC and has a measured EMI level of less than 30dB (μV/m). The PDIC and PIC were fabricated using a 65nm and 130nm CMOS process, respectively.

C20-3 - 11:20
Two-Dimensionally Arranged Display Drivers Achieved by OS/Si Structure, Y. Komura*, S. Miyata*, Y. Okamoto*, Y. Tamatsukuri*, H. Inoue*, T. Saito*, M. Kozuma*, H. Kobayashi*, T. Onuki*, Y. Yanagisawa*, T. Takeuchi*, Y. Okazaki*, H. Kunitake*, D. Nakamura*, T. Nagata*, Y. Yamane*, M. Ikeda**, S.-C. Yen***, C.-H. Chang***, W.-H. Hsieh***, H. Yoshida***, M.-C. Chen***, M.-H. Liao****, S.-Z. Chang*** and S. Yamazaki*, *Semiconductor Energy Laboratory Co., Ltd., **Univ. of Tokyo, Japan, ***Powerchip Semiconductor Manufacturing Corp. and ****National Taiwan Univ., Taiwan

We developed silicon (Si) display drivers that can be arranged two-dimensionally by monolithically stacking c-axis-aligned crystalline oxide semiconductor FETs over Si CMOS. The drivers can independently control resolutions and frame rates of corresponding display areas. Our display drivers will achieve a high frame rate, which is difficult to achieve with conventional display drivers.

C20-4 - 11:45
A 2048-Channel, 125μW/ch DAC Controlling a 9,216-Element Optical Phased Array Coherent Solid-State LiDAR, B. R. Moss, C. V. Poulton, M. J. Byrd, P. Russo, O. Shatrovoy, D. Paquette, A. Reardon and M. R. Watts, Analog Photonics, USA

A CMOS driver chip for controlling an optical phased array realizing a >50 meter coherent LiDAR engine has been demonstrated. Five identical 2048-channel driver chips flip onto a single silicon photonics LiDAR engine IC containing the 9,216-element optical phased array. Each voltage-mode driver cell controls an individual electro-optic phase shifter in the array and adjusts the phase shift from 0 to 2π over 8 bits. The driver chip is capable of a system point-to-point steering time <3.8μs. The circuit is optimized for low power and small area, consuming a measured average 125μW per channel including the phase shifter device and amortized chip peripherals, and equivalent area under 79x79μm^2 per driver. This work enabled the realization of a coherent frequency-modulated-continuous-wave (FMCW) chip-scale LiDAR engine with solid-state beamsteering and no external optical components, produced in inexpensive mass-producible 300mm silicon foundries.

C20-5 - 12:10
Super-Cutoff Analog Building Blocks for pW/Stage Operation and Demonstration of 78-pW Battery-Less Light-Harvested Wake-Up Receiver down to Moonlight, J. Basu, L. Fassio, K. Ali and M. Alioto, National Univ. of Singapore, Singapore

Techniques to lower power in analog and sensor interfaces well below regular transistor leakage (V_{GS}=0V) are introduced. The proposed circuit techniques enable ~pW power in super-cutoff (V_{GS}<0V) building blocks from current mirrors to OTAs, pseudoresistors and bias. A LiFi optical wake-up receiver with 78-pW power is demonstrated with continuous operation solely powered by an unregulated 1-mm^2 solar cell down to 1 lux (moonlight).

Circuits Session 21

PIM/CIM Systems [Suzaku I]

Thursday, June 15, 10:30-12:35

Chairpersons: Y. J. Lee, POSTECH
S. Kang, Adeia

C21-1 - 10:30
A General-Purpose Compute-in-Memory Processor Combining CPU and Deep Learning with Elevated CPU Efficiency and Enhanced Data Locality, Y. Ju, Y. Wei, X. Chen and J. Gu, Northwestern Univ., USA

This work presents a general-purpose compute-in-memory (GPCIM) processor combining DNN operations and vector CPU. Utilizing special reconfigurability, dataflow, and instruction set, the 65nm test chip demonstrates a 28.5 TOPS/W DNN macro efficiency and a best-in-class peak CPU efficiency of 802GOPS/W. Due to a data locality flow, 37% to 55% end-to-end latency improvement on AI-related applications is achieved by eliminating inter-core data transfer.

C21-2 - 10:55
A 709.3 TOPS/W Event-Driven Smart Vision SoC with High-Linearity and Reconfigurable MRAM PIM, W. Xie, H. Sang, B. Kwon, D. Im, S. Kim, S. Kim and H.-J. Yoo, KAIST, Korea

This paper presents a high energy-efficiency system-on-chip (SoC) for smart vision applications. A novel reconfigurable and high-linearity MRAM PIM is proposed and achieve high-accuracy event detection (ED) and high-energy-efficiency inference in the event-driven system. The 28nm SoC obtains an average core power consumption of 7.3mW, with an average power reduction of 30.9% at all event densities. The MRAM PIM achieves the peak energy efficiency of 709.3 TOPS/W (1bI-1bW-3bO) at 200MHz and inference accuracy of 91.90%/67.61% (CIFAR-10/100) with ResNet-20.

C21-3 - 11:20
A 5.6-89.9TOPS/W Heterogeneous Computing-in-Memory SoC with High-Utilization Producer-Consumer Architecture and High-Frequency Read-Free CIM Macro, J. Yue*, **, M. Zhan*, Z. Wang**, Y. He*, Y. Li*, S. Yu*, W. Sun*, L. Jie*, C. Dou**, X. Li*, N. Sun*, H. Yang*, M. Liu** and Y. Liu*, *Tsinghua Univ. and **Institute of Microelectronics of the Chinese Academy of Sciences, China

This work presents an energy-efficient CIM SoC with heterogeneous CPU, CIM, SIMD, DMA and COMM cores. The main contributions include: **1)** A producer-consumer instruction dependency controller (PCIDC) with shared multi-port SRAM to reduce CIM SoC-level data transfer. **2)** An inner-pipelined read-free digital CIM macro to achieve higher frequency. **3)** A parallel-to-serial (PTS) sparse architecture utilizing the low activity of partial-sum accumulation. This work demonstrates the first digital-CIM SoC. The fabricated 55nm chip achieves 261TOPS/W (macro) and 33.0TOPS/W (SoC) end-to-end energy efficiency on the test models. The peak SoC energy efficiency is 3.03x higher than the state-of-the-art analog-CIM SoC.

C21-4 - 11:45
GPPU: A 330.4-µJ/Task Neural Path Planning Processor with Hybrid GNN Acceleration for Autonomous 3D Navigation, S. Song, D. Han, S. Kim, S. Kim, G. Park and H.-J. Yoo, KAIST, Korea

A graph neural network (GNN)-based neural path planning processor, GPPU, is proposed for 3D navigation on mobile platforms. It realizes high-speed and energy-efficient path planning by using the hierarchical path planning (HPP) with three key features: 1) graph generation core (GGC) with structured dynamic resolution sampling (SDRS) and K-NN node grouping (KNG) block for GNN preprocessing, 2) reordered grid prefetcher (RGP) and hybrid diagonal-dense-distributed matrix (D^3M) aggregation architecture for fast and efficient GNN acceleration, 3) low-latency core cluster using GNN layer fusion (GLF) for external memory access (EMA) reduction. The GPPU is fabricated in a 28 nm CMOS process and successfully demonstrates on the 3D path planning application with 1.79 ms latency and 330.4 µJ/task energy efficiency at 0.9 V, 200 MHz operation condition.

C21-5 - 12:10
NeRPIM: A 4.2 mJ/Frame Neural Rendering Processing-in-Memory Processor with Space Encoding Block-Wise Mapping for Mobile Devices, W. Jo, S. Kim, J. Lee, D. Han, S. Kim, S. Choi and H.-J. Yoo, KAIST, Korea

NeRPIM, a world-first energy-efficient 3D neural rendering processing-in-memory (PIM) processor, is proposed for mobile devices. A PIM-based renderer reduces the per-sample rendering energy with 8T SRAM PIM. Space encoding block-wise mapping reduces the global memory access and reduces overall rendering energy. A ray-wise dynamic block reuse maximizes the reusability of PIM with enhanced throughput. NeRPIM is fabricated in 28nm CMOS technology and occupies 5.1 mm^2 of die area. As a result, the processor only consumes 129.8 mW of power at 30.7 FPS (NeRF synthetic dataset), achieving a state-of-the-art energy efficiency of 4.2 mJ/frame.

Technology / Circuits Joint Focus Session 4

3D System Integration [Shunju II]

Thursday, June 15, 10:30-12:35

Chairpersons: H. Morioka, Socionext Inc.
A. Loke, NXP Semiconductors N.V.

JFS4-1 - 10:30 (Invited)
AMD Instinct™ MI250X Accelerator Enabled by Elevated Fanout Bridge Advanced Packaging Architecture, R. Swaminathan, M. J. Schulte, B. Wilkerson, G. H. Loh, A. Smith and J. Norman, Advanced Micro Devices, Inc., USA

The recent advancement of leadership class supercomputers was enabled by Frontier, the world's first Exascale supercomputer, leveraging AMD EPYC™ CPU and AMD Instinct™ GPU accelerators. Meeting the compute density and efficiency targets was beyond traditional Moore's Law silicon scaling; accordingly, innovations in the AMD CDNA™ architecture and design as well as packaging and platform architectures were required. AMD utilized an advanced packaging architecture known as Elevated Fanout Bridge (EFB) to fabricate the accelerator engine with integrated High Bandwidth Memory (HBM). EFB has proven to be a cost-effective and reliable packaging technology with the ability to meet the current performance requirements for HBM2e and to scale for future architectures.

JFS4-2 - 10:55 (Invited)
An Integrated System Scaling Solution for Future High Performance Computing, C.-H. Tung and D. C. H. Yu, TSMC, Taiwan

Transistor and system parallel tracks scaling will drive the scaling trends in semiconductor Performance, Power, Area/ Formfactor, and Cost (PPAC). System scaling includes 3D/2.5D wafer level integration and heterogeneity. 3D FabricsTM scaling continues with system vertically scaling up, laterally scaling out, and interconnection pitch scaling in, all significantly contribute to system PPAC optimization. Another, as important, scaling trend is to incorporate in-package non-CMOS devices, thus heterogeneous integration, for PPAC optimization. 3DFabrics classical scaling, and Heterogeneity are the two pillars for future system scaling.

JFS4-3 - 11:20
4-Layer Wafer on Wafer Stacking Demonstration with Face to Face/Face to Back Stacked Flexibility Using Hybrid Bond/ TSV-Middle for Various 3D Integration, C.-L. Lu*, C.-H. Chuang*, C.-H. Huang*, S.-C. Lin*, Y.-H. Chang*, W.-Y. Lai*, M.-H. Chiu*, M.-H. Liao** and S.-Z. Chang*, *Powerchip Semiconductor Manufacturing Corp. and **National Taiwan Univ., Taiwan

Wafer on Wafer (WoW) stacking can provide a tighter pitch and higher interconnect density with higher through-put. In this work, a 4-layer WoW stacking architecture on 12-inch wafers with hybrid bonding/bump-less and through-silicon-via (TSV) middle techniques for enabling various 3D integration has been demonstrated and proposed. It projects >15% form factor and >10% interconnection resistance reduction than typical scheme. Low process temperature (180°C-250°C) is implemented for whole stacking process. For bump-less HBM-like structure, it needs special temporary bond and de-pond process for Face to Back (F2B) bonding. Face to Face (F2F) bonding can present a high dense interconnection for logic to memory AI computing application. The results of 4 layers (TSV x 3 and hybrid bond interface x 3) show that interconnection resistance is <0.25Ω per loop. From the eye-diagram and insertion loss simulation, hybrid bond/bump-less scheme leads to ~40% performance improvement than it in the bump scheme.

JFS4-4 - 11:45
Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy, N. Chujo*, **, K. Sakui*, S. Sugatani*, H. Ryoson*, T. Nakamura* and T. Ohba*, *Tokyo Institute of Technology and **Hitachi, Ltd., Japan

We propose a technology called BBCube 3D for AI and HPC applications, which need high bandwidth and power efficiency. BBCube 3D is constructed by heterogeneous 3D integration in which xPU (CPU, GPU etc.) chiplets and DRAM wafers are stacked using a combination of bumpless Wafer-on-Wafer and Chip-on-Wafer. BBCube 3D has the potential to achieve a bandwidth 30 times higher than DDR5 and four times higher than HBM2E with an bit access energy 1/20th that of DDR5 and 1/5th that of HBM2E.

JFS4-5 - 12:10
1Mbit 1T1C 3D DRAM with Monolithically Stacked One Planar FET and Two Vertical FET Heterogeneous Oxide Semiconductor layers over Si CMOS, Y. Okamoto*, Y. Komura*, T. Mizuguchi*, T. Saito*, M. Ito*, K. Kimura*, T. Onuki*, Y. Ando*, H. Sawai*, T. Murakawa*, H. Kunitake*, T. Matsuzaki*, H. Kimura*, M Fujita*, M Ikeda** and S. Yamazaki*, *Semiconductor Energy Laboratory Co., Ltd. and **Univ. of Tokyo, Japan

We have formed heterogeneous oxide semiconductor FETs (OSFETs) in one planar FET layer and two vertical FET (VFET) layers over Si by monolithically stacking OSFETs on top of Si CMOS. Formation of 1OS1C DRAM memory cells in the VFET layers and a primary sense amplifier (1st SA) in the planar FET layer has realized a memory with different functions such as memory switching and signal amplification in different layers for the first time. As a result, special features, which are three-dimensional monolithic stacking of memory and long date retention, are implemented.

Technology Session 14

New Channel Material 2: InOx and 2D Material [Shunju I]

Thursday, June 15, 10:30-12:35

Chairpersons: B. H. Lee, POSTECH
M. Shulaker, MIT

T14-1 - 10:30
A Nanosheet Oxide Semiconductor FET Using ALD InGaOx Channel and InSnOx Electrode with Normally-Off Operation, High Mobility and Reliability for 3D Integrated Devices, K. Hikake*, Z. Li*, J. Hao*, C. Pandy*, T. Saraya*, T. Hiramoto*, T. Takahashi**, M. Uenuma**, Y. Uraoka** and M. Kobayashi*, *The Univ. of Tokyo and **Nara Institute of Science and Technology, Japan

We have developed ALD InGaOx (IGO) and InSnOx deposition process for channel and electrode, systematically investigated the trade-off among mobility, electrostatics, and reliability in IGO FETs, designed and fabricated multi-gate nanosheet IGO FETs demonstrating normally-off operation, high mobility and reliability, simultaneously, for the first time. This work provides a practical device design guide for developing ALD-based oxide semiconductor FET for 3D integrated devices.

T14-2 - 10:55
Aggressively Scaled Atomic Layer Deposited Amorphous $InZnO_x$ Thin Film Transistor Exhibiting Prominent Short Channel Characteristics (SS= 69 mV/dec.; DIBL = 27.8 mV/V) and High G_m (802 µS/µm at V_{DS} = 2V), Y.-K. Liang*, J.-Y. Zheng*, Y.-L. Lin*, W.-L. Li*, Y.-C. Lu*, D.-R. Hsieh*, L.-C. Peng*, T.-T. Chou**, C.-C. Kei**, C.-C. Lu***, H.-Y. Huang***, Y.-C. Tseng*, T.-S. Chao*, E. Y. Chang* and C.-H. Lin*, *National Yang Ming Chiao Tung Univ., **Taiwan Instrument Research Institute (TIRI) and ***TSMC, Taiwan

In this work, we reported aggressively scaled amorphous $InZnO_x$ thin film transistor (TFT) in channel length (L_{ch} =8 nm) and thickness (2 nm) as a promising candidate for M3D integrations at BEOL. The bottom gate TFT with ultra-short L_{ch} of 8 nm exhibited excellent SS value of 69 mV/dec, high filed-effect mobility of 41 cm^2/V-s and on-current density up to 575 µA/µm (V_{DS}= 1V, V_G= 2V) with outstanding maximum transconductance (G_m) value of 521 µS/µm (V_{DS} = 1 V). In particular, the maximum G_m reaches 802 µS/ µm at V_{DS}= 2V and very low DIBL performance of 27.8 mV/V represent the best G_m and DIBL values reported for ternary amorphous oxide-semiconductor based TFTs. Furthermore, the highly stable device characteristics of the TFT was demonstrated with PBS, the threshold voltage shift of 26.5 mV (L_{ch} = 50 nm) after 3000 s stress with V_G-V_{th} of 3 V was observed.

T14-3 - 11:20
2D Materials in The BEOL, C. H. Naylor, K. Maxey, C. Jezewski, K. P. O'Brien, A. V. Penumatcha, M. S. Kavrik, B. Agrawal, C. V. Littlefield, J. Lux, B. Barley, J. R. Weber, A. Sen Gupta, C. J. Dorow, N. Arefin, S. King, R. Chebiam, J. Plombon, S. B. Clendenning, U. E. Avci, M. Kobrinsky and M. Metz, Intel Corp., USA

2D materials, such as Transition Metal Dichalcogenides (TMDs), have potential for large impact in future technologies due to their inherent atomic thickness. Here, we present multiple applications of 2D materials in the Back End of Line (BEOL). First, we report various 300 mm BEOL compatible growth methods for 2D materials. We reveal the ultra-scaling of interconnect barriers with a 1 nm 2D BEOL barrier yielding comparable performance to 2.5 nm Tantalum (Ta). Furthermore, we present a novel BEOL passivation technique for an unstable film by encapsulating it with a 2D material. Lastly, with a 300 mm BEOL grown WSe_2 film, we report appreciable PMOS currents up to 15 µA/µm for future BEOL CMOS technologies.

T14-4 - 11:45
Integration of Epitaxial Monolayer MX_2 Channels on 300mm Wafers via Collective-Die-To-Wafer (CoD2W) Transfer, S. Ghosh, Q. Smets, S. Banerjee, T. Schram, K. Kennes, R. Verheyen, P. Kumar, M.-E. Boulon, H. M. Silva, S. Kundu, B. Groven, D. Cott, D. Lin, P. Favia, T. Nuytten, I. Asselberghs, C. de la Rosa, S. Brems, A. Phommahaxay and G. S. Kar, imec, Belgium

Inspired by techniques designed for 3D integration, a die-to-wafer (D2W) transfer method can enable MX_2 channel devices in a semiconductor fab for either high-performance CFET or hybrid-integrated CMOS. A Collective D2W (CoD2W) technique was successfully developed to transfer epitaxial single-layer MX_2 from sapphire to 300mm device wafers which facilitates uniform and residue-free *dies*. We report a FEOL semiconductor compatible integration flow used to build back-gated transistors with high device yield and mobility values up to 50 cm^2/Vs on SiO_2 back gate dielectrics.

T14-5 - 12:10
Towards Low Damage and fab-Compatible Top-Contacts in MX_2 Transistors Using a Combined Synchronous Pulse Atomic Layer Etch and Wet-Chemical Etch Approach, S. Kundu, D. H. van Dorp, T. Schram, Q. Smets, S. Banerjee, B. Groven, D. Cott, S. Decoster, P. Bezard, F. Lazzarino, K. Banerjee, S. Ghosh, J.-F. de Marneffe, P. Morin, C. J. L. de la Rosa, I. Asselberghs and G. S. Kar, imec, Belgium

In the quest for process pathfinding for 2D-FET device integration in a 300mm fab, we demonstrate the concept of damascene-compatible top source-drain contacts. Top oxide removal is realized by a combination of self-limited synchronous pulse atomic layer etching of HfO_2-AlOx stack followed by a selective wet-chemical process step allowing soft-landing onto the WS_2 channel. The carrier mobility is preserved in *dry-ALE + wet* processed samples, demonstrating a damage-free process.

Circuits Session 22

Advanced Imagers [Suzaku II]

Thursday, June 15, 14:00-15:40

Chairpersons: T. Takahashi, Sony Semiconductor Solutions Corp.
M. Dielacher, Infineon Technologies AG

C22-1 - 14:00
A 90 µW at 1 fps and 1.33 mW at 30 fps 120 dB Intra-Scene Dynamic Range 640 x 480 Stacked Image Sensor for Autonomous Vision Systems, P.-F. Rüedi, R. Quaglia and H.-R. Graf, CSEM (Swiss Center for Electronics and Microtechnology), Switzerland

We present an ultra-low power high dynamic range image sensor dedicated to autonomous vision systems, realized in a back illuminated 65 nm/40 nm stacked process. Based on a time to digital pixel with in-pixel A/D conversion and data memory, it offers a logarithmic data representation on 10-bit, achieves a sensitivity of 6.4 V/lux/s, an FPN of 0.6 % and a temporal noise of 11 e-, with a pixel pitch of 6.3µm.

C22-2 - 14:25
A 320 x 320 1/5" BSI-CMOS Stacked Event Sensor for Low-Power Vision Applications, G. Schon, D. Bourke, P.-A. Doisneau, T. Finateu, A. Gonzalez, N. Hanajima, T. Hitana, L. Janse Van Vuuren, M. Kadry, C. Laurent, F. Le Goff, D. Matolin, A. Mezaour, B. Michel, T. Naguleswaran, T. Opperman, P. Perrin, E. Reynaud, F. Shahrokhi, H. Tahachouite, C. Tianfan, G. van den Branden, A. Ziram, J.-L. Jaffard and C. Posch, Prophesee, France

Event-based vision is an emerging paradigm of acquisition and processing of visual information. The highly efficient way of acquiring sparse data and the robustness to uncontrolled lighting conditions make event-based vision attractive for applications in industrial, surveillance, IoT, AR/VR, automotive. However, the unconventional format of the event data, non-constant data rates, non-standard interfaces pose challenges to usage and integration. A 320x320 6.3µm pixel BSI stacked event sensor was designed with the explicit goal to improve integrability and usability in embedded at-the-edge vision systems. Emphasis has been put on event data pre-processing and formatting, data interface compatibility and low-latency connectivity to various processing platforms including low-power uCs and neuromorphic processor architectures. Furthermore, the sensor has been optimized for ultra-low power operation, featuring a hierarchy of low-power modes and application-specific modes of operation. On-chip power management and an embedded microcontroller core further improve sensor flexibility and useability at-the-edge.

C22-3 - 14:50
An 0.08e^-·pJ/Step 14-bit Gain-Adaptive Single-Slope Column ADC with Enhanced HDR Function for High-Quality Imagers, L. Hung, K. Matsuura, H. Suto, K. Kodama, Y. Tanaka, T. Ono, J. Fujimagari, K. Akiyama, M. Akahide and Y. Inada, Sony Semiconductor Solutions Corp., Japan

We developed a high-speed, power-efficient single-slope column ADC. The ADC detects and attenuates the bright signals before conversion. A 7.1 Mpixel stacked prototype CMOS image sensor implementing the new ADC attains 14-bit, 224 fps with good characteristics. The ADC also works efficiently with pixel dual-conversion gain readout, achieving a dynamic range of 91 dB.

C22-4 - 15:15
A 60fps 9.9nJ/frame·pixel CMOS Image Sensor with On-Chip Pixel-wise Conversion Gain Modulation for Per-Frame Adaptive DCG-HDR Imaging, Y. Luo*, ** and S. Mirabbasi**, *vivo Mobile Communication Inc., China and **Univ. of British Columbia, Canada

High dynamic range (HDR) features are highly desired in high-end mobile CMOS image sensor (CIS) products. Among plentiful HDR techniques, dual conversion gain (DCG) HDR is preferred due to its high image quality and single-frame basis. For DCG based HDR applications, however, mobile CISs suffer from frame rate reduction and higher power consumption. In this paper, we introduce a CIS design with per-frame pixel-wise conversion gain (CG) modulation. According to the scene to be captured, each pixel is adaptively tuned in its unique CG mode. With only one image readout per frame and without image fusion, a prototype CIS operated in adaptive DCG-HDR mode achieved a dynamic range of 90.5dB and 97.6mW of power consumption at 60fps. Compared to conventional DCG-HDR imaging, the proposed adaptive DCG-HDR imaging reduced CIS power consumption by 38% and enabled single-frame pixel-wise HDR for future mobile CIS products.

Circuits Session 23

Short-Reach Links [Suzaku I]

Thursday, June 15, 14:00-15:40

Chairpersons: C. P. Yue, Hong Kong Univ. of Science and Technology
Z. T. Deniz, IBM T. J. Watson Research Center

C23-1 - 14:00
A Low-Voltage Area-Efficient TSV I/O for HBM with Data Rate Up to 15Gb/s Featuring Overlapped Multiplexing Driver, ISI Compensators and QEC, T. Kim*, J.-Y. Kim*, J. You*, H. Chae*, B. M. Moon**, K. Sohn** and S.-O. Jung*, *Yonsei Univ. and **Samsung Electronics Co., Ltd., Korea

This paper presents a low-voltage area-efficient through-silicon via (TSV) I/O for the high-bandwidth memory utilizing overlapped multiplexing driver, ISI compensators (hybrid equalizer, direct feedback 1-tap DFE) and quadrature error corrector. The proposed TSV I/O is implemented in 65nm CMOS process with emulated 12-stacked TSV. Measurement results show energy efficiency of 0.145pJ/b/pF and 30% timing margin with BER<10^{-12} at 15Gb/s with PRBS-31.

C23-2 - 14:25
A 0.190-pJ/bit 25.2-Gb/s/Wire Inverter-Based AC-Coupled Transceiver for Short-Reach Die-to-Die Interfaces in 5-nm CMOS, Y. Nishi, J. W. Poulton, X. Chen, S. Song, B. Zimmer, W. J. Turner, S. G. Tell, N. Nedovic, J. M. Wilson, W. J. Dally and C. T. Gray, NVIDIA Corp., USA

This paper presents an Inverter-based AC-coupled Toggle (ISR-ACT) transceiver targeted for short-reach die-to-die communication over silicon interposer or similar high-density interconnect. The ISR-ACT's transmitter sends NRZ data through a small on-chip capacitor into the line. The receiver amplifies the low-swing pulses using a 1st-stage TIA to fully toggle the 2nd-stage output, where positive feedback to the input pad maintains the DC level on the line. Fabricated in a 5nm standard CMOS process, ISR-ACT link shows 0.66UI margin at 25.2Gb/s/wire on a 0.75V supply over a 1.2mm on-chip channel and demonstrates the potential to achieve 0.190pJ/bit.

C23-3 - 14:50
A 5.2 Gb/s 3 mm Air-Gap 4.7 pJ/bit Capacitively-Coupled Transceiver for Giant Video Walls Enabled by a Dual-Edge Tracking Clock and Data Recovery Loop, M. B. Younis*, M. G. Ahmed**, T. Wang*, A. Abdelrahman*, M. Khalil*, A. Jose*** and P. K. Hanumolu*, *Univ. of Illinois at Urbana-Champaign, USA, **Ain Shams Univ., Egypt and ***Samsung Semiconductor, Inc., USA

A capacitively coupled transceiver for seamless communication between display tiles in giant video walls is presented in this paper. The transmitter and receiver communicate over a larger than 3 mm air-gap distance. The transceiver uses a slew-rate, impedance-controlled series-source terminated transmitter, a dual-edge tracking clock, and a data recovery receiver that leverages the ISI for error-free operation. Fabricated in a 65nm process, the transceiver operates at a display port rate of 5.2Gb/s and achieves BER < 1e-12, JTOL corner frequency of > 10MHz while consuming 24.6mW.

C23-4 - 15:15
A Sub-500fJ/bit 3D Direct Bond Silicon Photonic Transceiver in 12nm FinFET, P.-H. Chang*, A. Samanta**, P. Yan*, M. Fu**, Y. Zhang**, M. Berkay On**, A. Kumar*, H. Kang*, I.-M. Yi*, D. Annabattuni*, D. Scott***, R. Patti****, Y.-H. Fan*, Y. Zhu*, S. J. B. Yoo** and S. Palermo*, *Texas A&M Univ., **Univ. of California, Davis, ***Optelligent and ****Nhanced Semiconductors, USA

This paper presents an energy-efficient electronic-photonic co-designed transceiver heterogeneously 3D-integrated with high-density, low-parasitic direct bond interconnect (DBI®) featuring 32-channel silicon photonic microdisk modulator-filter based optical transceivers in 12nm FinFET for wavelength division multiplexing (WDM). The transmitter has $1.2V_{ppd}$ electrical modulation swing and 7dB extinction ratio. The receiver achieves an OMA sensitivity of -18.82dBm at 18Gbps. The transceiver pair at 18Gbps achieves 496fJ per bit energy efficiency. The receiver can further operate at 25Gbps with -16.9dBm OMA and 227fJ per bit efficiency.

Technology / Circuits Joint Focus Session 5

Automotive and Aerospace [Suzaku III]

Thursday, June 15, 14:00-15:15

Chairpersons: C. Shiah, Etron Technology, Inc.
T. V. Dinh, NXP Semiconductors N.V.

JFS5-1 - 14:00 (Invited)
How Harsh is Space?—Equations That Connect Space and Ground VLSI, D. Kobayashi and K. Hirose, Institute of Space and Astronautical Science, Japan Aerospace Exploration Agency, Japan

Both space and ground are radiation-rich environments. Ensuring soft-error reliability is essential for both space and ground VLSI. Recent ground VLSI, particularly for automotive applications, has high reliability. It can be naturally considered for applications in space systems. However, estimating the space reliability of the ground VLSI is challenging. Space radiation is often regarded as “harsh” in comparison with ground radiation, but the magnitude of its harshness is unclear. The types of the radiation are different. Converting a ground soft-error reliability to space one is so far difficult. This study provides simple equations that can handle ground and space soft errors uniformly. The equations estimate the harshness of space at approximately 2500-times that of the ground. They also provide implications for the effects of dynamic voltage and frequency scaling on soft-error reliability. Advanced SOI and FinFET SRAMs respond to voltage scaling differently from classical bulk ones.

JFS5-2 - 14:25 (Invited)
Enabling High-Speed, High-Resolution Space-Based Focal Plane Arrays with Analog In-Memory Computing, T. P. Xiao*, W. S. Wahby*, C. H. Bennett*, P. Hays*, V. Agrawal**, M. J. Marinella*** and S. Agarwal*, *Sandia National Laboratories and **Infineon Technologies, USA

JFS5-3 - 14:50
ASIL-D Automotive-Grade Microcontroller in 28nm FD-SOI with Full-OTA Capable 21MB Embedded PCM Memory and Highly Scalable Power Management, N. Grossier*, F. Disegni*, A. Ventre*, A. Barcella*, R. Mariani*, V. Marino*, S. Mazzara*, A. Scavuzzo*, M. Bansal***, S. Balwinder***, A. Anand***, S. Banzal***, D. Joshi***, R. Narwal***, M. Niranjani***, K. Trivedi***, P. Ferreira**, R. Ranica**, L. Vullo*, A. Cathelin**, A. Maurelli*, S. Pezzini* and M. Peri*, *STMicroelectronics N.V., Italy, **STMicroelectronics N.V., France and ***STMicroelectronics N.V., India

This paper proposes the first ever MCU product implementing an ASIL-D automotive grade 0 capable microcontroller with 21MB embedded phase-change memory (PCM) and with highly scalable power management capability.
This new solution from the ST Stellar family of automotive MCUs is developed in proprietary 28nm FD-SOI CMOS technology, with an embedded high density PCM macrocell (memory cell 0.019μm²). The 21MB PCM with high reliability mode can be almost doubled to 40.5MB in enhanced full over-the-air (OTA) mode to host old and new application images at the same time.
A dedicated power architecture allows scaling power consumption by more than four orders of magnitude, from a few amperes (high-performance configuration consumption-forward body biasing (FBB) temperature compensated) down to the 100μA range in the optimized STANDBY mode.

Technology Session 15

In-Memory Computing [Shunju II]

Thursday, June 15, 14:00-15:40

Chairpersons: H. Wu, Tsinghua Univ.
E. Vianello, CEA-LETI

T15-1 - 14:00
Chip Demonstration of a High-Density (43Gb) and High-Search-Bandwidth (300Gb/s) 3D NAND Based In-Memory Search Accelerator for Ternary Content Addressable Memory (TCAM) and Proximity Search of Hamming Distance, C.-C. Hsieh, H.-T. Lue, Y.-C. Li, S.-N. Hung, C.-H. Hung, K.-C. Wang and C.-Y. Lu, Macronix International Co., Ltd., Taiwan

We demonstrated a high density (43Gb) in-memory search (IMS) fully-integrated chip with the ability of Live DEMO for search applications. Based on 96-layer 3D NAND product, using our novel design of paired String-Select Line (SSL) inputs. It can accelerate exact TCAM and proximity Hamming-distance searches. The 128b SSL-inputs and 16KB BL's(output match lines) achieve maximum search bandwidth up to 300Gb/sec with measured chip power less than 400mW. For TCAM mode, large Vt window(>2V) exact search was demonstrated. The read disturb tests surpass 100M read without observable Vt shift. Tests also pass post-1K cycled + baking with qualification requirements. For proximity search, the BL current of paired SSL-input is directly proportional to the normalized Hamming distance so that we can provide an efficient in-memory sorter for similarity search. Our 3D NAND IMS device is suitable for supporting general-purpose data retrieval applications and can significantly save system energy of data movements.

T15-2 - 14:25
3-Bits-Per-Cell 2T32C$_{FE}$ nvTCAM by Angstrom-laminated Ferroelectric Layers with 10^{11} Cycles of Endurance and 4.92V of Ultra-Wide Memory-Windows for In-Memory-Searching, E. R. Hsieh, Y. T. Tang, C. R. Liu, S. M. Wang, Y. L. Hsueh, R. Q. Lin, Y. X. Huang and Y. T. Chen, National Central Univ., Taiwan

A 3D monolithically embedded ferroelectric nvTCAM has been firstly proposed. For proof the concept, the 2T32C$_{FE}$ nvTCAM array has been fabricated, which is fully integrated in the standard CMOS technology. 32 ferro-layers can be deposited between metal layers in the back-end-of-line, which effectively reduces 16x layout overhead. With performance-enhanced angstrom-laminated ferroelectrics, the TCAM shows ultra-wide memory window, 4.94V, and 5x1e4 of on/off ratios, with 8-levels-storage in between. Moreover, searching-power only consumes 9.6 μW/b in 4.5ns. The endurance achieves 1e11 cycles for each storage level, and decade-lifetime can be well-predicted at 87.6°C. This work will prove a competitive solution for future in-memory-searching technologies, aiming for super-chip applications in up-coming 1-trillion-transistors era.

T15-3 - 14:50
Write-Enhanced Single-Ended 11T SRAM Enabling Single Bitcell Reconfigurable Compute-in-Memory Employing Complementary FETs, W.-X. You, C.-Y. Wang, Y. Wang, T.-Y. Chang and S. Liao, TSMC, Taiwan

A write-enhanced single-ended 11T complementary FET (CFET) SRAM capable of performing reconfigurable compute-in-memory (CIM) using a single bitcell is presented for the first time. By leveraging the dummy PFETs within the standard 6T (or 8T) CFET SRAM layout, the write ability of the proposed 11T SRAM can be enhanced more than 2.5 times compared with the 6T (or 8T) SRAM without sacrificing the write half-selected disturb. In addition, the dummy PFETs acting as additional write transistors offers an opportunity to perform Boolean CIM with three reconfigurable schemes introduced in this work. By employing the CFET technology, the 11T CFET SRAM cell shows tiny area overhead compared with the 6T high current SRAM cell (HCC) using non-stacked CMOS and has a comparable footprint as the standard 8T CFET SRAM cell.

T15-4 - 15:15
Monolithic 3D Integration of FeFET, Hybrid CMOS Logic and Analog RRAM Array for Energy-Efficient Reconfigurable Computing-In-Memory Architecture, Y. Du, J. Tang, Y. Li, Y. Xi, B. Gao, H. Qian and H. Wu, Tsinghua Univ., China

In this work, we report a monolithically **3D** integration of $HfZrO_x$ (HZO) ferroelectric FET (FeFET), **a**nalog computing-in-memory (CIM), hybrid back-end-of-line (BEOL) **C**MOS on top of standard Si-CMOS **t**echnology, namely **M3D-FACT**. The 1st layer is Si CMOS circuits for control logic, and the 2nd layer is an analog resistive random-access memory (RRAM) array for CIM. The 3rd layer is a reconfigurable datapath (RCD), consisting of FeFETs with $InGaZnO_x$ (IGZO) channel and hybrid CMOS logic based on carbon nanotube (CNT) PMOS and IGZO NMOS. The structure and functions of each layer were verified. Furthermore, a reconfigurable CIM architecture was implemented using the M3D-FACT chip, and the system-level benchmark against its 2D counterpart shows higher energy efficiency in three different network models (6.9x for VGG-8, 19.2x for DenseNet-121, and 9.9x for ResNet-18).

Technology Session 16

Logic Technology 3: Advanced Platforms and Processes [Shunju I]

Thursday, June 15, 14:00-15:40

Chairpersons: J. Cai, TSMC
A. Veloso, imec

T16-1 - 14:00
Characterizing and Reducing the Layout Dependent Effect and Gate Resistance to Enable Multiple-Vt Scaling for a 3nm CMOS Technology, C.-A. Lu, H. P. Lee, H. C. Chen, Y. C. Lin, Y. H. Chung, S. H. Wang, J. Y. Yeh, V. S. Chang, M. C. Chiang, W. Chang, H. C. Chung, C. F. Cheng, H. H. Hsu, H. H. Liu, W. P. N. Chen and C. Y. Lin, TSMC, Taiwan

In this work, a multiple-Vt solution with a Vt range of ~200 mV and a tight Vt distribution is demonstrated to enable the design flexibility for a 3nm CMOS technology. This is achieved by characterizing and reducing the gate-related layout dependent effects and the gate resistance at scaled cell height and gate length to meet the Vt requirements without compromising the device performance through careful metal gate stack optimization enabled by inserting a passivation layer on thin, low-resistivity work function metal.

T16-2 - 14:25
Novel Low Thermal Budget CMOS RMG: Performance and Reliability Benchmark Against Conventional High Thermal Budget Gate Stack Solutions, J. Franco, H. Arimura, J.-F. de Marneffe, S. Brus, R. Ritzenthaler, E. Dentoni Litta, K. Croes, B. Kaczer and N. Horiguchi, imec, Belgium

Low thermal budget gate stack fabrication is a key enabler for several upcoming CMOS technology innovations, including Sequential-3D integration and CFETs. In this paper we evaluate on a planar CMOS transistor platform various low thermal budget RMG gate stacks based on the novel low temperature atomic hydrogen and oxygen treatments that we have recently demonstrated on MOScap test vehicles, and benchmark them against high temperature RMG and Gate-First counterparts. This first demonstration on both p- and n-channel transistors with properly tuned gate work functions allows us to benchmark electron and hole mobilities, and to assess the nMOS short channel performance (I_{ON}-I_{OFF}), stochastic variability (Vth mismatch) and reliability (BTI and Channel Hot Carrier). We find that the atomic hydrogen treatment boosts also the nMOS performance and reliability due to a remarkably improved interfacial layer quality, matching high-temperature counterparts and thus providing a complete solution for low thermal budget CMOS RMG.

T16-3 - 14:50
Highly Reliable/Manufacturable 4nm FinFET Platform Technology (SF4X) for HPC Application with Dual-CPP/HP-HD Standard Cells, K. Son, S. Park, K. Jung, J.-G. Kim, Y. Ko, K. Cheon, C. Yoon, J. Kim, J. Jeong, T. Myung, C. Hong, W. Jang, M.-C. Sun, S. Jo, J.-Y. Kim, B. Song, Y. Yasuda-Masuoka, J.-H. Ku and G. Jeong, Samsung Electronics Co., Ltd., Korea

In this paper, the most upgraded 4nm (SF4X) ensuring HPC application was successfully demonstrated. Key features are (1) Significant performance +10% boosting with Power -23% reduction via advanced SD stress engineering, Transistor level DTCO (T-DTCO) and MOL scheme, (2) New HPC options: Ultra-Low-Vt device (ULVT), high speed SRAM and high Vdd operation guarantee with a newly developed MOL scheme. SF4X enhancement has been proved by a product to bring CPU Vmin reduction -60mV / IDDQ -10% variation reduction together with improved SRAM process margin. Moreover, to secure high Vdd operation, Contact-Gate breakdown voltage is improved by >1V without Performance degradation. This SF4X technology provides a tremendous performance benefits for various applications in a wide operation range

T16-4 - 15:15
Extremely High-κ $Hf_{0.2}Zr_{0.8}O_2$ Gate Stacks Integrated into $Ge_{0.95}Si_{0.05}$ Nanowire and Nanosheet nFETs Featuring Respective Record ION per Footprint of 9200μA/μm and Record I_{ON} per Stack of 360μA at V_{OV}=V_{DS}=0.5V, Y.-C. Liu, Y.-R. Chen, Y.-W. Chen, H.-C. Lin, W.-H. Hsieh, C.-T. Tu, B.-W. Huang, W.-J. Chen, C.-Y. Cheng, S.-J. Chueh and C. W. Liu, National Taiwan Univ., Taiwan

By taking advantage of the extremely high dielectric constant (κ) of 47, the $Hf_{0.2}Zr_{0.8}O_2$ gate stacks with ultralow EOT/CET of 0.62/0.87nm are integrated into the 8 stacked high mobility $Ge_{0.95}Si_{0.05}$ channels with low thermal budget (450°C) to significantly enhance the I_{ON}. The simulation of κ vs [Zr] in HZO confirms that the κ can be peaked at [Zr]=80%. The 8 stacked $Ge_{0.95}Si_{0.05}$ nanowires and nanosheets achieve the record I_{ON} per footprint of 9200μA/μm and the record I_{ON} per stack of 360μA at V_{OV}=V_{DS}=0.5V, respectively, among all Si/GeSi/Ge 3D nFETs. Moreover, the significant gate delay improvement by combining the extremely high-κ gate stacks and the large floor number is confirmed by simulation.

Circuits Session 24

Sensor Circuits and Systems [Suzaku III]

Thursday, June 15, 16:00-18:05

Chairpersons: M. Takamiya, The Univ. of Tokyo
I. Lee, Univ. of Pittsburgh

C24-1 - 16:00
A Wideband CMOS NMR Spectrometer for Multinuclear Molecular Fingerprinting, A. Zhang, D. Krueger, B. Aghelnejad, G. Yang, H. Hinton, Y.-Q. Song and D. Ham, Harvard Univ., USA

We report a wideband (1-100 MHz) CMOS spectrometer capable of multinuclear nuclear magnetic resonance (NMR) spectroscopy and demonstrate it by performing ^{1}H, ^{19}F, and ^{2}H NMR spectroscopy with high spectral resolution down to 0.07 ppm. This is made possible by developing a wideband digitally-assisted CMOS RF transceiver, where a delay-locked loop (DLL) with a broad locking range is the most critical functional block for enabling the operation across the bandwidth. The portable multinuclear NMR system can enhance the capability of online molecular fingerprinting.

C24-2 - 16:25
A Highly-Digital PWM-Based Impedance Monitoring IC with 143.2dB DR and 17.7fF$_{rms}$ Resolution, H. Han*, W. Choi***, J. Kim*, J. Sung**, H.-J. Choi*, ** and Y. Chae*, *Yonsei Univ., **NFormare, Korea and ***ETH Zurich, Switzerland

This paper presents a highly-digital PWM-based impedance monitoring IC. It achieves a dynamic range of 143.2dB and a resolution of 17.7fF$_{rms}$ for capacitance measurements in a conversion time of 16ms, while consuming only 310.9μW. This corresponds to the state-of-the-art FoM of 199.2dB, a 7.5dB improvement over the prior art. This performance is achieved by a mismatch-free adjustable current stimulator, an improved PWM generator, and 2nd-order DCO-based ADCs.

C24-3 - 16:50
A 36nW CMOS Temperature Sensor with <0.1K Inaccuracy and Uniform Resolution, W. Wang, L. Jiang, S. Dutta, Y. Su, Z. Chen, Z. Yu, C. Kemere and K. Yang, Rice Univ., USA

This paper presents a 36nW high-accuracy subthreshold oscillator-based temperature sensor in 180nm. The proposed super cut-off contention-free (SCCF) delay cell closely mimics the temperature dependency of a single MOS, leading to best-in-class -0.072/+0.082°C (±0.27°C) inaccuracy after 2- (1-) pt calibration. A compact voltage regulator with three native transistors realizes 0.02%/°C line sensitivity and 1mK noise floor. A uniform resolution frequency to digital converter (FDC) keeps the sensing resolution constant across a wide temperature range. In addition to standard testing, the 1-pt calibrated sensor was demonstrated for in-vivo animal body temperature tracking and outperformed off-the-shelf solutions.

C24-4 - 17:15
38.4-pW, 0.14-mm^2 Body-Driven Temperature-to-Digital Converter and Voltage Reference with 0.6-1.6-V Unregulated Supply for Battery-Less Systems, L. Fassio, O. Aiello and M. Alioto, National Univ. of Singapore, Singapore

A temperature-to-digital converter for low-cost purely-harvested systems is introduced. Its architecture is based on an oscillator pair with PTAT and CTAT frequency via body-driven control, and compact temperature sensors with implicit self-regulation. Supply regulation is eliminated for true sub-100 pW power. State-of-the-art power of 38.4 pW is achieved in 180 nm at 0.6 V with 0.49-degree Celsius resolution at 0.14-mm^2 area.

C24-5 - 17:40
A 720 nW Current Sensor with 0-to-15V Input Common-Mode Range and 0.5% Gain Error from -40 to 85 C, R. Zamparette and K. Makinwa, Delft Univ. of Technology, Netherlands

This paper presents a nano-power high-side shunt-based current sensor (CS) that digitizes the voltage drop across an on-chip (1A) or a lead-frame (30A) shunt. A TC-tunable ADC reference compensates for the shunts' large temperature coefficient (TC), resulting in a 0.5% gain error from -40 to 85C. The CS employs a capacitively coupled gm-boosted front-end followed by a CCO-based DSM ADC. Together with a floating input chopper, this results in an input common-mode range (ICMR) of 0-to-15V, the largest reported for a CS implemented in a standard CMOS process. It achieves high energy efficiency (164dB FoM) while consuming only 720nW, representing a 4x improvement on the state-of-the-art and making this the first ever reported sub-uW smart current sensor.

Circuits Session 25

Power and Security Control Systems [Suzaku II]

Thursday, June 15, 16:00-18:05

Chairpersons: K. Kanda, Fujitsu Research
B. Zimmer, NVIDIA Corp.

C25-1 - 16:00
Proactive Power Regulation with Real-time Prediction and Fast Response Guardband for Fine-Grained Dynamic Voltage Droop Mitigation on Digital SoCs, X. Chen*, J. Feng*, A. Shoukry*, X. Zhang**, R. Magod***, N. Desai**** and J. Gu*, *Northwestern Univ., **IBM Corp., ***Texas Instruments Inc. and ****Intel Corp., USA

A proactive power regulation scheme for mitigating dynamic supply droop is proposed with a fully-integrated buck converter, a CPU core and a real-time machine learning (ML) engine. Combined with droop guardband circuit, the proactive scheme demonstrates up to 9.9% higher CPU frequency or 9.2% higher power efficiency compared with prior fast LDO scheme or conventional converters using a 65nm test chip.

C25-2 - 16:25
A 2.6 mV/b Resolution, 1.2 GHz Throughput, All-Digital Voltage Droop Monitor Using Coupled Ring Oscillators in Intel 4 CMOS, C. Augustine, P. Meinerzhagen, W. Lim, A. Veerabathini, M. Bright, K. C. Mojjada, J. W. Tschanz, M. M. Khellah and V. De, Intel Corp., USA

We present an all-digital voltage droop monitor (VDM) with coupled ring-oscillators (CoRO) for accurate in-situ droop monitoring every clock cycle. Measurements from a 3.2mm^2 testchip in Intel 4 CMOS containing 9 3-way CoRO and baseline RO VDMs demonstrate 3X improvement in CoRO resolution (~2.6mV/b) over the baseline. In addition, measurements show 3-sigma uncertainty (repeatability) error of CoRO VDM (+/-9mV) is ~25% lower than the baseline. The overall droop detection error improvements achieved by CoRO VDM are 12mV, 15mV and 17mV, respectively, depending on the type of calibration used - per instance/temperature/die, per temperature/die, or per die. This corresponds to associated IP power savings of 2.9%, 3.2% and 3.7% during functional use.

C25-3 - 16:50
Self-Referenced Design-Agnostic Laser Voltage Probing Attack Detection with 100% Protection Coverage, 58% Area Overhead for Automated Design, H. Zhang*, L. Lin**, Q. Fang*, U. S. H. Kalingage* and M. Alioto*, *National Univ. of Singapore, Singapore and **Southern Univ. of Science and Technology, China

A self-referenced distributed on-chip scheme is introduced to achieve continuous detection of laser voltage probing (LVP) attacks against digital IPs with full-area coverage via temperature sensing. Calibration-free, automated and design-agnostic adoption are enabled by a stdcell-based approach, offering a 2.5X area overhead reduction compared to prior art.

C25-4 - 17:15
Visual Content-Agnostic Novelty Detection Engine with 2.4 pJ/pixel Energy and Two-Order of Magnitude DNN Activity Reduction in 40 nm, A. Gupta, S. Kumar, V. Konandur, S. Taneja and M. Alioto, National Univ. of Singapore, Singapore

An engine to identify frames with novel content in a video stream is proposed as additional vision pipeline stage following conventional saliency detection. Based on connected component analysis with mean-center tracking, its complexity is reduced to linear compared to quadratic in prior art. This introduces frame-level temporal sparsity for subsequent DNN activity/power reduction (177X beyond saliency detection). 2.4 pJ/pixel energy is achieved in 40 nm.

C25-5 - 17:40
Voltage Scaling-Agnostic Counteraction of Side-Channel Neural Net Reverse Engineering via Machine Learning Compensation and Multi-Level Shuffling, Q. Fang*, L. Lin**, H. Zhang*, T. Wang* and M. Alioto*, *National Univ. of Singapore, Singapore and **Southern Univ. of Science and Technology, China

This work proposes a voltage scaling-agnostic counteraction against neural network weight reverse engineering via side-channel attacks. Multi-level shuffling and machine learning-based dual power compensation are introduced. State-of-the-art protection (>200 million MTD) is achieved at low power overhead (1.76x) and zero latency overhead.

Circuits Session 26

Frequency Generation [Suzaku I]

Thursday, June 15, 16:00-18:05

Chairpersons: S. Kondo, Toshiba Corp.
B. Staszewski, Univ. College Dublin

C26-1 - 16:00
A Reference-Sampling PLL with Low-Ripple Double-Sampling PD Achieving −80-dBc Reference Spur and −259-dB FoM with 12-pF Input Load, Y. Zunsong, O. Masaru, L. Shuowei, Z. Yuyang and I. Tetsuya, The Univ. of Tokyo, Japan

A reference-sampling PLL with a low-ripple double-sampling phase detector is proposed to lower the PD's in-band phase noise by 3dB without raising PLL's input load and crystal oscillator's power consumption. A unity-gain-buffer-based charger and a multiplexed dummy sampler are proposed to reduce PLL's input load by a factor of 4 without compromising spur and jitter performances. With a 100-MHz input reference, the prototype in 65-nm CMOS achieves an RMS jitter of 63fs with a spur level of -80dBc. The total power consumption is 3.1mW at 3.4GHz.

C26-2 - 16:25
A 2.4-to-4.2GHz 440.2fs$_{rms}$-Integrated-Jitter 4.3mW Ring-Oscillator-Based PLL Using a Switched-Capacitor-Bias-Based Sampling PD in 4nm FinFET CMOS, J. Jaehong, L. Kyungmin, K. Gunwoo, L. Baekmin, K. Seungjin, O. Seunghyun and L. Jongwoo, Samsung Electronics Co., Ltd., Korea

This work presents a 2.4-to-4.2GHz type-I ring-oscillator (RO)-based PLL with wide bandwidth. The switched-capacitor-bias-based sampling PD ensures the PVT-robustness and high linearity across the wide lock-in range. Due to its merits, the effect of a fast phase-error correction (PEC) scheme is maximized so that the integrated-jitter is 440.2fs$_{rms}$ with 4.3mW. Furthermore, the optimal varactor-tuned RO shields the ripple caused by the sampling PD and PEC, resulting in the reference spur of less than -72.8dBc.

C26-3 - 16:50
A 6nW 30.8kHz Relaxation Oscillator with Sampling Bias-Free RC Circuit and Dynamic Power Scaling in a 12nm FinFET, F.-W. Liao, S.-C. Tsou and C.-S. Chao, MediaTek Inc., Taiwan

An ultra-low power 30.8kHz relaxation oscillator (RxO) is presented. To achieve low power consumption, a sampling bias-free RC circuit is proposed and leveraged in a frequency-lock-loop. Moreover, dynamic power scaling is implemented by adopting local phase allocation and global duty control. In this work, the RxO consumes only 6.05nW under a 0.7V supply. The FoM achieves 0.196nW/kHz, and the active area of RxO occupies 0.063mm^2 in a 12nm FinFET process.

C26-4 - 17:15
A 50μW Ring-Type Complementary Inverse-Class-D Oscillator with 191.4dBc/Hz FoM and 205.6dBc/Hz FoM$_A$, K. Xu*, B. Yu*, J. Hu*, Y. Li*, R. B. Staszewski** and H. Xu*, *Fudan Univ., China and **Univ. College Dublin, Ireland

This paper presents a two-stage 8GHz and a showcased one-stage 6.5GHz VCO in 28nm CMOS. They both feature the complementary inverse class-D operation ensured by the fundamental and second harmonic doubly-tuned 1:1 transformer. By progressively reducing the number of stages from two to one, their peak FoMs improve from 187 to 191.4dBc/Hz (at a 10MHz offset) while breaking the power consumption record to as low as 50uW. Benchmarking with the prior art, our single-stage complementary inverse class-D LC-tank VCO is the first-ever to break the 100uW barrier. It achieves a competitively high FoM (>190dBc/Hz) and the record FoMA with at least 10x lower power dissipation and 5x lower silicon area.

C26-5 - 17:40
A 122fs$_{rms}$-Jitter and –60dBc-Reference-Spur 12.24GHz MDLL with a 102-Multiplication Factor Using a Power-Gating Technique, Y. Cho*, J. Lee*, S. Park*, S. Yoo** and J. Choi*, *KAIST, Korea and **Qualcomm Technologies, Inc., USA

This work presents a low-jitter and high-frequency ring-oscillator (RO)-based multiplying DLL (MDLL). To overcome the limit of conventional MDLLs that use a series MUX for edge switching, the proposed MDLL uses a power-gating (PG) technique to periodically remove the accumulated jitter of the RO. So, it can achieve a very low jitter even at a very high output frequency above 10GHz with a large multiplication factor (*N*) over 100. The proposed hybrid accumulator (HACC) allows the calibrator to achieve high resolution and wide bandwidth concurrently. The measured rms jitter and reference spur at 12.24GHz (*N* = 102) were 122fs and -60dBc, respectively.

Technology Session 17

New Channel Material 3: IGZO [Shunju III]

Thursday, June 15, 16:00-18:05

Chairpersons: A. V-Y Thean, National Univ. of Singapore
Z. Chen, Purdue Univ.

T17-1 - 16:00
Overcoming Negative nFET V_{TH} by Defect-Compensated Low-Thermal Budget ITO-IGZO Hetero-Oxide Channel to Achieve Record Mobility and Enhancement-Mode Operation, S. Devi, C.-K. Chen, M. Lal, S.-H. Tsai, E. Zamburg and A. V.-Y. Thean, National Univ. of Singapore, Singapore

We have successfully demonstrated, oxide-based FETs with a record ID of 790 μA(μm)$^{-1}$ at VDS:1V, an enhancement-mode operation (V_{TH}>0), S.S. <90 mV(dec.)$^{-1}$ and DIBL ~20mV(V)$^{-1}$ at an ultra-scaled channel length of 50 nm. This is enabled by ITO-IGZO hetero-junction channel to achieve channel defect self-compensation. This approach overcomes fundamental issue of negative V_{TH} seen in n-type oxide FETs due to donor-type channel oxygen vacancy and the limited tunability of gate metal work function. Through our ITO-IGZO channel and defect self-compensation approach, our transistor effective mobility is boosted to 110 cm^2(V.s)$^{-1}$ with the channel thickness scaled down to 4 nm. This unique T_{CH}-independent mobility behavior is not observed for IGZO or ITO mono-channel FETs. With such enhancement, our ITO-IGZO FETs exhibit the best-in-class mobility among oxide-based FETs, and are competitive to unstrained Silicon thin film and SOI FETs, while being compatible with sub-400oC back-end-of-line processes.

T17-2 - 16:25
First Demonstration of BEOL-Compatible Atomic-Layer-Deposited InGaZnO TFTs with 1.5 nm Channel Thickness and 60 nm Channel Length Achieving ON/OFF Ratio Exceeding 10^{11}, SS of 68 mV/dec, Normal-Off Operation and High Positive Gate Bias Stability, J. Zhang, Z. Zhang, Z. Lin, K. Xu, H. Dou, B. Yang, X. Zhang, H. Wang and P. D. Ye, Purdue Univ., USA

In this work, we report on the first demonstration of atomic-layer-deposited (ALD) InGaZnO (IGZO) thin film transistors (TFTs) with extreme scaled channel thickness (T_{ch}) of 1.5 nm and channel length (L_{ch}) of 60 nm. These ALD IGZO TFTs exhibit desirable electrical performance including a high on/off ratio exceeding 10^{11}, a steep subthreshold swing (SS) of 68 mV/dec, a small DIBL of 30 mV/V and a normal-off operation. By optimizing the duration of O_2 annealing at 250°C, the threshold voltage (V_T) roll-off issue at scaled L_{ch} is resolved together with a remarkably high degree of stability to the positive gate bias stress (PBS). A trap model with its possible microscopic origin is proposed, providing a new insight into the reliability of IGZO TFTs.

T17-3 - 16:50
First Demonstration of a-IGZO GAA Nanosheet FETs Featuring Achievable SS=61 mV/dec, I_{off}<10^{-7}μA/μm, DIBL=44 mV/V, Positive V_T, and Process Temp. of 300°C, J.-C. Chiu, E. Sarkar, Y.-M. Liu, Y.-C. Chen, Y.-C. Fan and C. W. Liu, National Taiwan Univ., Taiwan

The first amorphous InGaZnO (a-IGZO) gate-all-around (GAA) nanosheet FET is demonstrated. All of the process temperatures are below 300°C, showing great back-end-of-line (BEOL) compatibility. The channel release is achieved by sophisticated reactive-ion etch (RIE) with extremely high etching selectivity of the SiN sacrificial layer over the a-IGZO channel. A novel composite field oxide (FOX) is exploited to form an etching stop layer and avoid gate leakage. The device with gate length (L) of 52nm shows I_{off} <10^{-7}μA/μm (detection limit), high I_{on}/I_{off}>$1.3x10^8$, the enhancement mode with the positive threshold voltage (V_T) of 3.5V, and the clear saturation region in the output characteristic. Moreover, the smallest SS of 61 mV/dec among all oxide semiconductor nanowire /nanosheet devices is achieved with the gate length of 150nm.

T17-4 - 17:15
Demonstration of Crystalline IGZO Transistor with High Thermal Stability for Memory Applications, W. Kim, J. Kim, D. Ko, J.-H. Cha, G. Park, Y. Ahn, J.-Y. Lee, M. Sung, H. Choi, S. W. Ryu, S. Kim, M. Na and S. Cha, SK hynix Inc., Korea

Highly ordered crystalline InGaZnO (c-IGZO) TFTs have been demonstrated in subsequent processes above 550°C Celsius compatible with memory applications. Notably c-IGZO featured strong immunity to high temperature and hydrogen-containing processes unlike amorphous IGZO (a-IGZO) where agglomeration occurs. The c-IGZO TFTs with optimized process in this study show a higher on-current (I_{on}) at a similar V_{th} of -1 V and Ioff of $1.82x10^{-18}$ A per 1 μm compared with a-IGZO TFTs. In addition striking enhancement in the short channel margin and V_{th} stability over a-IGZO was achieved. With thin gate-oxide (5 nm) the improved device performance was realized such as S.S. x0.41 and DIBL x0.18 and I_{on} x76.5 compared with a-IGZO TFT at T_{ox} 10 nm.

T17-5 - 17:40
Lowest I_{OFF} < $3×10^{-21}$ A/μm in Capacitorless DRAM Achieved by Reactive Ion Etch of IGZO-TFT, A. Belmonte, S. Kundu, S. Subhechha, A. Chasin, N. Rassoul, H. Dekkers, H. Puliyalil, F. Seidel, P. Carolan, R. Delhougne and G. S. Kar, imec, Belgium

We demonstrate that the retention of IGZO-based 2T0C devices is boosted by patterning the active module by RIE. While IBE generates Al redeposition on the device sidewalls creating an extrinsic conductive path, RIE enables a clean process which suppresses metal redeposition. With RIE, we achieve the lowest IOFF ever reported for 2T0C cells (< 3E-21 A/μm), and we successfully perform multi-level and multiply-accumulate operations enabling machine-learning applications. We also demonstrate device functionality down to L_G=25nm.

Technology Session 18

DRAM/MRAM [Shunju II]

Thursday, June 15, 16:00-18:05

Chairpersons: K. Hamada, Micron Memory Japan, K.K.
A. Calderoni, Micron Technology, Inc.

T18-1 - 16:00
14nm DRAM Development and Manufacturing, K. Kim, Y. Son, H. Ryu, B. Lee, J. Kim, H. Shin, J. Kang, J. Kim, S. Jeong, K. Chae, D. Lee, I. Jung, Y. Kim, B. Song, J. Oh, S. Park, K. Lee, H. Ban, J. Kim, J. Lee and J. Song, Samsung Electronics Co., Ltd., Korea

As the most scaled memory solution at present, we for the first time developed and begun volume production of 14nm DRAM to extend the continuous shrink trend in semiconductor memory industry. In the new era of 14nm node DRAM and beyond, process integration and device performance are both essential due to the rapid increase of memory cell disturbance and resistance. To resolve the difficulty of process integration, five layer EUV processes and Line type storage node contact scheme were devised, reducing the number of process steps by approximately 20%. To boost device performance, extremely shallow doping engineering played a pioneering role to advance the performance of PMOS transistor by 40% in terms of contact resistance. Our 14nm DRAM will provide the finest and most advanced solution for the next-generation DRAM platform

T18-2 - 16:25
A 135 GBps/Gbit 0.66 pJ/bit Stacked Embedded DRAM with Multilayer Arrays by Fine Pitch Hybrid Bonding and Mini-TSV, S. Wang*, ***, B. Yu*, W. Xiao*, F. Bai*, X. Long*, L. Bai*, X. Jia*, F. Zuo*, J. Tan*, Y. Guo*, P. Sun**, J. Zhou**, Q. Zhan**, S. Hu**, Y. Zhou**, Y. Kang***, Q. Ren* and X. Jiang*, ****, *Xi'an UniIC Semiconductors, **Wuhan Xinxin Semiconductor Manufacturing Co., Ltd., ***Univ. of Science and Technology of China and ****Institute of Microelectronics of the Chinese Academy of Sciences, China

For the first time, multilayer die stack using fine hybrid bonding (HB) with mini-TSV stacking technology is presented and demonstrated for stacked embedded DRAM (SeDRAM). The daisy chains in the multilayer structure with over ten thousand TSVs and bonds were tested and demonstrated the good bonding, stacking quality and reliability. We fabricated LPDD4/4X product by the SeDRAM, with 2048 I/O of 541 Mbps per Gbit, achieving a bandwidth of 135 GBps and power efficiency of 0.66 pJ/bit, exhibiting the improvement of 27.7X for bandwidth and 83% for power efficiency compared to HBM3. Besides, we also put forward the x-test to achieve normal testing and TSV quality judgment.

T18-3 - 16:50
Epitaxial Strain Control of $Hf_xZr_{1-x}O_2$ with Sub-nm IGZO Seed Layer Achieving EOT=0.44 nm for DRAM Cell Capacitor, S. Kim*, Y. K. Park*, G. S. Lee*, E. J. Shin*, W. S. Ko**, H. D. Lee**, G. W. Lee** and B. J. Cho*, *KAIST and **Chungnam National Univ., Korea

We propose for the first time a method to crystallize 4.5 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO) in the ferroelectric orthorhombic phase (o-phase) by using a sub-nm InGaZnO (IGZO) seed layer. Atomic mismatch between IGZO and HZO layers introduces epitaxial strain, inducing ferroelectric phase crystallization even at thickness of 4.5 nm. HZO/IGZO achieved an EOT of 0.44 nm, coercive voltage of 0.51 V, and high endurance $>10^{14}$. Hence, HZO/IGZO is a promising candidate for next generation high-k dielectric in DRAM capacitor applications.

T18-4 - 17:15
Highly Reliable and Manufacturable MRAM Embedded in 14nm FinFET Node, S. Ko, J. H. Park, J. H. Bak, H. Jung, J. Shim, D. S. Kim, W. Lim, D.-E. Jeong, J. H. Lee, K. Lee, J.-H. Park, Y. Kim, C. Kim, J. H. Jeong, C. Y. Lee, S. H. Han, Y. Ji, S. H. Hwang, H. J. Shin, K. Lee, Y. J. Song, Y. G. Shin and J. H. Song, Samsung Electronics Co., Ltd., Korea

We demonstrated highly reliable and manufacturable 16Mb magnetic random access memory (eMRAM) embedded in 14nm FinFET logic by achieving high yield over 90% at an operating temperature ranging from -40°C to 125°C and passing the PKG reliability tests, such as HTOL and endurance 10^6 cycles. In addition, for automotive application and further scaling down, we confirmed the function of eMRAM macro at the elevated temperature of 160°C, and achieved the low short fail of 1ppm level for sub 10nm eMRAM pitch using the novel patterning technology, respectively.

T18-5 - 17:40
U-MRAM: Transistor-Less, High-Speed (10 ns), Low-Voltage (0.6 V), Field-Free Unipolar MRAM for High-Density Data Memory, M.-H. Wu*, **, M.-C. Hong*, **, C. Shih*, **, Y.-J. Chang**, Y.-C. Hsin**, S.-C. Chiu**, K.-M. Chen**, Y.-H. Su**, C.-Y. Wang**, S.-Y. Yang**, G.-L. Chen**, H.-H. Lee**, S. Z. Rahaman**, I.-J. Wang**, C.-Y. Shih**, T.-C. Chang**, J.-H. Wei**, S.-S. Sheu**, W.-C. Lo**, S.-C. Chang** and T.-H. Hou*, *National Yang Ming Chiao Tung Univ. and **Industrial Technology Research Institute of Taiwan, Taiwan

U-MRAM, an enabler of a diode-selected cross-point MRAM array, is demonstrated using a mature device structure identical to STT-MRAM. U-MRAM exploits the probabilistic switching of thermal fluctuations using a single write voltage. The asymmetric synthetic antiferromagnetic layer (SAF) enables promising U-MRAM properties, including low voltage (0.6 V), high speed (10 ns), excellent endurance ($>10^{10}$), and long retention (>10 years) without an external magnetic field. Diode-selected U-MRAM is a strong candidate for future high-density embedded memory.

Technology Focus Session 2

BEOL/BSPDN [Shunju I]

Thursday, June 15, 16:00-18:05

Chairpersons: M. Kanda, Toshiba Electronic Devices & Storage Corp.
M. Delaus, Analog Devices, Inc.

TFS2-1 - 16:00 (Invited)
Novel Cell Architectures with Back-side Transistor Contacts for Scaling and Performance, M. Kobrinsky*, J. D Silva*, E. Mannebach*, S. Mills*, M. Abd El Qader**, O. Adebayo**, N. Arkali Radhakrishna****, M. Beasley**, J. Chawla***, S. Chugh***, A. Dasgupta**, U. Desai**, E. De Re**, G. Dewey*, T. Edwards**, C. Engel*, V. Gudmundsson**, J. Hicks***, B. Krist*, R. Mehandru**, I. Meric***, P. Morrow*, D. Nandi**, P. Patel**, R. Ramamurthy***, D. Samanta**, L. Shoer**, A. St Amour**, L. H. Tan**, S. Yemenicioglu, X. Wang**** and T. Ghani**, Interl Corp.

PowerVia increases the efficiency of power delivery by adding back-side interconnects [1]. It also improves performance by relaxing the minimum front-side interconnect pitch and by optimizing them for signaling. Research to further improve performance and density synergistically with PowerVia includes back-side device contacts and device stacking. In this paper, we present an experimental demonstration of a novel cell architecture with back-side device contacts and back side power delivery.

TFS2-2 - 16:25
Nano-Through Silicon Vias (nTSV) for Backside Power Delivery Networks (BSPDN), B. Eric, A. Jourdain, G. Beyer and G. van der Plas, imec, Belgium

In this paper we discuss the driving forces for moving to chip backside power delivery. Possible integration flows and challenges are discussed for integrating through-silicon via (TSV) connections that directly interconnect the chip at the standard-cell level. These approaches use power rail integration schemes that can be “buried” in the STI and Si below the devices or directly integrated as backside metallization scheme on the wafer backside. Both nTSV “last” and “first” integration flows have been demonstrated. Key technology challenges are the extreme wafer thinning required and back-side lithography correction to compensate for wafer distortions caused by wafer processing and W2W bonding.

TFS2-3 - 16:50
BEOL Interconnect Innovation: Materials, Process and Systems Co-optimization for 3nm Node and Beyond, G. Thareja, A. Pal, X. Wang, S. Dag, S. You, S. Sharma, Q. Zhu, C. L. Cervantes, S. Hwang, M. Spuller, B. Ng, P. S. Kumar, N. Tam, M. Gage, S. Deshpande, Z. Wu, A. Jansen, L. Dey, F. Chen, X. Xie, K. Kashefizadeh, V. Reddy, A. Lo, Z. Chen, S. Huey, J. Tang, H. Ren, M. Naik, B. Brown, S. Kesapragada, B. A. Sangamali, E. M. Bazizi and X. Tang, Applied Materials, Inc., USA

We present novel back-end-of-line (BEOL) copper interconnect integration for advanced technology nodes using integrated selective barrier copper barrier seed (CuBS) process, annealing and chemical mechanical planarization (CMP). Electrical tests (resistance, reliability) combined with Materials-to-Systems Co-Optimization (MSCO™) simulations confirm significant power-performance-area (PPA) gains for 3nm technology node and beyond.

TFS2-4 - 17:15
Block-level Evaluation and Optimization of Backside PDN for High-Performance Computing at the A14 Node, G. Sisto*, R. Preston**, R. Chen*, G. Mirabelli*, A. Farokhnejad*, Y. Zhou*, I. Ciofi*, A. Jourdain*, A. Veloso*, M. Stucchi*, O. Zografos*, P. Weckx*, G. Hellings* and J. Ryckaert*, *imec, Belgium and **ARM Ltd., USA

This paper evaluates the impact of backside power delivery on the physical implementation of a commercial 64-bit high-performance block from ARM™ at the A14 node. A backside BEOL, including nTSV connections, is proposed and calibrated using TCAD and experimental data. The developed stack is modeled in a commercial cell-level parasitic extraction tool to enable its use during place and route. The same benchmark is physically implemented using imec's own A14 PDK. The backside PDN enables frequency improvements from 2% to 6% compared to the frontside PDN, stemming from a core area reduction from 8% to 23%. These results are obtained without negatively impacting the total power and simultaneously limiting dynamic IR drop below 35mV. Furthermore, different TSV options have been studied to potentially boost the IR drop gains up to 23%

TFS2-5 - 17:40
Structural Reliability and Performance Analysis of Backside PDN, S. Kim, G.-M. Kim, S.-N. Kim, S. Ahn, Y.-S. Kim, I. Jang, K.-W. Lee and D. S. Kim, Samsung Electronics Co., Ltd., Korea

One of the innovative packaging solutions for beyond-4nm node, Backside-Power Delivery Network (BS-PDN) is investigated to analyze the chip package interaction (CPI) effects. BS-PDN configuration contains dense mircothrough silicon vias (μTSV) and power/ground metal stack on the backside of the silicon die. By employing submodeling simulation, stress concentration of this both-side backend-of-the-line (BEOL) structure is analyzed with the node displacement of packaging-level macro model as the boundary condition. Compared to the conventional front-side BEOL structure of current 4nm node, stress concentration is observed in the last Dx metal next to μTSV in BS-PDN structure for expecting risks of delamination. In addition, we analyze the oscillation frequency of an inverter ring oscillator (INV RO) built using BS-PDN. Effects on the dimension of μTSVs, materials applied in μTSVs, and the barrier metal thickness of μTSVs to suggest the optimal scenario with respect to the CPI risks and RO performance of BS-PDN.

Forum

Compute Paradigms for Secured Microelectronics and Combinatorial Optimization [Suzaku I+II+III]

Friday , June 16, 8:50-15:30

Chairpersons: S. Yu, Georgia Institute of Technology
M. Takamiya, The Univ. of Tokyo
S. Fujii, Kioxia Corp.

8:50 Opening by Forum Chair

8:55 Cyber-Physical Security from Chip to Cloud, Y.-T. Clochard, Secure-IC

9:25 In-Memory-Computing Based Accelerators for Privacy-Preserving Computing,
X. S. Hu, CISE CCF, National Science Foundation

9:55 Cryptographic Circuit Technology Consisting of Photonic Logic Gates,
J. Takahashi, NTT Social Informatics Laboratories

10:25 Hardware Security, Cryptography, Side-Channel Attacks, Fault Attacks, Embedded Security,
S. Bhasin, Nanyang Technological University, Singapore

10:55 Panel Discussion for Secured Microelectronics

11:40 Lunch

12:40 Quantum-Inspired Annealing Processor, C. H. Kim, Univ. of Minnesota

13:10 Simulated Bifurcation Machines: Combinatorial Optimization Accelerators Based on a Quantum-Inspired Parallelizable Algorithm, K. Tatsumura, Toshiba Corp.

13:40 Flexible Optimization Solver Using Mixed Analog-Digital In-Memory Computing, J. P. Strachan, RWTH Aachen

14:10 Engineering for Large-Scale Superconducting Quantum Annealers, S. Kawabata, AIST

14:40 Panel Discussion for Combinatorial Optimization

15:25 Closing by Forum Chair