2.1 – 10:25 a.m.
A Low Power 6-bit Flash ADC with Reference Voltage and Common-Mode Calibration, C.-Y. Chen, M. Le, K.Y. Kim, Broadcom Corporation, USA

A low power 6-bit ADC that uses reference voltage and common-mode calibration to improve linearity and reduce power dissipation is presented. The ADC occupies 0.13mm² in 65nm CMOS. The ADC dissipates 4mW at 100MS/s and 12mW at 800MS/s from a 1.2V supply.

2.2 – 10:50 a.m.
A 7.6 mW 1.75 GS/s 5 Bit Flash A/D Converter In 90nm Digital CMOS, B. Verbruggen, P. Wambacq, M. Kuijk*, G. Van der Plas, IMEC, *Vrije Universiteit, Belgium

A 5 bit 1.75 GS/s flash ADC is realized in 90 nm CMOS. It uses a comparator array with built-in imbalance and offset calibration to lower power consumption. The SNDR is 30.9 dB at low frequencies and gradually degrades to 28.2 dB at 2 GHz. The ADC occupies 280µm by 110µm and draws only 7.6 mA from a 1 V supply yielding an energy efficiency of 0.15 pJ/conversion step.

2.3 – 11:15 a.m.
A 6-bit 5-GSample/s Nyquist A/D Converter in 65nm CMOS, M. Choi, J. Lee, J. Lee, H. Son, Samsung Advanced Institute of Technology, Korea

A 6-bit Nyquist A/D converter (ADC) that converts at 5 GHz is reported. Using a wideband track-and-hold amplifier, array averaging, reset switches on analog signal paths, and phase-adjusted clocking for cascaded comparators, a 6-bit flash ADC achieves better than 5 effective bits for input frequencies up to 2.5 GHz at 5 GSample/s. This ADC does not rely on time interleaving, digital calibration, and post data processing for its dynamic performance. This ADC consumes about 320mW from 1.3 V at 5 GSample/s. The chip occupies 0.3mm² active area, fabricated in 65nm CMOS.

2.4 – 11:40 a.m.

A 10.3GS/s ADC with 5GHz input BW and 6 bit resolution in 90nm CMOS is presented. The architecture is based on an 8 way interleaved/pipelined ADC using open-loop amplifiers and digital calibration. The measured performance is 5.8 ENOB (36.6dB SNDR) for a 100MHz input signal and 5.1 ENOB (32.4dB SNDR) for a 5GHz input (Nyquist) with phase offset correction across the interleaved array.