
A 1-kb memory-cell array composed of single-electron shut-off (SESO) cells was fabricated with the 90-nm logic process for the first time. It features a 0.1-FIT/Mb soft error, 100-MHz random cycle, and 100-ms retention. In addition to a logic-compatible cell structure and a write-data caching scheme, a backup latch circuit with SESO transistors for logic application was also proposed.


An asymmetric memory interface cell with 32 bidirectional data and four unidirectional request links operating at 16Gb/s per link is implemented in TSMC 65nm CMOS technology. Timing adjustment and equalization circuits for both memory read and write are on the controller to reduce memory cost. Each link operates at a maximum rate of 16Gb/s with comparable margins in both directions at a BER of 10-12. The measured energy efficiency for the cell is 13mW/Gb/s.


This paper describes a 16-Gb/s differential bidirectional I/O transceiver cell in an emulated 40nm DRAM process. The transceiver implements several techniques to achieve low jitter despite the slow process and constrained power consumption. The transceiver has measured random jitter of 380fs rms at the transmitter output and BER < 10-14 while consuming 8mW/Gb/s.