2014 VLSI SYMPOSIA HIGHLIGHTS

The 2014 VLSI Symposia technical program consists of overlapping sessions from June 9 – 12 (Technology) and June 10 – 13 (Circuits), with more than 200 presentations, short courses and panel discussions by the leading researchers and scientists. Program is designed to highlight recent advances in microelectronics technology and circuits, and promote networking amongst participants.

SYMPOSIUM ON VLSI TECHNOLOGY

PLENARY PRESENTATIONS
Tuesday morning, June 10

- Device & Technology Implications of the Internet of Things
  – Robert Atkin, ARM
- Customer Value Creation in the Information Explosion Era
  – Keichiro Shimada, Sony Corporation

RUMP SESSION (panel discussion)
Tuesday evening, June 10

450mm, EUV, III-V, SD – All in 7nm? Are You Serious?!
  – Moderator: Andrzej Strojwas, PDF Solutions

TECHNOLOGY FOCUS SESSIONS
Embedded NV Memory Technologies
Session T5 (Tuesday, June 10, 3:25pm)

Interconnect: Local & Global
Session T16 (Wednesday, June 11, 8:05am)

SYMPOSIUM ON VLSI CIRCUITS

PLENARY PRESENTATIONS
Wednesday morning, June 11

- Data Center 2020: Near-memory Acceleration for Data-Oriented Applications – Ed Dolter, Micron Technology
- Technology Development for Printed LSIs Based on Organic Semiconductors – Jun Takeya, University of Tokyo

RUMP SESSIONS (panel discussion)
Thursday evening, June 12

What Should Circuit Designers do in an Era of System Level Design? – Moderator: Jan Rabaey, UC Berkeley

TECHNOLOGY & CIRCUITS LinkedIn Group

PROFESSIONAL DEVELOPMENT OPPORTUNITIES (TECHNOLOGY)

SHORT COURSE
High Performance Mobile SoCs Enabled by 10nm SoC Technology
Monday, June 9

- Key Semiconductor Products, Applications & Device Drivers
- System On Chip – Applications & Key Aspects
- FEOL Scaling & Integration, 3rd Gen FinFET Devices & Architectures
- BEOL, Interconnect, Scaling, Processes & Integration
- Technology/Design Co-Optimization (FET/circuits, Standard Cell, eMemory, DDR)
- Embedded SoC Memory: eSRAM, eNVM & eDRAM
- Variability & DFM
- 2.5D or 3D Packaging for Mobile SIP

PROFESSIONAL DEVELOPMENT OPPORTUNITIES (CIRCUITS)

SHORT COURSES

- Advanced Data Converter & Mixed-Signal Circuit Design – June 10
  A/D Converter Trends: Power Efficiency & Digitally Assisted Architectures
  System Design for Direct Sampling RF Front Ends
  Advances in SAR ADCs with the Scaling of CMOS
  Ultra-wideband Time-interleaved SAR ADCs for Wireline/Optical Communications
- Digital Error Correction of Time-interleaved A/D Converters
- Digitally Assisted Wireless Transceivers & Synthesizers
- Emerging Semiconductor Industry Trends & Implications
  – Moderator: Dan Hutcheson, CEO of VLSI Research, Inc.
- Advanced Energy-Efficient System Architectures
- Energy-Efficient System Architectures
- Low Power CPUs for SoC Integration
- Fine-Grained Power Management Using Integrated DC-DC Converters
- Challenges & Techniques for Ultra-Low Voltage Logic with Nearly-Minimal Energy
- Advanced Energy Efficient SRAM Design

SATELLITE WORKSHOPS

IEEE Silicon Nanoelectronics Workshop
  – June 8 & 9
- Spintronics Workshop
  – June 9

For complete conference and registration information, visit: http://www.vlsisymposium.org/