Welcome to the 2010 Symposium on VLSI Technology!

On behalf of the organizing Committees, it is our pleasure to invite you to attend the 2010 Symposium on VLSI Technology which will be held from June 15-17, 2010 in Honolulu, Hawaii.

Since its founding in 1982, this symposium has been one of the most prestigious international forums for the latest research and development in VLSI technology. The program committee has worked very hard this year to select 92 excellent contributed and invited papers and organized them into 22 sessions. We are delighted to have two distinguished Invited Speakers for the Plenary Session.

Michael Rosenfield of IBM TJ Watson Research Center will present a talk titled: “The Smart Grid and Key Research Technical Challenges” and Tsunenobu Kimoto of Kyoto University will speak on “SiC Technologies for Future Energy Electronics”.

Two focus topics with invited papers will cover a selection of key developments in Design Enablement and Heterogeneous Integration. Design Enablement will focus on how new or disruptive device, process and materials technologies will impact circuit design (including design rule restrictions, device models, OPC, DFM,...etc), product performance, and product migratability. Heterogeneous Integration will focus on integrating non-Si substrates/materials on large Si wafers (CNT, graphene, Ge, SiGe, III-V,...etc), including their process integration, device architectures, performance and impact on CMOS roadmaps.

The conference will also have three Rump Sessions on the evening of June 15 as a means to facilitate informal discussions among researchers. One is a joint session with the Symposium on VLSI Circuits which will ask the question: “The Next Decade of VLSI Technology and Circuits – Are We on the Same Road?”. The other two sessions will cover specific technology related topics of current interest, “What Will End Moore’s Law?” and “The Future of Embedded Memory”.

In addition, there will be a one-day Short Course on Monday June 14 and will cover “Emerging Logic and Memory Technologies for VLSI Implementation”.

Six distinguished researchers will discuss the following key subjects – advanced high performance and low power technologies, design enablement for these new technology options, 3D IC’s, beyond-CMOS devices and advanced memory technologies. The Short Course promises to be an excellent opportunity for experienced as well as new engineers to broaden their technical base.

One of the unique strengths of the Symposium on VLSI Technology has been its close association with the Symposium on VLSI Circuits. For 2010 we will continue with the two days of overlap with a single registration fee permitting attendees to attend both technology and circuit sessions from June 15th through Jun 18th.

The symposium registration fee covers all of the sessions including the Rump Sessions, coffee breaks, Monday night Reception and the Wednesday night joint banquet for both Circuits and Technology attendees. Registration for the Short Course is extra. The registration fees and hotel reservation schedules are detailed at the end of the Advance Program.

As in past years, we expect a strong participation of top VLSI researchers from both the industry and the academic sectors. We look forward to seeing you at this year’s exciting Symposium in Honolulu.

Ming-Ren Lin
Hitoshi Wakabayashi
Program Chair
Program Co-Chair
SESSION 1 – TAPA I
Plenary Session

Tuesday, June 15, 8:05 a.m.
Chairpersons: M.R. Lin, GLOBALFOUNDRIES
H. Wakabayashi, Sony Corporation

8:05 a.m. Welcome and Opening Remarks
C. Dennison, Ovonyx Technologies, Inc.
M. Niwa, Panasonic Corp.

1.1 – 8:35 a.m.
The Smart Grid and Key Research Technical Challenges, Michael Rosenfield, IBM TJ Watson Research Center

1.2 – 9:20 a.m.
SiC Technologies for Future Energy Electronics, Tsunenobu Kimoto, Kyoto University

SESSION 2 – TAPA I
Advanced CMOS I

Tuesday, June 15, 10:20 a.m.
Chairpersons: O. Faynot, CEA-LETI
M. Masahara, AIST

2.1 - 10:20 a.m.

2.2 - 10:45 a.m.

2.3 - 11:05 a.m.
Gate-all-around Silicon Nanowire 25-Stage CMOS Ring Oscillators with Diameter Down to 3 nm, S. Bangsaranitp, A. Majumdar, G. Cohen, S. Engelmann, Y. Zhang, M. Guillom, L. Gignac, S. Mittal, W. Graham, E. Joseph, D. Klaus, J. Chang, E. Cartier, J. Sleight, IBM T.J. Watson Research Center, USA

SESSION 3 – TAPA II
Reliability and Stability

Tuesday, June 15, 10:20 a.m.
Chairpersons: J. Cheek, Freescale
S. Chung, National Chiao Tung University

3.1 - 10:20 a.m.

3.2 - 10:45 a.m.

3.3 - 11:05 a.m.

3.4 - 11:35 a.m.
SESSION 4 – TAPA I
Advanced CMOS II

Tuesday, June 15, 1:30 p.m.
Chairpersons: M. Khare, IBM
H. Kurata, Fujitsu Microelectronics Ltd.

4.1 - 1:30 p.m.
20nm Gate Length Trigate pFETs on Strained SGOI for High Performance CMOS,

4.2 - 1:55 p.m.
SiGe CMOS on (110) Channel Orientation with Mobility Boosters: Surface Orientation, Channel Directions, and Uniaxial Strain,

4.3 - 2:20 p.m.
High-Mobility Si_{1-x}Ge_{x}-Channel PFETs: Layout Dependence and Enhanced Scalability, Demonstrating 90% Performance Boost at Narrow Widths,

4.4 - 2:45 p.m.
FDSOI CMOS with Dielectrically-Isolated Back Gates and 30nm L Gate High-k/Metal Gate,

SESSION 5 – TAPA II
MRAM and X-Point RRAM

Tuesday, June 15, 1:30 p.m.
Chairpersons: K. Parekh, Micron
B.H. Lee, Gwangju Institute of Science and Technology

5.1 - 1:30 p.m.
A Multi-Level-Cell Spin-Transfer Torque Memory with Series-Stacked Magnetotunnel Junctions,
T. Ishigaki, T. Kawahara, R. Takemura, K. Ono, K. Ito, H. Matsuoka, Hideo Ohno*, Hitachi, Ltd., *Tohoku University, Japan

5.2 - 1:55 p.m.
Highly Scalable STT-MRAM with MTJs of Top-pinned Structure in 1T/1MTJ Cell,

5.3 - 2:20 p.m.
Non-volatile Spin-Transfer Torque RAM (STT-RAM): Data, Analysis and Design Requirements for Thermal Stability,

5.4 - 2:45 p.m.
Novel Cross-point Resistive Switching Memory with Self-formed Schottky Barrier,

SESSION 6 – TAPA I
Ultra Thin Body FDSOI

Tuesday, June 15, 3:25 p.m.
Chairpersons: W. Xiong, Texas Instruments
T. Iwamatsu, Renesas Electronics Corp.

6.1 - 3:25 p.m.
Low Leakage and Low Variability Ultra-Thin Body and Buried Oxide (UT2B) SOI Technology for 20nm Low Power CMOS and Beyond,

6.2 - 3:50 p.m.
Hybrid Localized SOI/Bulk Technology for Low Power System-on-Chip,

6.3 - 4:15 p.m.
Ultra-Thin-Body and BOX (UTBB) Fully Depleted (FD) Device Integration for 22nm Node and Beyond,
6.4 - 4:40 p.m.
Scalability Study of Ultra-Thin-Body SOI-MOSFETs Using Full-band and Quantum Mechanical Based Device Simulation, H. Takeda, K. Takeuchi, Y. Hayashi, NEC Electronics Corporation, Japan

6.5 - 5:05 p.m.

SESSION 7 – TAPA II
Process Technology

Tuesday, June 15, 3:25 p.m.
Chairpersons: C.-P. Chang, Applied Materials, Inc.
S. Hayashi, Panasonic Corp.

7.1 - 3:25 p.m.

7.2 - 3:50 p.m.
Minimization of Threshold Voltage Variation to AVt=1.3mVµm in Bulk High-k/Metal Gated Devices by Dopant-Diffusion Control Using Integrated FSP-FLA Technology, S. Kato, T. Aoyama, T. Onizawa, K. Ikeda, Y. Ohji, Semiconductor Leading Edge Technologies, Inc, Japan

7.3 - 4:15 p.m.

7.4 - 4:40 p.m.

7.5 - 5:05 p.m.
Evidence of Correlation Between Surface Roughness and Interface States Generation in Unstrained and Strained-Si MOSFETs, Y. Zhao, M. Takenaka, S. Takagi, The University of Tokyo, Japan

The International Technology Roadmap for Semiconductors (ITRS) charts future technology requirements and potential pathways for the industry to sustain the historical pace of improvement in transistor performance and cost. These include the use of higher-permittivity gate dielectric materials, high-mobility semiconductor channel materials, and non-classical structures to improve transistor drive current and scalability, and they vary depending on the application (high performance vs. low operating power vs. low standby power). The issues of increasing MOSFET off-state leakage current and performance variations with transistor scaling are fundamental challenges which will require joint Technology-Circuits solutions, in order for the industry to sustain the historical pace of improvement in circuit performance and cost.

This panel discussion will aim to answer the following questions:

- What do we expect to see in the next 10 years in terms of new devices and technologies? (Technologists will provide an ITRS-based perspective for future transistor improvement.)
- Will these address the needs of the expected applications? (Circuit designers will describe driver applications and associated device requirements in terms of performance, power, cost, and design complexity.)

Panelists:
M. Brillouet, CEA LETI
M. Izzard, Texas Instruments
T. Hiramoto, The Univ. of Tokyo
K. Imai, NECEL
D. Robertson, Analog Devices
K. Ishibashi, Renesas Electronics Corp.

R1 What Will End Moore’s Law?
Honolulu I

Moderators: H. Ishiuchi, Toshiba Corp.
M. Jurczak, IMEC

Moore’s Law of exponentially increasing transistor count per chip over time has prevailed despite the challenges of increasing power density and variability for deep-sub-micron CMOS technologies. Some argue that in fact Moore’s Law ended at the 90 nm node, beyond which the pace of circuit performance gains slowed. Others hold that the essence of Moore’s Law, that is decreasing cost per transistor, has been maintained. As new materials and non-classical transistor
structures are adopted, even this may be in jeopardy, however. This panel discussion will discuss various reasons why Moore’s Law will end, and describe approaches to delay or circumvent them. These include the following:

• Lithography: It may be too costly to print features at sub-16nm half-pitch.
• Device physics: Quantum-mechanical tunneling and voltage-scaling limits can result in unacceptably high power densities and therefore limit device pitch scaling.
• Economics: The semiconductor market will not grow at a pace sufficient to provide the economies of scale needed to sustain Moore’s Law.

Finally, this panel will consider possible replacements for Moore’s Law to set the cadence for the semiconductor industry after 2020.

Panelists:
W. Arnold, ASML
S. Biesemans, IMEC
R. Chau, Intel
S. Kramer, SEMATECH
H. Shinohara, STARC
T. Watanabe, Toshiba

R2 The Future of Embedded Memory
Honolulu II
Moderators: L. Chang, IBM T. J. Watson Research Center
T. Endoh, Tohoku University

Embedded memory is a key component in determining the speed, power, reliability, and yield of integrated circuits. For decades, six-transistor (6T-) SRAM scaled in accordance with Moore’s Law and served well as the primary embedded memory option. However, continued scaling of 6T-SRAM brings about fundamental challenges such as transistor mismatch due to Vth fluctuation, which, particularly in conjunction with voltage scaling, can result in severe degradation of read and write operating margins. While the industry has worked in earnest to cope with SRAM scaling issues, alternative approaches have also been widely investigated.

In recent years, embedded DRAM has gained acceptance, even for high performance applications, and emerging technologies such as embedded Flash, MRAM, SP-RAM, FeRAM, PCM, ReRAM, FBC-RAM, and T-RAM have all made significant strides. This panel discussion will look towards future embedded memory technology in the 22/16 nm era and beyond to answer the following questions:

- In this time frame, what do we need memory to do (e.g. density, performance, power, non-volatility) in embedded applications? What might we be able to trade off to achieve these goals?
- Will SRAM ever be displaced as the embedded memory of choice?
- Which emerging technologies are practically suited for anticipated embedded memory needs? What challenges are involved in developing these technologies?

8.1 - 8:30 a.m.
Novel Ultra-Low Power RRAM with Good Endurance and Retention, C.H. Cheng, A. Chin, F.S. Yeh, National Tsing Hua University, National Chiao-Tung University

8.2 - 8:55 a.m.
A New Approach for Improving Operating Margin of Unipolar ReRAM using Local Minimum of Reset Voltage, Y. Sakotsubo, M. Terai, S. Kotsujii, Y. Saito, M. Tada, Y. Yabe, H. Hada, NEC Corporation, Japan

8.3 - 9:20 a.m.

8.4 - 9:45 a.m.
A Novel TiTe Buffered Cu-GeSbTe/SiO$_2$ Electrochemical Resistive Memory (ReRAM), Y.-Y. Lin, F.-M. Lee, Y.-C. Chen, W.-C. Chien, C.- W. Yeh, K.-Y. Hsieh, C.-Y. Lu, Macronix International Co., Ltd, Taiwan
9.3 - 11:15 a.m.
Statistical Evaluation for Trap Energy Level of RTS Characteristics, A. Teramoto, T. Fujisawa, K. Abe, S. Sugawa, T. Ohmi, Tohoku University, Japan

9.4 - 11:40 a.m.

SESSION 10 – TAPA III
3D Integration

Wednesday, June 16, 10:25 a.m.
Chairpersons: B. van Schravendijk, Novellus Systems, Inc.
T. Tanaka, Tohoku University

10.1 - 10:25 a.m.

10.2 - 10:50 a.m.
Assembly-Stress-Mechanism in Pad Areas on High-k/Metal Gate Transistors, Y. Oto, F. Itoh, K. Ishikawa, K. Hagihara, T. Matsumoto, T. Iwase, Y. Itoh, H. Hirano, Panasonic Corporation, Japan

10.3 - 11:15 a.m.

10.4 - 11:40 a.m.

SESSION 11 – TAPA II
Beyond CMOS

Wednesday, June 16, 1:30 p.m.
Chairpersons: A. Seabaugh, Notre Dame University
T. Hiramoto, The University of Tokyo

11.1 - 1:30 p.m.

11.2 - 1:55 p.m.
Realistic Spin-FET Performance Assessment for Reconfigurable Logic Circuits, Y. Gao, C. Augustine, D. Nikonov*, K. Roy, M. Lundstrom, Purdue University, *Intel, USA

11.3 - 2:20 p.m.

11.4 - 2:45 p.m.

SESSION 12 – TAPA III
NAND Flash Memory

Wednesday, June 16, 1:30 p.m.
Chairpersons: J. Lutze, Sandisk Corp.
J.T. Moon, Samsung Electronics Co., Ltd.

12.1 - 1:30 p.m.

12.2 - 1:55 p.m.
SESSION 13 – TAPA II
Design Enablement I

Wednesday, June 16, 3:25 p.m.
Chairpersons: K. Schruefer, Infineon Technologies AG
                    C. Wann, TSMC

13.1 - 3:25 p.m.
A Dual Core Oxide 8T SRAM Cell with Low Vccmin and Dual Voltage Supplies in 45nm Triple Gate Oxide and Multi Vt CMOS for Very High Performance yet Low Leakage Mobile SoC Applications,

13.2 - 3:50 p.m.
A 32nm Low Power RF CMOS SOC Technology Featuring High-k/Metal Gate,

13.3 – 4:15 p.m.
Enabling Application-Specific Integrated Circuits on Limited Pattern Constructs (Invited),
  D. Morris, V. Rovner, L. Pileggi, A. Strojwas, K. Vaidyanathan, Carnegie Mellon University, USA

13.4 – 4:40 p.m.
Novel Circuit Design and Process Technology for Leading-Edge Products (Invited),

13.5 – 5:05 p.m.
Design-Technology Interaction for Post-32 nm Node CMOS Technologies (Invited),
  G. Shahidi, IBM Thomas J. Watson Research Center, USA

SESSION 14 – TAPA III
Heterogeneous Integration

Wednesday, June 16, 3:25 p.m.
Chairpersons: R. Chau, Intel Corp.
                    K. Shibahara, Hiroshima University

14.1 – 3:25 p.m.
III-V/Ge CMOS Technologies on Si Platform (Invited),
  S. Takagi and M. Takenaka, The University of Tokyo, Japan

14.2 – 3:50 p.m.
III-V: Replacing Si or More than Moore? (Invited),
  Y. Sun, IBM Thomas J. Watson Research Center, USA

14.3 – 4:15 p.m.
GaN-on-Si: A Scalable Material System to Realize Cost Effective Next-Generation Solid State Lighting and Power Devices (Invited),
  S. Decoutere, H. Osman, J. Dekoster, B. Dutta, S. Biesemans, IMEC, Belgium

14.4 – 4:40 p.m.
How Can High Mobility Channel Materials Boost or Degrade Performance in Advanced CMOS (Invited),
  T. Skotnicki and F. Boeuf, STMicroelectronics, France

14.5 – 5:05 p.m.
Classification and Benchmarking of III-V MOSFETs for CMOS (Invited),
  M. Passlack, G. Doornbos, C. Wann, Y.C. Sun, TSMC, Belgium, Taiwan

SESSION 15 – TAPA II
DRAM

Thursday, June 17, 8:30 a.m.
Chairpersons: C. Mazure, SOITEC
                    R. Yamada, Hitachi, Ltd.

15.1 - 8:30 a.m.
Integration of Back-Gate Doping for 15-nm Node Floating Body Cell (FBC) Memory,
  I. Ban, U. Avci, D. Kencke, P. Tolchinsky, P. Chang, Intel Corp, USA

15.2 - 8:55 a.m.

15.3 - 9:20 a.m.
Vertical Double Gate Z-RAM Technology with Remarkable Low Voltage Operation for DRAM Application,
SESSION 16 – TAPA III

Novel Devices

Thursday, June 17, 8:30 a.m.
Chairpersons: C.P. Chang, Applied Materials, Inc.
Y. Mochizuki, NEC Corporation

16.1 - 8:30 a.m.
Short-Channel Performance and Mobility Analysis of <110>- and <100>-Oriented Tri-Gate Nanowire MOSFETs with Raised Source/Drain Extensions, M. Saitoh, Y. Nakabayashi, H. Itokawa, M. Murano, I. Mizushima, K. Uchida*, T. Numata, Toshiba Corporation,
*Tokyo Institute of Technology, Japan

16.2 - 8:55 a.m.
Bistable Resistor (Biristor) – Gateless Silicon Nanowire Memory, J.-W. Han, Y.-K. Choi, KAIST, Korea

16.3 - 9:20 a.m.

16.4 - 9:45 a.m.
Mobility Enhancement over Universal Mobility in (100) Silicon Nanowire Gate-All-Around MOSFETs with Width and Height of Less Than 10nm Range, J. Chen, T. Saraya, T. Hiramoto, University of Tokyo, Japan

SESSION 17 – TAPA II

Advanced CMOS III

Thursday, June 17, 10:25 a.m.
Chairpersons: T. Skotnicki, STMicroelectronics
Y. Akasaka, Tokyo Electron Ltd.

17.1 - 10:25 a.m.
*Osaka University, **University of Tsukuba, **Waseda University, Japan

17.2 - 10:50 a.m.

17.3 - 11:15 a.m.
Dipole Controlled Metal Gate with Hybrid Low Resistivity Cladding for Gate-Last CMOS with Low Vt, C. Hinkke, R. Galatage, R. Chapman, E. Vogel, H. Alshareef*, C. Freeman**, E. Wimmer**, H. Niimi^, A. Li-Fatou^, J. Shaw^, J. Chambers, University of Texas at Dallas, USA, King Abdullah University of Science and Technology, Saudi Arabia, **Materials Design Inc., USA, ^Texas Instruments, USA

17.4 - 11:40 a.m.

SESSION 18 – TAPA III

Characterization and Modeling

Thursday, June 17, 10:25 a.m.
Chairpersons: E. Kan, Cornell University
E. Morifuji, Toshiba Corp.

18.1 - 10:25 a.m.

18.2 - 10:50 a.m.

18.3 - 11:15 a.m.

18.4 - 11:40 a.m.
SESSION 19 – TAPA II
PCRAM

Thursday, June 17, 1:30 p.m.
Chairpersons:  K. Parekh, Micron
               H. Miyake, Elpida Memory, Inc.

19.1 - 1:30 p.m.

19.2 - 1:55 p.m.
MLC PRAM with SLC Write-Speed and Robust Read Scheme, Y. Hwang, C. Um, J. Lee, C. Wei, H.-R. Oh, G. Jeong, H. Jeong, C. Kim, C. Chung, Samsung Electronics Co., LTD, Korea

19.3 - 2:20 p.m.

19.4 - 2:45 p.m.

SESSION 20 – TAPA III
GeMOSFETs

Thursday, June 17, 1:30 p.m.
Chairpersons:  R. Jammy, SEMATECH
               K. Shibahara, Hiroshima University

20.1 - 1:30 p.m.
Electron Mobility in High-k Ge-MISFET Goes to Higher, T. Nishimura, C.H. Lee, S. Wang, T. Tabata, K. Kita, K. Nagashio, A. Toriumi, The University of Tokyo, Japan

20.2 - 1:55 p.m.
High-k/Ge p- & n-MISFETs with Strontium Germanide Interlayer for EOT Scalable CMIS Application, Y. Kamata, K. Ikeda, Y. Kamimuta, T. Tezuka, Toshiba, Japan

SESSION 21 – TAPA II
Design Enablement II

Thursday, June 17, 3:25 p.m.
Chairpersons:  M. Khare, IBM Corp.
               C. Wann, TSMC

21.1 - 3:25 p.m.

21.2 - 3:50 p.m.

21.3 – 4:15 p.m.
Multi-Design of Architecture, Circuit/Device/Process and Package for Cost-effective Smart Mobile Devices: An Integrated Fabless Manufacturer (IFM)’s Perspective (Invited), G.C-F Yeap, Qualcomm, Inc., USA

21.4 – 4:40 p.m.
Design Challenges and Enablement for 28nm and 20nm Technology Nodes (Invited), C.Y-C Hou, Taiwan Semiconductor Manufacturing Company, Taiwan

21.5 – 5:05 p.m.
High Performance Design with Advanced Features in 22nm and Beyond (Invited), S. Borkar, Intel Corporation, USA
SESSION 22 – TAPA III
Exploratory Research

Thursday, June 17, 3:25 p.m.
Chairpersons: A. Seabaugh, Notre Dame University
S. Takagi, The University of Tokyo

22.1 - 3:25 p.m.
Study of Channel Length Scaling in Large-Scale Graphene FETs,
S.-J. Han, Y. Sun, A. Bol, W. Haensch, Z. Chen, IBM T.J. Watson
Research Center, USA

22.2 - 3:50 p.m.
III-V MOSFETs with New Self-Aligned Contact,
Y.-C. Yeo, National University of Singapore, *TSMC, **National Nano Device Laboratory, *National Chiao-Tung University, Taiwan

We report the first demonstration of III-V n-MOSFETs with self-aligned contact technology. The self-aligned contact was formed using a salicide-like process which is compatible with CMOS process flow.

22.3 - 4:15 p.m.
High Mobility III-V-On-Insulator MOSFETs on Si with ALD-Al₂O₃
BOX Layers,

22.4 - 4:40 p.m.
Efficient Metallic Carbon Nanotube Removal Readily Scalable to Wafer-Level VLSI CNFET Circuits,
H. Wei, N. Patil, J. Zhang, A. Lin, H.-Y. Chen, H.-S.P. Wong, S. Mitra, Stanford University, USA

GENERAL INFORMATION
SCOPE OF SYMPOSIUM
The scope of the Symposium covers innovative areas such as new concepts and breakthroughs in VLSI processes and devices including Memory, Logic, I/O, and I/F (RF/Analog/Mixed-Signal/High-Voltage, Imager, MEMS, etc.; advanced gate stacks and interconnects in VLSI processes and devices; advanced lithography and fine-patterning technologies for high-density VLSI; new functional devices beyond CMOS with a path for VLSI implementation; packing of VLSI devices including 3D-system integration; advanced device analysis, materials and modeling for VLSIs; reliability related to the above devices; theories and fundamentals related to the above devices; new concepts and technologies for VLSI manufacturing; design enablement (including technology impacts on circuit design in advanced CMOS nodes); heterogeneous integration of non-Si substrates/materials on Si substrate

REGISTRATION INFORMATION:
When you register on-site, an additional $75 will be added to the registration fees.

Payment of the registration fee entitles the registrant to one copy of the Technical Digest, one CD-ROM, one banquet and one reception ticket.

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<thead>
<tr>
<th></th>
<th>Member</th>
<th>NonMember</th>
<th>Students</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tech Short Course</td>
<td>$295</td>
<td>$395</td>
<td>$100</td>
</tr>
<tr>
<td>Tech Symposium</td>
<td>$550</td>
<td>$650</td>
<td>$275</td>
</tr>
<tr>
<td>Circ Short Course</td>
<td>$350</td>
<td>$450</td>
<td>$125</td>
</tr>
<tr>
<td>Circ Symposium</td>
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<td>$275</td>
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<td>Circuits Luncheon</td>
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<td>Digest</td>
<td>$75</td>
<td>$75</td>
<td>$75</td>
</tr>
<tr>
<td>Add'l Short Course books</td>
<td>$95</td>
<td>$95</td>
<td>$95</td>
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<td>Banquet Tickets</td>
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REGISTRATION:
Credit Cards (MasterCard/Visa/Amex), personal checks, company checks or traveler’s checks payable to the 2010 VLSI Symposium in U.S. Dollars are the only acceptable forms of payment. All checks must be drawn on U.S. banks.

CANCELLATION POLICY:
All requests for refunds for registrations paid in US dollars must be made in writing and submitted to VLSI c/o Yes Events, PO Box 32862, Baltimore, MD 21282, USA
Fax: +1-410-559-2217 Email: vlsiinfo@yesevents.com

There will be a fee of $30 for all cancellations. No refunds will be issued for cancellations received after June 1, 2010. All refunds will be processed after the Symposium.

HOTEL RESERVATIONS
Hilton Hawaiian Village
2005 Kalua Road, Honolulu, HI 96815-1999 USA
Phone: +1 808-949-4321 Fax: +1 808-947-7914

A block of rooms has been reserved at the Hilton Hawaiian Village for 2010 VLSI Symposia participants. RESERVATIONS MUST BE RECEIVED BY May 19, 2010 to qualify for our special room rates:

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<tr>
<th>Room Type</th>
<th>Single/Double</th>
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</thead>
<tbody>
<tr>
<td>Garden View</td>
<td>$219.00</td>
</tr>
<tr>
<td>Ocean View</td>
<td>$245.00</td>
</tr>
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All rooms are subject to an 11.96% combined tax. To make a room reservation, go to www.vlsisymposium.org, click the tab at the top of the screen labeled Travel/Reservation Information. Click on the link for the hotel reservations.

All reservations must be accompanied by advanced deposit or guaranteed by a credit card in order to guarantee the reservation. A
confirmation will be mailed to you directly by the hotel. Check-in time is 2:00 pm and check-out is 11:00 am.

The hotel offers both non-smoking and handicapped rooms. Please make these specific requests when you make your hotel reservation.

TRANSPORTATION FROM THE HONOLULU INTERNATIONAL AIRPORT TO THE HILTON HAWAIIAN VILLAGE: Airport Express Shuttle and taxi services are available from the Honolulu International Airport to the hotel and return. Shuttle fare is approximately $15.00 each way. From the hotel to the airport you need to make a reservation one day in advance. Taxi fare is approximately $30.00 one way.

VISA REQUIREMENTS FOR ENTRY INTO U.S.: Citizens of foreign countries must have in their possession a valid passport and visa upon entering the United States. Foreign participants should contact the United States Embassy, Consulate, or Office of Tourism in their home country AS SOON AS POSSIBLE to determine their particular visa requirements.

SYMPOSIUM REGISTRATION DESK: The Symposia Registration Desk, located in the Palace Lounge Lobby will be open as follows:

<table>
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<tr>
<th>Day</th>
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<tr>
<td>Sunday, June 13</td>
<td>4:00 pm – 6:00 pm</td>
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<tr>
<td>Monday, June 14</td>
<td>7:30 am - 5:00 pm</td>
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<td>Tuesday, June 15</td>
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<td>Wednesday, June 16</td>
<td>7:30 am - 5:00 pm</td>
</tr>
<tr>
<td>Thursday, June 17</td>
<td>8:00 am – 5:00 pm</td>
</tr>
<tr>
<td>Friday, June 18</td>
<td>8:00 am – 3:00 pm</td>
</tr>
</tbody>
</table>

SYMPOSIA ON VLSI TECHNOLOGY AND VLSI CIRCUITS RECEPTION: A joint reception for both Technology and Circuits will be held on Tuesday, June 15 from 6:00 pm to 8:00 pm on the Lagoon Green.

SYMPOSIA ON VLSI TECHNOLOGY AND VLSI CIRCUITS BANQUET: The 2010 Symposia on VLSI Technology and VLSI Circuits Banquet will be held on Wednesday, June 17 on the Lagoon Green from 7:00 pm to 9:00 pm. Banquet tickets for accompanying guests can be purchased at the Registration desk in the Palace Lounge Lobby.

 SPEAKER PREPARATION CENTER: There will be a designated Speaker Preparation Room. Specifics will be available at the Registration Desk located in the Palace Lounge Lobby.

DIGEST: Registrants will receive (1) copy of the Digest and (1) copy of the CD-Rom when they pick up their Symposium materials at the Registration Desk. Additional copies of the Digest will be available on-site for $75. Following the Symposium, additional copies of the Digest will be available through IEEE Single Copy Sales, 445 Hoes Lane, Piscataway, NJ 08855, USA +1 732-981-0060 or (Toll free) 1 800-678-4333.

TRAVEL EXPENSE SUPPORT: Requests for partial travel expense support for students who are presenting papers should be sent to: the Secretariat USA, 19803 Laurel Valley Place, Montgomery Village, MD, 20886 USA  Fax: 301-527-0994 Email: vlsi@vlsisymposium.org  no later than April 25, 2010. All travel support will be paid after the Symposia.

MESSAGE CENTER: The Message Board will be located in the Palace Lounge Lobby adjacent to the Registration Desk. Please advise those who wish to reach you during the day to contact the Hilton Hawaiian Village at 808-949-4321 and request the VLSI Symposia Message Desk. Facsimiles clearly marked with both the recipient's name and the name of the Symposia may be sent to 808-947-7914.

ADDITIONAL INFORMATION: Additional information is available at:
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To obtain an Advance Program and other general information or to be placed on the Symposia mailing list, please contact:

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