We have investigated effects of the oxygen doping into TaCx on the effective work function ($\Phi_{m,\text{eff}}$) in TaCx/SiO2/Si and TaCx/HfO2/Si gate stacks. It has been found for the first time that the threshold voltage ($V_{th}$) is tunable within 0.5~0.6V for HfO2 MOSFETs by adjusting the oxygen content within 0~12 at. % in TaCx. Furthermore, it has been shown that unknown oxygen content in TaCx gates is a possible origin of scattering among the $\Phi_{m,\text{eff}}$ data reported.

We are reporting for the first time on the use of simple resist-based selective high-k dielectric capping removal processes of La2O3, Dy2O3 and Al2O3 on both HfSiO(N) and SiO2 to fabricate functional HK/MG CMOS ring oscillators with 40% fewer process steps compared to our previous report [1]. Both selective high-k removal (using wet chemistries) and resist strip processes (using NMP and APM) have been characterized physically and electrically indicating no major impact on $V_t$, EOT, $J_g$, mobility and gate dielectric integrity (PBTI, TDDB).

We demonstrate midgap and band-edge effective workfunctions (EWFs) control with simple metal gate process scheme (single metal gate/single gate dielectric), using impurity-segregated NiSi2/SiON structure for embedded memory application. The application of midgap and band-edge EWF enables us to lower power consumption in SRAM and logic devices by 30% and 15% compared to poly-Si devices, respectively, due to reduced channel impurity concentration, suppressed gate depletion and high carrier mobility. These results show that NiSi2/SiON stack is one of the most promising candidates for future system on chip (SoC) devices with embedded memory.

A laminate design technology of metal gates is proposed to improve FET characteristics regardless of EOT and gate dielectric material. The laminated metal gate structures are basically composed of low-Rs(sheet resistance) metal/WF(work-function)-lowering layer/ WFM(WF determining metal). A thin WFM (~2 nm) laminated by the Si-based WF-lowering layer such as poly-Si or TaSiN brings an additional benefit of dramatic improvements in mobility and PBTI in nFETs. A thick WFM (~10 nm) suppresses the WF-lowering in pFETs. The concept of the laminate design is indispensable for improving the performance in CMOSFETs.