Tuesday, June 13, 10:15 a.m.
Chairpersons: L. Tran, Micron Technology
S.S. Chung, National Chiao-Tung University

3.1 – 10:15 a.m.
A 60nm NOR Flash Memory Cell Technology Utilizing Back Bias Assisted Band-to-Band Tunneling Induced Hot-Electron Injection (B4-Flash), S. Shukuri, N. Ajika, M. Mihara, K. Kobayashi, T. Endoh*, M. Nakashima, GENUSION, Inc., Hyogo, Japan, *Tohoku University, Sendai, Japan

A p-channel SONOS flash memory cell technology, which utilizes novel Back Bias assisted Band-to-Band tunneling induced hot-electron (B4-HE) injection, has been developed for NOR architecture. By applying a moderate back bias to the cell, the bit-line voltage can be reduced below 1.8V. Resulting that the proposed cell achieves the gate length of 60nm, for the first time. Proposed B4-HE injection scheme realizes not only extreme scalability but also high programming efficiency for NOR flash.

3.2 – 10:40 a.m.

As a promising candidate for future scaling direction, a fully 3-D NOR flash cell with recessed channel and cylindrical floating gate is investigated in this paper. Good process feasibility and comparable device characteristics are proven by a successful integration of 65nm 512Mb MLC NOR technology. By overcoming the channel length scaling limit, the 3-D cell provides a promising path for the continued scaling of the floating gate flash memories for 65nm and beyond.

3.3 – 11:05 a.m.

A new 64-cell NAND flash memory with asymmetric S/D (Source/Drain) structure for sub-40nm node technology and beyond has been successfully developed. To suppress short channel effect in NAND memory cell, asymmetric S/D consisting of optimized junction and inversion layer induced by fringe field of WL bias which is applied at NAND operation conditions is successfully utilized. 64-cell NAND string which is double number of cells used in current NAND string is also used to further reduce bit cost by achieving over 10% chip size reduction while almost maintaining MLC (Multi-Level-Cell) NAND performance requirements.

3.4 – 11:30 a.m.

For the first time, multi-level NAND flash memories with a 63 nm design rule are developed successfully using charge trapping memory cells of Si/SiO₂/SiN/Al₂O₃/TaN (TANOS). We successfully integrated TANOS cells into multi-gigabit multi-level NAND flash memory without changing the memory window and circuit design of the conventional floating-gate type NAND flash memories by improving erase speed. The evolved TANOS cells show four-level cell distribution which is free from program disturbance and a charge loss of less than 0.4 V at high temperature bake test.