Thursday, June 15, 8:30 a.m.
Chairpersons: M. Ieong, IBM TJ Watson Research Ctr.
N. Nagashima, Sony Corp.

17.1 – 8:30 a.m.

For the first time, a transistor performance improvement is achieved by increasing the tensile stress of O3-TEOS pre-metal dielectric (PMD) using a novel plasma treatment and integration scheme. Plasma-treated O3-TEOS films show more tensile stress value about twice than that of an as-deposited O3-TEOS film. The novel process shows up to 10% improvement of Ion for nMOS without any cost of pMOS degradation.

17.2 – 8:55 a.m.
**A Novel Cu Electrical Fuse Structure and Blowing Scheme Utilizing Crack-Assisted Mode for 90-45nm-Node and Beyond,** T. Ueda, H. Takaoka, M. Hamada, Y. Kobayashi, A. Ono, NEC Electronics Corporation, Kanagawa, Japan

This paper presents the redundancy technology that uses Cu wiring as electrical fuse (e-fuse) for the first time. The novel e-fuse employs “crack-assisted mode” to blow fuse-material (Cu wire). Because Cu wiring is used instead of gate poly electrode material, the technology is extendible from the present 90nm~65nm technology-node to a few generations beyond 45nm-node, where Cu wiring is still likely to be employed. This e-fuse technology achieves very high reliability of less than 0.001ppm defective rate. High stability of this new e-fuse has been proven with actual 90nm generation products.

17.3 – 9:20 a.m.
**A New Route to Ultra-High Density Memory Using the Micro to Nano Addressing Block (MNAB),** R.S. Shenoy, K. Gopalakrishnan, C. T. Rettner, L.D. Bozano, R.S. King, B. Kurdi, H.K. Wickramasinghe, IBM Almaden Research Center, San Jose, California

For the first time, we demonstrate sublithographic memory read/write operation using Micro to Nano Addressing Block (MNAB) decoders. Test structures are fabricated with integrated one-time programmable oxide ROM elements addressed using MNAB devices that have 4 sub-50 nm silicon fins at 140 nm period. Functional operation is obtained for all 4-bit ROM sequences and over different ROM cell areas.

17.4 – 9:45 a.m.

CMOS image sensor (CIS) of 5-mega pixel density has been successfully developed with the smallest pixels (1.7µm x 1.7µm) ever made. The newly introduced unique pixel architecture brought excellent optical symmetry and high electron capacity. Degradation of sensitivity and cross-talk can be suppressed with the optimization of the optical structure through proper color filter material and reduction of total aspect ratio (vertical stack height / pixel pitch) with Cu back end of line (BEOL).