The first 45nm node planar-SOI technology has been developed with 6T-SRAM cell of 0.296um2. An adequate static noise margin of 120mV is obtained even at 0.6V operation. Fine patterning with line pitch of 130nm and contact pitch of 140nm by optical lithography is demonstrated. Transistors with 30nm gate length and 27nm slim spacer operate at 1V/0.85V with excellent drive currents of 1000/740 and 530/420 uA/um for N-FET and P-FET, respectively. The P-FET current is the best reported so far.

2.2 — 10:45 a.m.

General Purpose and Low Power 0.5µm² 6T-SRAM bit-cell was developed for 65nmCMOS platform using low cost CMOS process flow. Fully functional bit-cells show 240mV SNM and 35µA cell current at 1.2V operation. GP Ion measured 875µA/µm and 400µA/µm for NMOS and PMOS respectively for Vdd=1V. Analog mixed signal transistor parameters show Vt matching (Avt=2.2mV.µm) and analog voltage gain factor (Gm/Gd>2000 for L=10µm). NBTI criteria at 125 C were achieved.

2.3 — 11:10 a.m.

This paper describes the first 45nm Node CMOS technology (CMOS6) with optimized Vdd, EOT and BEOL parameters. For this technology to be applicable from high performance CPU to mobile applications, three sets of core devices are presented which are compatible with 0.069um² trench capacitor DRAM and 0.247um² 6T.SRAM embedded memories.

2.4 — 11:35 a.m.

A novel transistor optimization strategy that supports the data retention mode of an SRAM is applied to a 65 nm low-power technology with cell area <0.5 um². It is shown that reducing GDL is critical to achieve 2pA/bit retention leakage current in the SRAM. Process optimizations for 20% GDL reduction and high Idn/Idp of 550/300 uA/µm were demonstrated.