An 86% electron mobility improvement and 20% \( I_{\text{dn-sat}} \) enhancement were demonstrated for a 70nm strained-Si CMOS process fabricated on SiGe virtual substrates. Compared to bulk CMOS, strained-Si CMOS delivered 95% higher inverter peak-current and 2.2ps reduced ring oscillator delay for the same drive current. Strained and bulk CMOS featured equivalent gate leakage although higher dislocation-induced junction leakage on strained-Si was observed. Self-heating due to the lower thermal conductivity of SiGe reduces \( I_{\text{dn-sat}} \) by 7% during DC operation.