Ultra-Low Power and High Speed SRAM for Mobile Applications Using Single Poly-Si Gate 90nm CMOS Technology

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ABSTRACT

High speed and ultra-low power SRAM using single gate CMOS technology was developed. The drive currents of NMSOFET and PMOSFET were 410µA/µm and 205µA/µm, respectively. The random access time of 17ns at 1.65V operation voltage was achieved for the first time in low power application by the reduction of loading capacitance. Standby current was less than 15µA/chip. The highly manufacturable compact cell of 0.84 µm² area was integrated using PR (photo resist) flow technology and novel contact layout.