A Memory Using One-Transistor Gain Cell on SOI(FBC) with Performance Suitable for Embedded DRAM’s

Takashi Ohsawa, Tomoki Higashi\textsuperscript{1}, Katsuyuki Fujita, Tamio Ikehashi, Takeshi Kajiyama, Yoshiaki Fukuzumi, Tomoaki Shino, Hiroaki Yamada, Hiroomi Nakajima, Yoshihiro Minami, Takashi Yamada, Kazumi Inoh, Takeshi Hamamoto,

\textsuperscript{1}Design Solution Division, Toshiba Microelectronics Corp.
2-5-1 Kasama, Sakae-ku, Yokohama, Kanagawa 247-8585, Japan
Phone:+81-45-890-2420, Fax:+81-45-890-2893, E-mail:takashi5.oosawa@toshiba.co.jp

A 288Kbit memory featuring a one-transistor gain cell on SOI of the size 0.21um\textsuperscript{2} is presented and basic characteristics of the cell and the memory performance are disclosed. The threshold voltages of a cell transistor for data “1” and “0” are measured and a fail bit map is obtained. A sensing scheme is verified to be working and the random access time is measured. The retention time demonstrates to satisfy specifications for some embedded DRAM’s.