A low-power fourth order continuous-time complex $\Sigma\Delta$ ADC has been designed and fabricated for low-IF GSM and EDGE receivers in a 0.25 $\mu$m CMOS technology. This ADC has a bandwidth of 270 kHz centered around -100 kHz. The dynamic range is 82 dB at a sampling rate of 13 MHz even though the digital decimation filter and other blocks are active on the chip. The power consumption is 4.6 mW at 2 V supply.