A Fully Synchronized, Pipelined, and Re-Configurable 50Mb SRAM on 90nm CMOS Technology for Logic Applications

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A 50Mb SRAM chip is designed and fabricated on an industry leading 90nm CMOS technology that features a 1um^2 SRAM cell and 50nm gate length transistors with strained silicon. The SRAM chip is formed with 100x512Kb subarrays that have 2.5 GHz nominal operating frequency, 75% area efficiency, and fully synchronized internal timing along with efficient local power-down feature. And the design can be easily re-configured to form large high-density on-die cache memory for high-speed logic applications such as CPUs.