A High-Speed 128Kbit MRAM Core for Future Universal Memory Applications

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A 128Kb MRAM (Magnetic Random Access Memory) test chip has been fabricated utilizing for the first time a 0.18µm, VDD = 1.8V, logic process technology with Cu backend of line. The presented design uses a 1.4µm² 1T1MTJ (1-Transistor/1-Magnetic Tunnel Junction) cell and features a symmetrical high-speed sensing architecture using complementary reference cells and configurable load devices. Extrapolations from test chip measurements and circuit assessments predict a 5ns random array read access time and random write operations with <5ns write pulse width.