A 100 nm CMOS Technology with “Sidewall-Notched” 40 nm Transistors and SiC-Capped Cu/VLK Interconnects for High Performance Microprocessor Applications

Fujitsu Laboratories Ltd., C Project Group, 50 Fuchigami, Akiruno, Tokyo, 197-0833, Japan, E-mail: nakai@jp.fujitsu.com

*M. Kase, **M. Nakaishi, *M. Miyajima, *T. Ohba, and *I. Hanyu
Fujitsu Limited, Manufacturing Technology Development Div., 50 Fuchigami, Akiruno, Tokyo, 197-0833, Japan
**1500 Mizono, Tado-cho, Kuwana-gun, Mie, 511-0192, Japan

K. Yanai
Fujitsu Limited, LSI Quality Assurance Div.

We have developed a high performance 100 nm CMOS technology. High-NA 193 nm photolithography with phase shift mask and OPC allows 40 nm gate length and $0.999 \, \mu m^2$ SRAM cell. A sidewall-notched gate transistor suppresses variations of threshold voltage much better than poly-notched one. At off-currents of 100 nA/µm, on-currents are 890 µA/µm for NMOS and 380 µA/µm for PMOS. SiC-capped Cu/SiLK structure brings $k_{eff}$ of 3.0.