We have fabricated 55-nm poly-Si gated n- and p-MOSFETs with HfO$_2$ gate dielectric of 3-nm physical thickness deposited by atomic layer deposition (ALD). Conventional CMOS process was used with high-temperature source-drain anneal of $≥1000^\circ$C, cobalt-silicide and pocket implant. The devices showed very promising characteristics for low standby power applications due to drastic reduction of gate leakage current.