We have integrated high speed and high density 6T-SRAM cell of 0.998 \( \mu \text{m}^2 \) for system-on-a-chip (SOC) using enhanced 100nm CMOS logic technology. This is achieved by the systematic integration methodology, which includes high-NA ArF lithography, optimized optical proximity correction (OPC) CAD, narrow well isolation, poly-buffered shallow trench isolation (STI), offset spacer transistor, 9-level Cu interconnect and low-k dielectric technologies with the lithographically scalable SRAM cell design.