Employment of \(<100>\) channel direction in a strained-Si<sub>0.8</sub>Ge<sub>0.2</sub>p-MOSFET has demonstrated the substantial amount of hole mobility enhancement as large as 25% and parasitic resistance reduction of 20% compared to a \(<110>\) strained-Si<sub>0.8</sub>Ge<sub>0.2</sub> channel p-MOSFET, which already has an advantage in mobility and the threshold voltage roll-off characteristic over the Si p-MOSFET. This result indicates that the \(<100>\) strained SiGe channel p-MOSFET is a promising and practical candidate for realizing high-speed CMOS devices under low-voltage operation.