A differential-capacitance read scheme keeps the plateline voltage constant at ground and begins sensing the stored data immediately after a wordline is raised, hence eliminating the time spent in conventional read schemes in raising the highly capacitive plateline and in charge sharing of the bitlines with the ferroelectric capacitors. The proposed read scheme is used in a 256x128-bit testchip that features both 2T-2C and 1T-1C cells in 0.35µm technology. The read scheme achieves a 40% reduction in access time.