Selective Node Engineering for Chip-Level Soft Error Rate Improvement

Tanay Karnik, Sriram Vangal, V. Veeramachaneni, Peter Hazucha, Vasantha Erraguntla, Shekhar Borkar
Circuit Research, Intel Labs,
Hillsboro, OR, U.S.A.

This paper presents a technique to selectively engineer sequential or domino nodes in high performance circuits to improve soft error rate (SER) induced by cosmic rays or alpha particles. In 0.18μm process, the SER improvement is as much as 3X at the cell-level, 1.8X at the block-level and 1.3X at the chip-level without any penalty in performance or area, and <3% power penalty. The node selection, hardening and SER quantification steps are fully automated.