A so-called $\mu$I/O architecture, to provide low-cost system solutions with a 0.13-$\mu$m dual-$t_{\text{ox}}$ CMOS and multi-chip package (MCP) technologies, was developed. It provides a common interface and hierarchical I/O design for MCPs and, thus, enables high design reusability for short turnaround. It includes a signal-level converter for integrating wide-supply-voltage-range (0.75-1.3 or 1.5-3.6 V) circuit blocks, and a signal-wall function for turning off each block independently—without invalid signal transmission—by using an internal power switch.