We have developed a cylindrical Ru/ST/Ru capacitor for gigabit-scale DRAMs. Using cylindrical CVD-Ru as storage node (SN), a new 2-step CVD-ST was employed to improve ST step coverage, surface morphology and to control composition at Ru/ST interface. A SiO₂ equivalent thickness (teq) of 0.6nm and cell capacitance of 18 fF/cell with leakage current of 0.1fA/cell at ±0.7V applied voltage has been achieved on 256K cylindrical Ru/ST/Ru capacitor array.