A High Performance 100 nm Generation SOC Technology [CMOS IV] for High Density Embedded Memory and Mixed Signal LSIs


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Abstract

This paper demonstrates a 100 nm generation SOC technology [CMOS IV] for the first time. Three types of core devices are presented with optimized gate oxynitrides for their stand-by power conditions. This advanced LOGIC process is compatible with 0.18 \( \mu m^2 \) trench capacitor DRAM and 1.25 \( \mu m^2 \) 6 Tr. SRAM. Two kinds of high \( V_{dd} \) devices can be prepared by triple gate oxide process. Moreover, for mixed signal applications, TaOx MIM capacitors are introduced into Cu and low-k interconnects.