A Post-Package Bit-Repair Scheme Using Static Latches with Bipolar-Voltage Programmable Antifuse Circuit for High-Density DRAMs

Kyeong-Sik Min*, Jong-Tai Park, Sang-Pil Lee, Young-Hee Kim, Tae-Heum Yang, Jong-Doo Joo, Kyung-Mi Lee, Jae-Kyung Wee, and Jin-Yong Chung

Memory R&D Division, Hyundai Electronics Industries Co. Ltd.
*1, Hyangjeong-dong, Hungduk-gu, Cheongju-si, 361-725, Korea
San 136-1, Ami-ri, Bubal-eub, Ichon-si, Kyoungki-do, 467-701, Korea

A post-package bit-repair scheme using static latches with bipolar-voltage programmable antifuse circuit is proposed in this paper. Here, the antifuses are programmed by bipolar voltages of Vcc and -Vcc, alleviating high-voltage problems and achieving a smaller layout area than the previous scheme. In addition, an efficient bit-repair scheme is used instead of the conventional line-repair one, reducing a layout area for the redundancy bits. And, using the static latches instead of the dynamic memory cells for the redundancy bits eliminates possible defects in the redundancy area, making this scheme robust.