Parametric Yield Enhancement System via Circuit Level Device Optimization using Statistical Circuit Simulation

Mikako Miyama, Shiro Kamohara, Kousuke Okuyama, Yuzuru Oji
Semiconductor & Integrated Circuits Div, Hitachi, Ltd.
Kokubunji-shi, Tokyo, Japan

To achieve high yield products, it is important to optimize the device condition, considering the process variation. We present a statistical model parameter extraction methodology to accurately extract the process variation from the E-T data. We have estimated the parametric yield of a 0.20μm process SRAM test chip using Monte Carlo simulation and have obtained good agreement comparing to measurement. We also performed device optimization using a critical path to improve the parametric yield.