An SOI CMOS LVDS Driver and Receiver Pair

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A low-voltage differential signaling (LVDS) driver and receiver pair utilizing source-body-tied silicon-on-insulator CMOS transistors is shown to operate at 1Gb/s data rates with zero bit error rate using a $2^{31}-1$ pseudo-random bit sequence. For the driver, a level-shifter with gate voltage protection transitions from thin oxide core transistors to DGO output transistors. The receiver uses parallel PFET and NFET dual gate oxide transistors to enable common-mode input from 0-2.4V.